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Understanding Embedded - Microprocessors

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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544eavtaqga

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



MPC8544E Overview

- Two key (K1, K2, K1) or three key (K1, K2, K3)
- ECB and CBC modes for both DES and 3DES
- AESU—Advanced Encryption Standard unit
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, CTR, and CCM modes
 - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- MDEU—message digest execution unit
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- KEU-Kasumi execution unit
 - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
 - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I^2C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data bus operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
 - Two protocol engines available on a per chip select basis:

Electrical Characteristics

	Characteristic	Symbol	Recommended Value	Unit	Notes
Three-speed Ethe	ernet I/O voltage	LV _{DD} (eTSEC1)	3.3 V ± 165 mV 2.5 V ± 125 mV	V	4
		TV _{DD} (eTSEC3)	3.3 V ± 165 mV 2.5 V ± 125 mV		
PCI, DUART, PCI and JTAG I/O vol	Express, system control and power management, I ² C, tage	OV _{DD}	3.3 V ± 165 mV	V	3
Local bus I/O volt	age	BV _{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	5
Input voltage	DDR and DDR2 DRAM signals	MV _{IN}	GND to GV _{DD}	V	2
	DDR and DDR2 DRAM reference	MV _{REF}	GND to GV _{DD} /2	V	2
Three-speed Ethernet signals		LV _{IN} TV _{IN}	GND to LV _{DD} GND to TV _{DD}	V	4
	Local bus signals	BV _{IN}	GND to BV _{DD}	V	5
	PCI, Local bus, DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	OV _{IN}	GND to OV _{DD}	V	3
Junction tempera	ture range	Τj	0 to 105	°C	—

Table 2. Recommended Operating Conditions (continued)

Notes:

1. This voltage is the input to the filter discussed in Section 21.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

2. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

4. Caution: T/LV_{IN} must not exceed T/ LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

5. Caution: BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.



Enhanced Three-Speed Ethernet (eTSEC), MII Management

Parameter		Symbol	Min	Тур	Max	Unit	Notes
Input differential voltage	LSTS = 0	V _{rx_diffpp}	100	—	1200	mV	2, 4
	LSTS = 1	1	175	—			
Loss of signal threshold	LSTS = 0	VI _{os}	30	—	100	mV	3, 4
	LSTS = 1	1	65	—	175		
Input AC common mode voltage		V _{cm_acpp}	—	—	100	mV	5.
Receiver differential input impedance		Zrx_diff	80	—	120	Ω	
Receiver common mode input impedance		Zrx_cm	20	—	35	Ω	—
Common mode input voltage		Vcm	xcorevss	—	xcorevss	V	6

Table 25. DC Receiver Electrical Characteristics (continued)

Notes:

1. Input must be externally AC-coupled.

- 2. $V_{RX_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage
- 3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to Section 17.4.3, "Differential Receiver (RX) Input Specifications," for further explanation.
- 4. The LSTS shown in this table refers to the LSTSCD bit field of MPC8544E SerDes 2 control register 1.
- 5. V_{CM ACp-p} is also referred to as peak-to-peak AC common mode voltage.
- 6. On-chip termination to SGND_SRDS2 (xcorevss).

8.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs ($SD2_TX[n]$ and $\overline{SD2_TX[n]}$) or at the receiver inputs ($SD2_RX[n]$ and $\overline{SD2_RX[n]}$) as depicted in Figure 10, respectively.

8.4.1 SGMII Transmit AC Timing Specifications

Table 26 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 26. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XVDD_SRDS2 = $1.0 V \pm 5\%$.

Parameter	Symbol	Min	Тур	Мах	Unit	Notes
Deterministic jitter	J _D	—	—	0.17	UI p-p	—
Total jitter	J _T	—	—	0.35	UI p-p	—
Unit interval	UI	799.92	800	800.08	ps	2
V _{OD} fall time (80%–20%)	t _{fall}	50	—	120	ps	—
V _{OD} rise time (20%–80%)	t _{rise}	50	—	120	ps	—

Notes;

1. Source synchronous clock is not supported.

2. Each UI value is 800 ps \pm 100 ppm.



Enhanced Three-Speed Ethernet (eTSEC), MII Management

8.5.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.5.2.1 GMII Transmit AC Timing Specifications

Table 30 provides the GMII transmit AC timing specifications.

Table 30. GMII Transmit AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{GTX}	—	8.0	—	ns	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t _{GTKHDX}	0.2	—	5.0	ns	2
GTX_CLK data clock rise time (20%-80%)	t _{GTXR}	—	—	1.0	ns	—
GTX_CLK data clock fall time (80%-20%)	t _{GTXF}	—	—	1.0	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

2. Data valid t_{GTKHDV} to GTX_CLK Min setup time is a function of clock period and max hold time (Min setup = cycle time – Max delay).

Figure 13 shows the GMII transmit AC timing diagram.



Figure 13. GMII Transmit AC Timing Diagram



Table 45. Local Bus General Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled (continued)

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	_	2.5	ns	5

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
</sub>

2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.

3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.

4. Input timings are measured at the pin.

5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

- 6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.

Table 46 describes the general timing parameters of the local bus interface at $BV_{DD} = 2.5$ V.

Table 46. Local Bus General Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	12	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{lbkskew}	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	2.4	—	ns	3, 4
LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.8	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t _{lbotot}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	_	2.8	ns	_
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	2.8	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	2.8	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}	—	2.8	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	—	2.6	ns	5





Figure 33. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

11 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).



Table 50. JTAG AC Timing Specifications (Independent of SYSCLK)¹ (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol ²	Min	Мах	Unit	Notes
JTAG external clock to output high impedance:				ns	5
Boundary-scan data	t _{JTKLDZ}	3	19		
TDO	t _{JTKLOZ}	3	9		

Notes:

- 2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK} .

Figure 34 provides the AC test load for TDO and the boundary-scan outputs.



Figure 34. AC Test Load for the JTAG Interface

Figure 35 provides the JTAG clock input timing diagram.



 $VM = Midpoint Voltage (OV_{DD}/2)$

Figure 35. JTAG Clock Input Timing Diagram

Figure 36 provides the TRST timing diagram.



All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 34). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.



Figure 37 provides the boundary-scan timing diagram.



Figure 37. Boundary-Scan Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8544E.

13.1 I²C DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the I²C interfaces.

Table 51. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
Input high voltage level	V _{IH}	$0.7\times \text{OV}_{\text{DD}}$	OV _{DD} + 0.3	V	_
Input low voltage level	V _{IL}	-0.3	$0.3\times\text{OV}_{\text{DD}}$	V	_
Low level output voltage	V _{OL}	0	$0.2\times\text{OV}_{\text{DD}}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$ (max)	Ι _Ι	-10	10	μA	3
Capacitance for each I/O pin	CI	_	10	pF	_

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

2. Refer to the MPC8544EPowerQUICC III Integrated Communications Host Processor Reference Manual for information on the digital filter used.

3. I/O pins will obstruct the SDA and SCL lines if $\ensuremath{\mathsf{OV}_{\text{DD}}}$ is switched off.

Figure 42 shows the PCI input AC timing conditions.



Figure 42. PCI Input AC Timing Measurement Conditions

Figure 43 shows the PCI output AC timing conditions.



Figure 43. PCI Output AC Timing Measurement Condition

16 High-Speed Serial Interfaces (HSSI)

The MPC8544E features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 dedicated for PCI Express data transfers. The SerDes2 can be used for PCI Express and/or SGMII application. This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 44 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{SDn}_T\overline{X}$) or a receiver input (SD*n*_RX and $\overline{SDn}_R\overline{X}$). Each signal swings between A Volts and B Volts where A > B.



High-Speed Serial Interfaces (HSSI)



Figure 54. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 8.3.1, "The DBWO Signal"
- Section 17.2, "AC Requirements for PCI Express SerDes Clocks"

16.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/SD1_REF_CLK were designed to work with a spread spectrum clock (+0 to -0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/SD2_REF_CLK are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

16.3 SerDes Transmitter and Receiver Reference Circuits

Figure 55 shows the reference circuits for SerDes data lane's transmitter and receiver.



Figure 55. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in the section below (PCI Express or SGMII) in this document based on the application usage:

- Section 8.3, "SGMII Interface Electrical Characteristics"
- Section 17, "PCI Express"

Please note that external AC Coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in specification of each protocol section.



Table 59. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
T _{crosslink}	Crosslink random timeout	0		1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 58 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 56.)
- 3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of T_{TX-JITTER-MAX} = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The T_{TX-EYE-MEDIAN-to-MAX-JITTER} median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- 4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 58.) Note that the series capacitors C_{TX} is optional for the return loss measurement.
- 5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 58 for both V_{TX-D+} and V_{TX-D-} .
- 6. See Section 4.3.1.8 of the PCI Express Base Specifications, Rev 1.0a.
- 7. See Section 4.2.6.3 of the PCI Express Base Specifications, Rev 1.0a.

17.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 56 is specified using the passive compliance/test measurement load (see Figure 58) in place of any real PCI Express interconnect +RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).



Table 60. Differential Receiver	(RX) Input S	pecifications	(continued)
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Symbol	Parameter	Min	Nom	Max	Units	Comments
L _{TX-SKEW}	Total skew			20	ns	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 58 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 57). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes, see Figure 58). Note that the series capacitors CTX is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5-ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
- 6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 57 is specified using the passive compliance/test measurement load (see Figure 58) in place of any real PCI Express RX component.

In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 58) will be larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 57) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.



Package Description

Signal Package Pin Number		Pin Type	Power Supply	Notes				
DDR SDRAM Memory Interface								
MDQ[0:63]	A26, B26, C22, D21, D25, B25, D22, E21, A24, A23, B20, A20, A25, B24, B21, A21, E19, D19, E16, C16, F19, F18, F17, D16, B18, A18, A15, B14, B19, A19, A16, B15, D1, F3, G1, H2, E4, G5, H3, J4, B2, C3, F2, G2, A2, B3, E1, F1, L5, L4,N3, P3, J3, K4, N4, P4, J1, K1, P1, R1, J2, K2, N1, R2	I/O	GV _{DD}	_				
MECC[0:7]	G12, D14, F11, C11, G14, F14,C13, D12	I/O	GV _{DD}	—				
MDM[0:8]	C25, B23, D18, B17, G4, C2, L3, L2, F13	0	GV _{DD}	21				
MDQS[0:8]	D24, B22, C18, A17, J5, C1, M4, M2, E13	I/O	GV _{DD}	—				
MDQS[0:8]	C23, A22, E17, B16, K5, D2, M3, P2, D13	I/O	GV _{DD}	_				
MA[0:15]	B7, G8, C8, A10, D9, C10, A11, F9, E9, B12, A5, A12, D11, F7, E10, F10	0	GV _{DD}	_				
MBA[0:2]	A4, B5, B13	0	GV _{DD}	_				
MWE	B4	0	GV _{DD}	—				
MCAS	E7	0	GV _{DD}	—				
MRAS	C5	0	GV _{DD}	_				
MCKE[0:3]	H10, K10, G10, H9	0	GV _{DD}	10				
MCS[0:3]	D3, H6, C4, G6	0	GV _{DD}	—				
MCK[0:5]	A9, J11, J6, A8, J13, H8	0	GV _{DD}	_				
MCK[0:5]	B9, H11, K6, B8, H13, J8	0	GV _{DD}	_				
MODT[0:3]	E5, H7, E6, F6	0	GV _{DD}	—				
MDIC[0:1]	H15, K15	I/O	GV _{DD}	25				
TEST_IN	A13	I	—	27				
TEST_OUT	A6	0	—	17				
	Local Bus Controller Interfac	e	I					
LAD[0:31]	K22, L21, L22, K23, K24, L24, L25, K25, L28, L27, K28, K27, J28, H28, H27, G27, G26, F28, F26, F25, E28, E27, E26, F24, E24, C26, G24, E23, G23, F22, G22, G21	I/O	BV _{DD}	23				
LDP[0:3]	K26, G28, B27, E25	I/O	BV _{DD}					
LA[27]	L19	0	BV _{DD}	4, 8				
LA[28:31]	K16, K17, H17,G17	0	BV _{DD}	4, 6, 8				
LCS[0:4]	K18, G19, H19, H20, G16	0	BV _{DD}	—				
LCS5/DMA_DREQ2	H16	I/O	BV _{DD}	1				

Table 62. MPC8544E Pinout Listing (continued)



Table 62. MPC8544E Pinout Listing (continued	Table 62	. MPC8544E	Pinout	Listing	(continued
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Signal	Signal Package Pin Number		Power Supply	Notes			
UART_SIN[0:1]	AG7, AH6	I	OV _{DD}				
UART_SOUT[0:1]	AH7, AF7	0	OV _{DD}				
	I ² C interface						
IIC1_SCL	AG21	I/O	OV _{DD}	20			
IIC1_SDA	AH21	I/O	OV _{DD}	20			
IIC2_SCL	AG13	I/O	OV _{DD}	20			
IIC2_SDA	AG14	I/O	OV _{DD}	20			
	SerDes 1						
SD1_RX[0:7]	N28, P26, R28, T26, Y26, AA28, AB26, AC28	I	XV _{DD}	_			
SD1_RX[0:7]	N27, P25, R27, T25, Y25, AA27, AB25, AC27	I	XV _{DD}				
SD1_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	0	XV _{DD}				
SD1_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	0	XV _{DD}				
SD1_PLL_TPD	V28	0	XV _{DD}	17			
SD1_REF_CLK	U28	I	XV _{DD}	_			
SD1_REF_CLK	U27	I	XV _{DD}	_			
SD1_TST_CLK	T22		—	—			
SD1_TST_CLK	Т23		—	—			
	SerDes 2						
SD2_RX[0]	AD25	I	xv _{DD}	—			
SD2_RX[2]	AD1	I	XV _{DD}	26			
SD2_RX[3]	AB2	I	XV _{DD}	26			
SD2_RX[0]	AD26	I	XV _{DD}	—			
SD2_RX[2]	AC1	I	XV _{DD}	26			
SD2_RX[3]	AA2	I	XV _{DD}	26			
SD2_TX[0]	AA21	0	XV _{DD}	—			
SD2_TX[2]	AC4	0	xv _{DD}	26			
SD2_TX[3]	AA5	0	XV _{DD}	26			
SD2_TX[0]	AA20	0	XV _{DD}	—			
SD2_TX[2]	AB4	0	XV _{DD}	26			
SD2_TX[3]	Y5	0	XV _{DD}	26			
SD2_PLL_TPD	AG3	0	XV _{DD}	17			
SD2_REF_CLK	AE2	I	XV _{DD}	—			



Package Description

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
SD2_REF_CLK	AF2	I	xv _{DD}	—			
SD2_TST_CLK	AG4	_	—	—			
SD2_TST_CLK	AF4	_	—	—			
	General-Purpose Output						
GPOUT[0:7]	AF22, AH23, AG27, AH25, AF21, AF25, AG26, AF26	0	OV _{DD}	_			
	General-Purpose Input			•			
GPIN[0:7]	AH24, AG24, AD23, AE21, AD22, AF23, AG25, AE20	I	OV _{DD}	_			
	System Control		I				
HRESET	AG16	I	OV _{DD}	—			
HRESET_REQ	AG15	0	OV _{DD}	21			
SRESET	AG19	I	OV _{DD}	—			
CKSTP_IN	AH5	I	OV _{DD}	—			
CKSTP_OUT	AA12	0	OV _{DD}	2, 4			
	Debug						
TRIG_IN	AC5	I	OV _{DD}	—			
TRIG_OUT/READY/ QUIESCE	AB5	0	OV _{DD}	5, 8, 15, 21			
MSRCID[0:1]	Y7, W9	0	OV _{DD}	4, 5, 8			
MSRCID[2:4]	AA9, AB6, AD5	0	OV _{DD}	5, 15, 21			
MDVAL	Y8	0	OV _{DD}	5			
CLK_OUT	AE16	0	OV _{DD}	10			
	Clock						
RTC	AF15	I	OV _{DD}	—			
SYSCLK	AH16		OV _{DD}	—			
JTAG							
тск	AG28		OV _{DD}	—			
TDI	AH28		OV _{DD}	11			
TDO	AF28	0	OV _{DD}	10			
TMS	AH27	I	OV _{DD}	11			
TRST	AH22	I	OV _{DD}	11			



Package Description

Table 62. MPC8544E Pinout Listing (continued)

		(,		
Signal	Package Pin Number	Pin Type	Power Supply	Notes
6.The value of LA[28:31] du resistors. See Section 1	ring reset sets the CCB clock to SYSCLK PLL ration 9.2. "CCB/SYSCLK PLL Ratio."	o. These pins requ	ire 4.7-k Ω pull-up (or pull-down

- 7.The value of LALE, LGPL2, and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 19.3, "e500 Core PLL Ratio."
- 8. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. Therefore, this pin will be described as an I/O for boundary scan.
- 9. For proper state of these signals during reset, DMA_DACK[1] must be pulled down to GND through a resistor. DMA_DACK[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on DMA_DACK[0].
- 10. This output is actively driven during reset rather than being three-stated during reset.
- 11. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 12. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
- 13. Anode and cathode of internal thermal diode.
- 14.Treat pins AC7, T5, V2, and M7 as spare configuration pins cfg_spare[0:3]. The spare pins are unused POR config pins. It is highly recommended that the customer provide the capability of setting these pins low (that is, pull-down resistor which is not currently stuffed) in order to support new config options should they arise between revisions.
- 15.If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
- 16. This pin is only an output in FIFO mode when used as Rx flow control.

17.Do not connect.

18. These are test signals for factory use only and must be pulled up (100 Ω to 1 k Ω) to OV_{DD} for normal machine operation.

- 19.Independent supplies derived from board $\ensuremath{\mathsf{V}_{\text{DD}}}$.
- 20.Recommend a pull-up resistor (1 K~) be placed on this pin to OV_{DD} .
- 21. The following pins must not be pulled down during power-on reset: HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], and ASLEEP.
- 22. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven.
- 23.General-purpose POR configuration of user system.
- 24.When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the address pins as No Connect or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the address pins are not connected to any other PCI device. The PCI block will drive the address pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
- 25.MDIC0 is grounded through an 18.2-Ω precision 1% resistor and MDIC1 is connected GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
- 26.For SGMII mode.

27.Connect to GND.

28. For systems that boot from a local bus (GPCM)-controlled flash, a pull-up on LGPL4 is required.



19.5 Security Controller PLL Ratio

Table 67 shows the SEC frequency ratio.

Table 67. SEC Frequency Ratio

Signal Name	Value (Binary)	CCB CLK:SEC CLK
LWE_B	0	2:1 ¹
	1	3:1 ²

Notes:

1. In 2:1 mode the CCB frequency must be operating ≤ 400 MHz.

2. In 3:1 mode any valid CCB can be used. The 3:1 mode is the default ratio for security block.

19.6 Frequency Options

19.6.1 SYSCLK to Platform Frequency Options

Table 68 shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

CCB to SYSCLK Ratio	SYSCLK (MHz)						
	33.33	41.66	66.66	83	100	111	133.33
			Platform	CCB Freque	ncy (MHz)	·	
2							
3					—	333	400
4			—	333	400	445	533
5			333	415	500		
6			400	500		-	
8		333	533		-		
9		375					
10	333	417					
12	400	500					
16	533		-				

 Table 68. Frequency Options of SYSCLK with Respect to Memory Bus Speeds



19.6.2 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed. Refer to Section 4.4, "Platform to FIFO Restrictions," for additional information.

Platform Speed (MHz)	Maximum FIFO Speed for Reference Clocks TSEC <i>n</i> _TX_CLK, TSEC <i>n</i> _RX_CLK (MHz) ¹
533	126
400	94

Table 69. FIFO Maximum Speed Restrictions

Note:

1. FIFO speed should be less than 24% of the platform speed.

20 Thermal

This section describes the thermal specifications of the MPC8544E.

20.1 Thermal Characteristics

Table 70 provides the package thermal characteristics.

 Table 70. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single layer board (1s)	R_{\thetaJA}	26	°C/W	1, 2
Junction-to-ambient natural convection	Four layer board (2s2p)	$R_{ extsf{ heta}JA}$	21	°C/W	1, 2
Junction-to-ambient (@200 ft/min)	Single layer board (1s)	$R_{ extsf{ heta}JA}$	21	°C/W	1, 2
Junction-to-ambient (@200 ft/min)	Four layer board (2s2p)	$R_{ extsf{ heta}JA}$	17	°C/W	1, 2
Junction-to-board thermal	—	$R_{ extsf{ heta}JB}$	12	°C/W	3
Junction-to-case thermal	_	R_{\thetaJC}	<0.1	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.

3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1°C/W.



Figure 62 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance.)

Figure 62. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

20.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 63 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.



22.2 Nomenclature of Parts Fully Addressed by this Document

Table 75 provides the Freescale part numbering nomenclature for the MPC8544E.

Table 75. Device Nomenclature

MPC	nnnn	Ε	С	НХ	AA	X	В
Product Code	Part Identifier	Encryption Acceleration	Temperature Range	Package ¹	Processor Frequency ²	Platform Frequency	Revision Level
MPC	8544	Blank = not included E = included	B or Blank = Industrial Tier standard temp range(0° to 105°C) C = Industrial Tier Extended temp range(-40° to 105°C)	VT = FC-PBGA (lead-free) VJ = lead-free FC-PBGA	AL = 667 MHz AN = 800 MHz AQ = 1000 MHz AR = 1067 MHz	F = 333 MHz G = 400 MHz J = 533 MHz	Blank = Rev. 1.1 1.1.1 A = Rev. 2.1

Notes:

- 1. See Section 18, "Package Description," for more information on available package types.
- Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
- 3. The VT part number is ROHS-compliant, with the permitted exception of the C4 die bumps.
- 4. The VJ part number is entirely lead-free. This includes the C4 die bumps.

22.3 Part Marking

Parts are marked as in the example shown in Figure 70.



Notes:

MMMMM is the 5-digit mask number.

ATWLYYWW is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 70. Part Marking for FC-PBGA Device