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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.067GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544eavtarja

- Two key (K1, K2, K1) or three key (K1, K2, K3)
 - ECB and CBC modes for both DES and 3DES
- AESU—Advanced Encryption Standard unit
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, CTR, and CCM modes
 - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- MDEU—message digest execution unit
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- KEU—Kasumi execution unit
 - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
 - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data bus operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
 - Two protocol engines available on a per chip select basis:

- Three PCI Express interfaces
 - Two $\times 4$ link width interfaces and one $\times 1$ link width interface
 - PCI Express 1.0a compatible
 - Auto-detection of number of connected lanes
 - Selectable operation as root complex or endpoint
 - Both 32- and 64-bit addressing
 - 256-byte maximum payload size
 - Virtual channel 0 only
 - Traffic class 0 only
 - Full 64-bit decode with 32-bit wide windows
- Power management
 - Supports power saving modes: doze, nap, and sleep
 - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the 8 counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™-compliant, JTAG boundary scan
- 783 FC-PBGA package

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 35	$BV_{DD} = 3.3\text{ V}$ $BV_{DD} = 2.5\text{ V}$	1
	45 (default) 45 (default) 125	$BV_{DD} = 3.3\text{ V}$ $BV_{DD} = 2.5\text{ V}$ $BV_{DD} = 1.8\text{ V}$	
PCI signals	25	$OV_{DD} = 3.3\text{ V}$	2
	42 (default)		
DDR signal	20	$GV_{DD} = 2.5\text{ V}$	—
DDR2 signal	16 32 (half strength mode)	$GV_{DD} = 1.8\text{ V}$	—
TSEC signals	42	$LV_{DD} = 2.5/3.3\text{ V}$	—
DUART, system control, JTAG	42	$OV_{DD} = 3.3\text{ V}$	—
I ² C	150	$OV_{DD} = 3.3\text{ V}$	—

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSR.
2. The drive strength of the PCI interface is determined by the setting of the `PCI_GNT1` signal at reset.

2.2 Power Sequencing

The device requires its power rails to be applied in specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD} , AV_{DD-n} , BV_{DD} , LV_{DD} , SV_{DD} , OV_{DD} , TV_{DD} , XV_{DD}
2. GV_{DD}

Note that all supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, then the sequencing for GV_{DD} is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

4.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8544E. [Table 8](#) provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 8. RESET Initialization Timing Specifications¹

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	μs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYCLKs	1
PLL input setup time with stable SYCLK before $\overline{\text{HRESET}}$ negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYCLKs	1

Note:

1. SYCLK is the primary clock input for the MPC8544E.

[Table 9](#) provides the PLL lock times.

Table 9. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
Core and platform PLL lock times	—	100	μs	—
Local bus PLL	—	50	μs	—
PCI bus lock time	—	50	μs	—

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8544E. Note that DDR SDRAM is $\text{GV}_{\text{DD}}(\text{typ}) = 2.5 \text{ V}$ and DDR2 SDRAM is $\text{GV}_{\text{DD}}(\text{typ}) = 1.8 \text{ V}$.

Table 16 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 16. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	—	V	—

Table 17 provides the input AC timing specifications for the DDR SDRAM interface.

Table 17. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
533 MHz		−300	300		3
400 MHz		−365	365		—
333 MHz		−390	390		—

Notes:

- t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - \text{abs}(t_{CISKEW}))$, where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} . See Figure 3.
- Maximum DDR1 frequency is 400 MHz.

Figure 3 shows the DDR SDRAM input timing diagram.

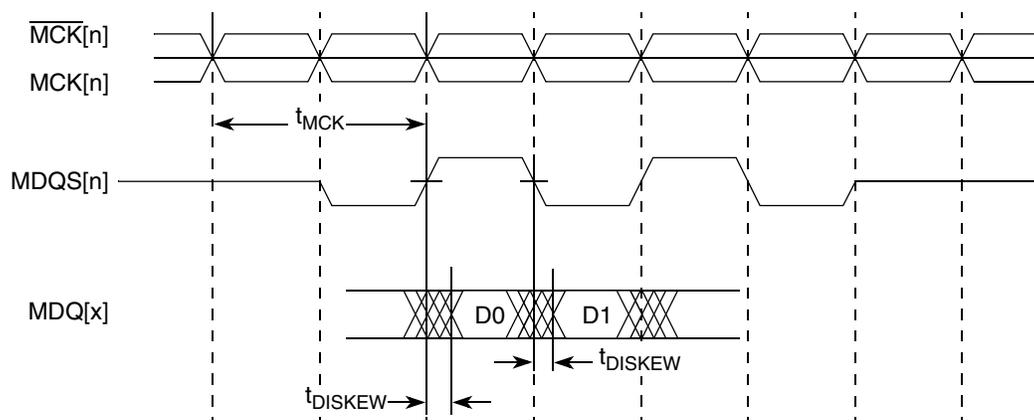


Figure 3. DDR SDRAM Input Timing Diagram (t_{DISKEW})

Figure 10 provides the AC test load for SGMII.

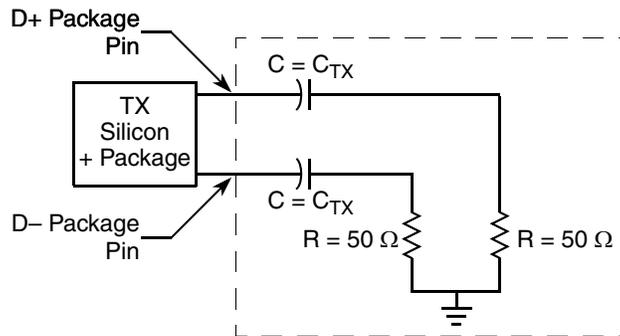


Figure 10. SGMII AC Test/Measurement Load

8.5 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.5.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC $_n$ TSEC $_n$ _TX_CLK, while the receive clock must be applied to pin TSEC $_n$ _RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC $_n$ _GTX_CLK pin (while transmit data appears on TSEC $_n$ _TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC $_n$ _GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver.

A summary of the FIFO AC specifications appears in [Table 28](#) and [Table 29](#).

Table 28. FIFO Mode Transmit AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TX_CLK, GTX_CLK clock period	t_{FIT}	—	8.0	—	ns	—
TX_CLK, GTX_CLK duty cycle	t_{FITH}	45	50	55	%	—
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps	—
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns	—

Table 46. Local Bus General Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	—	2.6	ns	5

Notes:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(First two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- All signals are measured from BV_{DD}/2 of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to 0.4 × BV_{DD} of the signal in question for 2.5-V signaling levels.
- Input timings are measured at the pin.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.

Table 47 describes the general timing parameters of the local bus interface at BV_{DD} = 1.8 V DC.

Table 47. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	12	ns	2
Local bus duty cycle	t _{LBKH} /t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	2.6	—	ns	3, 4
LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t _{LBOTOT}	1.2	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	3.2	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	3.2	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	3.2	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.9	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.9	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	—	2.6	ns	5

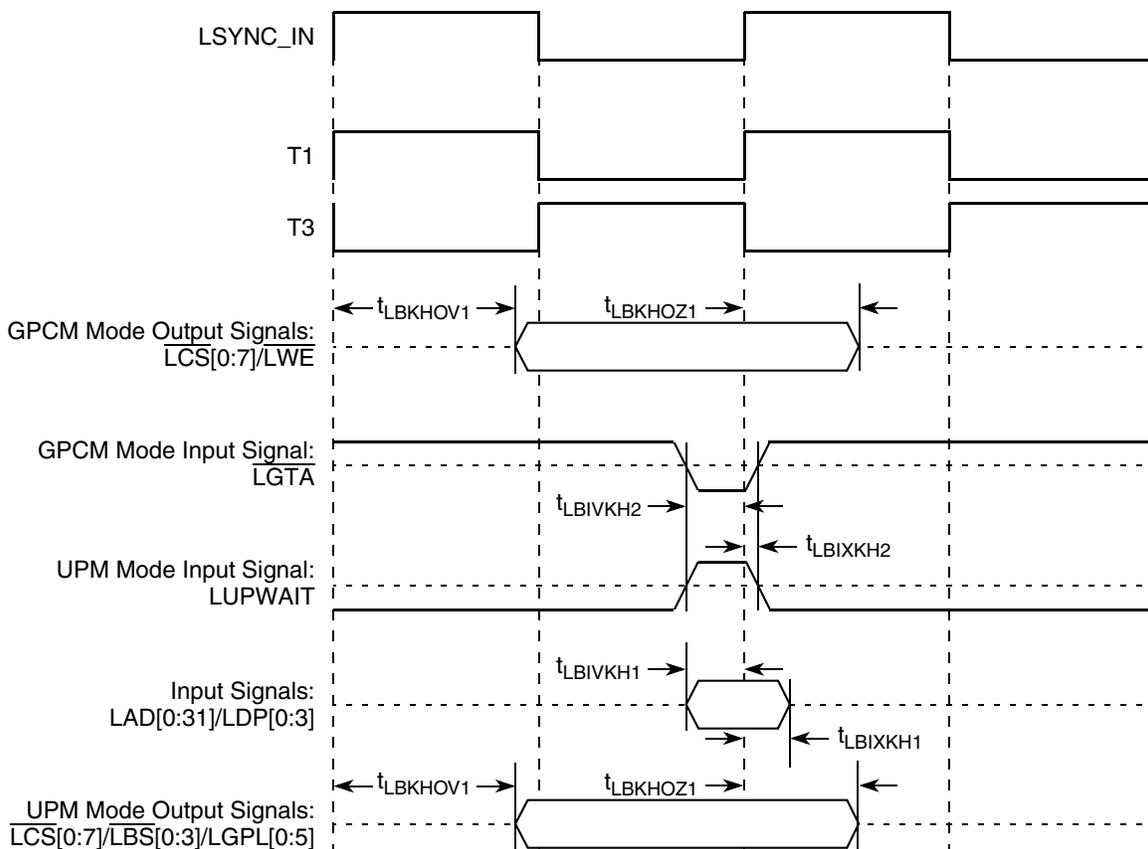


Figure 30. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)

13.2 I²C AC Electrical Specifications

Table 52 provides the AC timing parameters for the I²C interfaces.

Table 52. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 51).

Parameter	Symbol ¹	Min	Max	Unit	Notes
SCL clock frequency	f _{I2C}	0	400	kHz	—
Low period of the SCL clock	t _{I2CL}	1.3	—	μs	—
High period of the SCL clock	t _{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t _{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	—	μs	—
Data setup time	t _{I2DVKH}	100	—	ns	—
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	— 0	— —	μs	2
Data output delay time	t _{I2OVKL}	—	0.9		3
Set-up time for STOP condition	t _{I2PVKH}	0.6	—	μs	—
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _b	300	ns	4
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b	300	ns	4
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	0.1 × OV _{DD}	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	0.2 × OV _{DD}	—	V	—

Notes:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- The MPC8544E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- C_B = capacitance of one bus line in pF.

15.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. Table 56 provides the PCI AC timing specifications at 66 MHz.

Table 56. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	—	7.4	ns	2, 3
Output hold from SYSCLK	t_{PCKHOX}	2.0	—	ns	2
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4
Input setup to SYSCLK	t_{PCIVKH}	3.7	—	ns	2, 5
Input hold from SYSCLK	t_{PCIXKH}	0.5	—	ns	2, 5
$\overline{REQ64}$ to \overline{HRESET} ⁹ setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	6, 7
\overline{HRESET} to $\overline{REQ64}$ hold time	t_{PCRHRX}	0	50	ns	7
\overline{HRESET} high to first \overline{FRAME} assertion	t_{PCRHFV}	10	—	clocks	8
Rise time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—
Fall time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
- All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Input timings are measured at the pin.
- The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 19, “Clocking.”
- The setup and hold time is with respect to the rising edge of \overline{HRESET} .
- The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
- The reset assertion timing requirement for \overline{HRESET} is 100 μs .

Figure 41 provides the AC test load for PCI.

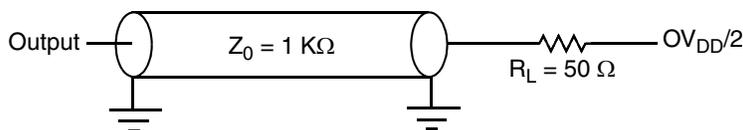


Figure 41. PCI AC Test Load

- For **external DC-coupled** connection, as described in Section 16.2.1, “SerDes Reference Clock Receiver Characteristics,” the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 46 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
 - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDSn. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDSn). Figure 47 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
 - The reference clock can also be single-ended. The SDn_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-peak (from Vmin to Vmax) with SDn_REF_CLK either left unconnected or tied to ground.
 - The SDn_REF_CLK input average voltage must be between 200 and 400 mV. Figure 48 shows the SerDes reference clock input requirement for single-ended signaling mode.
 - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase (SDn_REF_CLK) through the same source impedance as the clock input (SDn_REF_CLK) in use.

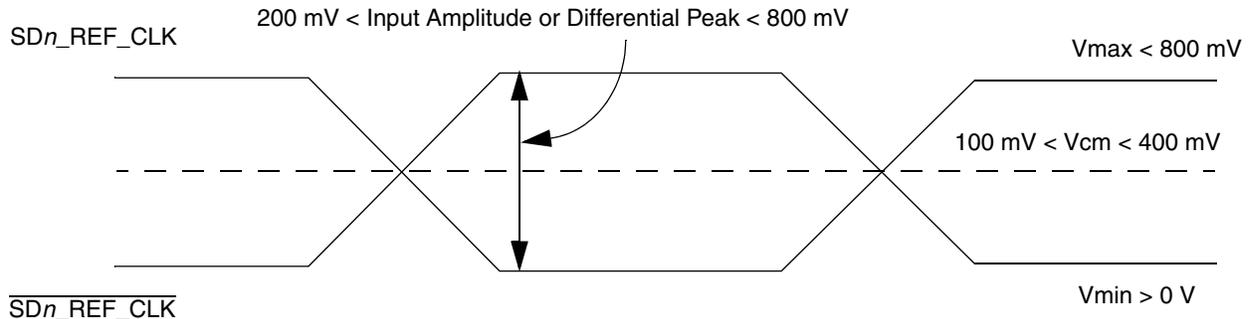


Figure 46. Differential Reference Clock Input DC Requirements (External DC-Coupled)

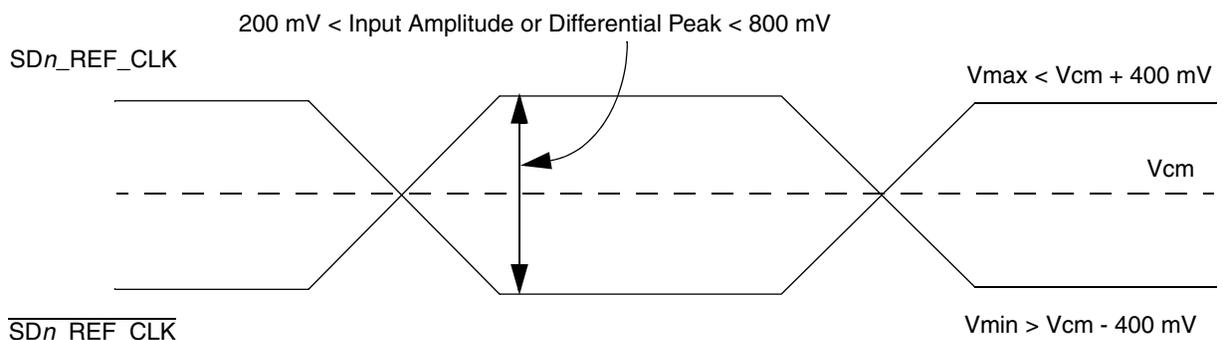


Figure 47. Differential Reference Clock Input DC Requirements (External AC-Coupled)

Table 59. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$T_{\text{crosslink}}$	Crosslink random timeout	0	—	1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in [Figure 58](#) and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in [Figure 56](#).)
3. A $T_{\text{TX-EYE}} = 0.70$ UI provides for a total sum of deterministic and random jitter budget of $T_{\text{TX-JITTER-MAX}} = 0.30$ UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{\text{TX-EYE-MEDIAN-to-MAX-JITTER}}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a vector network analyzer with 50- Ω probes—see [Figure 58](#).) Note that the series capacitors C_{TX} is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in [Figure 58](#) for both $V_{\text{TX-D+}}$ and $V_{\text{TX-D-}}$.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications, Rev 1.0a*.
7. See Section 4.2.6.3 of the *PCI Express Base Specifications, Rev 1.0a*.

17.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in [Figure 56](#) is specified using the passive compliance/test measurement load (see [Figure 58](#)) in place of any real PCI Express interconnect +RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

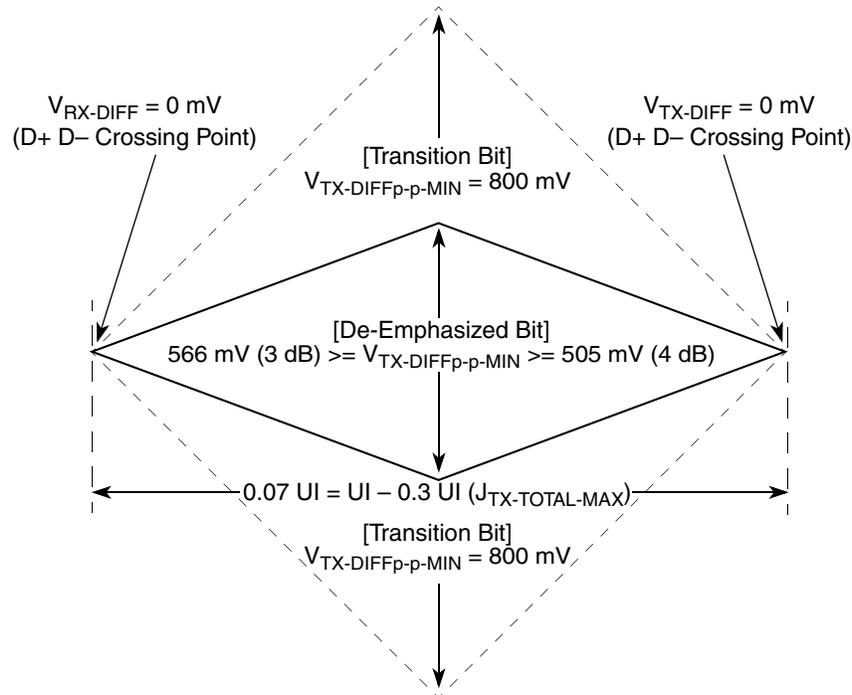


Figure 56. Minimum Transmitter Timing and Voltage Output Compliance Specifications

17.4.3 Differential Receiver (RX) Input Specifications

Table 60 defines the specifications for the differential input at all receivers. The parameters are specified at the component pins.

Table 60. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps \pm 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ See Note 2.
T_{RX-EYE}	Minimum receiver eye width	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6 UI$. See Notes 2 and 3.

19.6.2 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed. Refer to [Section 4.4, “Platform to FIFO Restrictions,”](#) for additional information.

Table 69. FIFO Maximum Speed Restrictions

Platform Speed (MHz)	Maximum FIFO Speed for Reference Clocks TSEC _n _TX_CLK, TSEC _n _RX_CLK (MHz) ¹
533	126
400	94

Note:

1. FIFO speed should be less than 24% of the platform speed.

20 Thermal

This section describes the thermal specifications of the MPC8544E.

20.1 Thermal Characteristics

[Table 70](#) provides the package thermal characteristics.

Table 70. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single layer board (1s)	R _{θJA}	26	°C/W	1, 2
Junction-to-ambient natural convection	Four layer board (2s2p)	R _{θJA}	21	°C/W	1, 2
Junction-to-ambient (@200 ft/min)	Single layer board (1s)	R _{θJA}	21	°C/W	1, 2
Junction-to-ambient (@200 ft/min)	Four layer board (2s2p)	R _{θJA}	17	°C/W	1, 2
Junction-to-board thermal	—	R _{θJB}	12	°C/W	3
Junction-to-case thermal	—	R _{θJC}	<0.1	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1°C/W.

Table 71 provides the thermal resistance with heat sink in open flow.

Table 71. Thermal Resistance with Heat Sink in Open Flow

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance (°C/W)
Wakefield 53 × 53 × 25 mm pin fin	Natural convection	6.1
Wakefield 53 × 53 × 25 mm pin fin	1 m/s	3.0
Aavid 35 × 31 × 23 mm pin fin	Natural convection	8.1
Aavid 35 × 31 × 23 mm pin fin	1 m/s	4.3
Aavid 30 × 30 × 9.4 mm pin fin	Natural convection	11.6
Aavid 30 × 30 × 9.4 mm pin fin	1 m/s	6.7
Aavid 43 × 41 × 16.5 mm pin fin	Natural convection	8.3
Aavid 43 × 41 × 16.5 mm pin fin	1 m/s	4.3

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease. For system thermal modeling, the MPC8544E thermal model without a lid is shown in Figure 60. The substrate is modeled as a block 29 × 29 × 1.18 mm with an in-plane conductivity of 18.0 W/m•K and a through-plane conductivity of 1.0 W/m•K. The solder balls and air are modeled as a single block 29 × 29 × 0.58 mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 7.6 × 8.4 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 6.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to Figure 59 for actual dimensions.

20.2 Recommended Thermal Model

Table 72 shows the MPC8544E thermal model.

Table 72. MPC8544E Thermal Model

Conductivity	Value	Units
Die (7.6 × 8.4 × 0.75mm)		
Silicon	Temperature dependent	—
Bump/Underfill (7.6 × 8.4 × 0.070 mm) Collapsed Thermal Resistance		
Kz	6.5	W/m•K
Substrate (29 × 29 × 1.18 mm)		
Kx	18	W/m•K
Ky	18	
Kz	1.0	

Table 72. MPC8544E Thermal Model (continued)

Conductivity	Value	Units
Solder and Air (29 × 29 × 0.58 mm)		
Kx	0.034	W/m•K
Ky	0.034	
Kz	12.1	

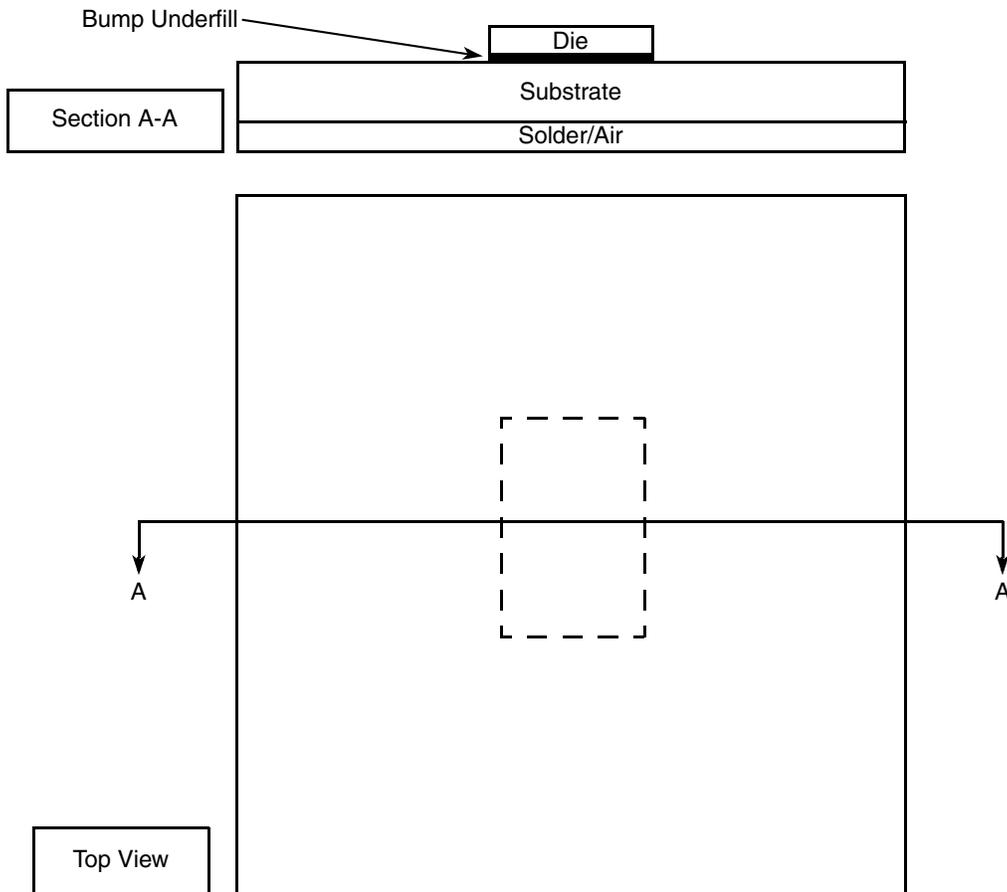


Figure 60. System Level Thermal Model for MPC8544E (Not to Scale)

The Flotherm library files of the parts have a dense grid to accurately capture the laminar boundary layer for flow over the part in standard JEDEC environments, as well as the heat spreading in the board under the package. In a real system, however, the part will require a heat sink to be mounted on it. In this case, the predominant heat flow path will be from the die to the heat sink. Grid density lower than currently in the package library file will suffice for these simulations. The user will need to determine the optimal grid for their specific case.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 61). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

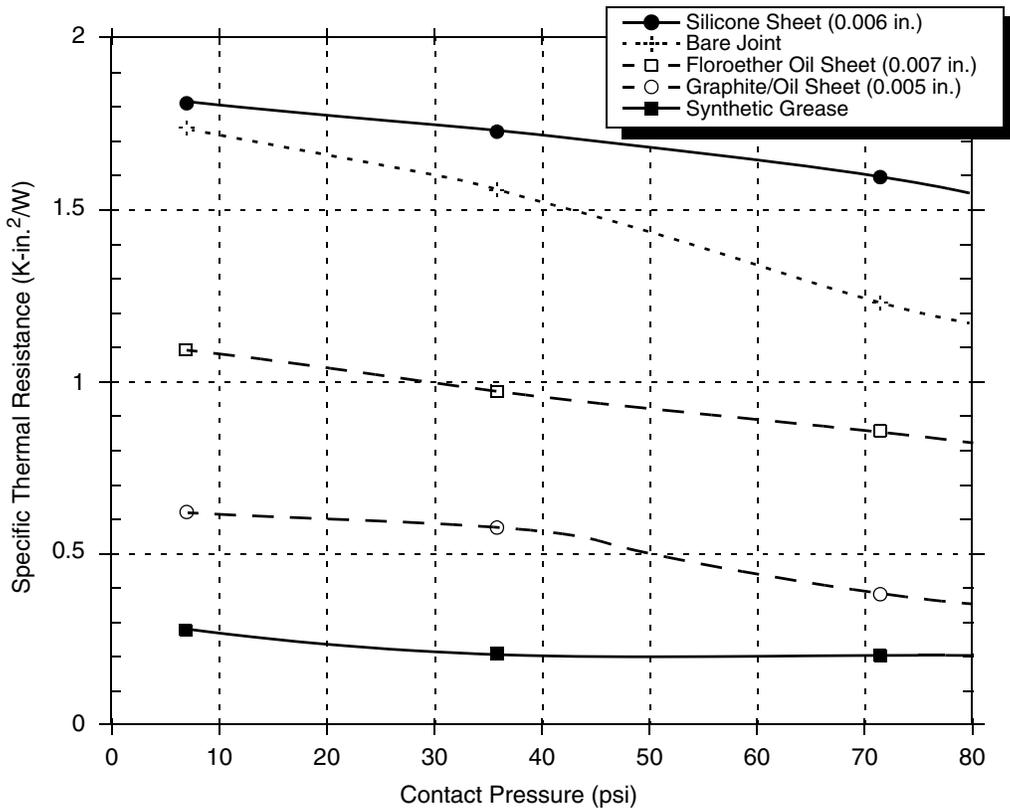


Figure 63. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 781-935-4850
 77 Dragon Ct.
 Woburn, MA 01801
 Internet: www.chomerics.com

Dow-Corning Corporation 800-248-2481
 Corporate Center
 P.O.Box 999
 Midland, MI 48686-0997
 Internet: www.dow.com

Shin-Etsu MicroSi, Inc. 888-642-7674
 10028 S. 51st St.
 Phoenix, AZ 85044
 Internet: www.microsi.com

The Bergquist Company 800-347-4572
 18930 West 78th St.

21.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} , and GND pins of the device.

21.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8544E requires weak pull-up resistors (2–10 k Ω is recommended) on open drain type pins including I²C pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 69](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

The following pins must NOT be pulled down during power-on reset: TSEC3_TXD[3], $\overline{\text{HRESET_REQ}}$, TRIG_OUT/READY/ $\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP. The $\overline{\text{DMA_DACK}}[0:1]$ and $\overline{\text{TEST_SEL}}$ pins must be set to a proper state during POR configuration. Refer to the pinout listing table ([Table 62](#)) for more details. Refer to the *PCI 2.2 Local Bus Specifications*, for all pullups required for PCI.

21.7 Output Buffer DC Impedance

The MPC8544E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I²C). To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see [Figure 67](#)). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_p is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_p then becomes the

23 Document Revision History

This table provides a revision history for the MPC8544E hardware specification.

Table 76. MPC8544E Document Revision History

Revision	Date	Substantive Change(s)
8	09/2015	<ul style="list-style-type: none"> In Table 10 and Table 12, removed the output leakage current rows and removed table note 4.
7	06/2014	<ul style="list-style-type: none"> In Table 75, “Device Nomenclature,” added full Pb-free part code. In Table 75, “Device Nomenclature,” added footnotes 3 and 4.
6	05/2011	<ul style="list-style-type: none"> Updated the value of t_{JTKLDX} to 2.5 ns from 4ns in Table 50.
5	01/2011	<ul style="list-style-type: none"> Updated Table 75.
4	09/2010	<ul style="list-style-type: none"> Modified local bus information in Section 1.1, “Key Features,” to show max local bus frequency as 133 MHz. Added footnote 28 to Table 62. Updated solder-ball parameter in Table 61.
3	11/2009	<ul style="list-style-type: none"> Update Section 20.3.4, “Temperature Diode,” Update Table 61 Package Parameters from 95.5%sn to 96.5%sn
2	01/2009	<ul style="list-style-type: none"> Update power number table to include 1067 MHz/533 MHz power numbers. Remove Part number tables from Hardware spec. The part numbers are available on Freescale web site product page. Removed I/O power numbers from the Hardware spec. and added the table to bring-up guide application note. Update t_{DDKHMP}, t_{DDKHME} in Table 18. Updated RX_CLK duty cycle min, and max value to meet the industry standard GMII duty cycle. Update paragraph Section 21.3, “Decoupling Recommendations.” Update Figure 5 DDR Output Timing Diagram. In Table 40, removed note 1 and renumbered remaining note. Update Section 22, “Device Nomenclature,” with regards to Commercial Tier.
1	06/2008	Update in Table 18 DDR SDRAM Output AC Timing Specifications tMCK Max value Improvement to Section 16 , “High-Speed Serial Interfaces (HSSI) Update Figure 59 Mechanical Dimensions Update in Table 48 Local Bus General Timing Parameters—PLL Bypassed
0	04/2008	Initial release.