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Understanding Embedded - Microprocessors

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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544ecvjalfa

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



MPC8544E Overview

- Broadcast address (accept/reject)
- Hash table match on up to 512 multicast addresses
- Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache
- OCeaN switch fabric
 - Full crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
 - Four-channel controller
 - All channels accessible by both the local and remote masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Support for scatter and gather transfers
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no snoop)
 - Ability to start and flow control each DMA channel from external 3-pin interface
 - Ability to launch DMA from single write transaction
- PCI controller
 - PCI 2.2 compatible
 - One 32-bit PCI port with support for speeds from 16 to 66 MHz
 - Host and agent mode support
 - 64-bit dual address cycle (DAC) support
 - Supports PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses
 - Supports posting of processor-to-PCI and PCI-to-memory writes
 - PCI 3.3-V compatible
 - Selectable hardware-enforced coherency



Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8544E.



Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}/LV_{DD}/BV_{DD}/TV_{DD}

The core voltage must always be provided at nominal 1.0 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.



Input Clocks

4.1 System Clock Timing

Table 5 provides the system clock (SYSCLK) AC timing specifications for the MPC8544E.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with $OV_{DD} = 3.3 V \pm 165 mV$.

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
SYSCLK frequency	f _{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t _{SYSCLK}	7.5	—	30.3	ns	_
SYSCLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	2.1	ns	2
SYSCLK duty cycle	t _{KHK} /t _{SYSCLK}	40	—	60	%	_
SYSCLK jitter	_	—	—	±150	ps	3, 4

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.

2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.

3. This represents the total input jitter-short- and long-term.

4. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 5 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC8544E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8544E is compatible with spread spectrum sources if the recommendations listed in Table 6 are observed.

Table 6. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Мах	Unit	Notes
Frequency modulation	20	60	kHz	—
Frequency spread	0	1.0	%	1

Note:

1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 5.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.



6.1 DDR SDRAM DC Electrical Characteristics

Table 10 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8544E when $GV_{DD}(typ) = 1.8 V_{.}$

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV _{DD}	1.71	1.89	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.26	GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.24	V	_
Output high current (V _{OUT} = 1.26 V)	I _{OH}	-13.4	_	mA	_
Output low current (V _{OUT} = 0.33 V)	I _{OL}	13.4	_	mA	_

Table 10. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} , and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

Table 11 provides the DDR2 I/O capacitance when $GV_{DD}(typ) = 1.8 V$.

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, \overline{DQS}	C _{DIO}	_	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 12 provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}(typ) = 2.5 \text{ V}.$

Table 12. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.31	GV _{DD} + 0.3	V	
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.3	V	
Output high current (V _{OUT} = 1.8 V)	I _{OH}	-16.2	—	mA	



DDR and DDR2 SDRAM

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 18 provides the output AC timing specifications for the DDR SDRAM interface.

Table 18. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, MCK[n]/MCK[n] crossing	t _{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK	t _{DDKHAS}			ns	3
533 MHz 400 MHz 333 MHz		1.48 1.95 2.40			7
ADDR/CMD output hold with respect to MCK	t _{DDKHAX}			ns	3
533 MHz 400 MHz 333 MHz		1.48 1.95 2.40			7
MCS[n] output setup with respect to MCK	t _{DDKHCS}			ns	3
533 MHz 400 MHz 333 MHz		1.48 1.95 2.40			7
MCS[n] output hold with respect to MCK	t _{DDKHCX}			ns	3
533 MHz 400 MHz 333 MHz		1.48 1.95 2.40			7
MCK to MDQS Skew	t _{DDKHMH}	-0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	^t DDKHDS, t _{DDKLDS}			ps	5
533 MHz 400 MHz 333 MHz		538 700 900			7
MDQ/MECC/MDM output hold with respect to MDQS	t _{DDKHDX,} t _{DDKLDX}			ps	5
533 MHz 400 MHz 333 MHz		538 700 900			7 — —
MDQS preamble	t _{DDKHMP}	0.75 x tMCK	—	ns	6



Enhanced Three-Speed Ethernet (eTSEC), MII Management

Parameter		Symbol	Min	Тур	Max	Unit	Notes
Input differential voltage	LSTS = 0	V _{rx_diffpp}	100	—	1200	mV	2, 4
	LSTS = 1	1	175	—			
Loss of signal threshold	LSTS = 0	VI _{os}	30	—	100	mV	3, 4
	LSTS = 1	1	65	—	175		
Input AC common mode voltage		V _{cm_acpp}	—	—	100	mV	5.
Receiver differential input impedar	ice	Zrx_diff	80	—	120	Ω	
Receiver common mode input impedance		Zrx_cm	20	—	35	Ω	—
Common mode input voltage		Vcm	xcorevss	—	xcorevss	V	6

Table 25. DC Receiver Electrical Characteristics (continued)

Notes:

1. Input must be externally AC-coupled.

- 2. $V_{RX_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage
- 3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to Section 17.4.3, "Differential Receiver (RX) Input Specifications," for further explanation.
- 4. The LSTS shown in this table refers to the LSTSCD bit field of MPC8544E SerDes 2 control register 1.
- 5. V_{CM ACp-p} is also referred to as peak-to-peak AC common mode voltage.
- 6. On-chip termination to SGND_SRDS2 (xcorevss).

8.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs ($SD2_TX[n]$ and $\overline{SD2_TX[n]}$) or at the receiver inputs ($SD2_RX[n]$ and $\overline{SD2_RX[n]}$) as depicted in Figure 10, respectively.

8.4.1 SGMII Transmit AC Timing Specifications

Table 26 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 26. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XVDD_SRDS2 = $1.0 V \pm 5\%$.

Parameter	Symbol	Min	Тур	Мах	Unit	Notes
Deterministic jitter	J _D	—	—	0.17	UI p-p	—
Total jitter	J _T	—	—	0.35	UI p-p	—
Unit interval	UI	799.92	800	800.08	ps	2
V _{OD} fall time (80%–20%)	t _{fall}	50	—	120	ps	—
V _{OD} rise time (20%–80%)	t _{rise}	50	—	120	ps	—

Notes;

1. Source synchronous clock is not supported.

2. Each UI value is 800 ps \pm 100 ppm.



Enhanced Three-Speed Ethernet (eTSEC), MII Management

Table 28. FIFO Mode Transmit AC Timing Specification (continued)

(continued)At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol	Min	Тур	Max	Unit	Notes
Fall time TX_CLK (80%–20%)	t _{FITF}	_	—	0.75	ns	—
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t _{FITDX}	0.5	—	3.0	ns	1

Note:

1. Data valid $t_{\ensuremath{\mathsf{FITDV}}}$ to GTX_CLK Min setup time is a function of clock period and max hold time.

(Min setup = Cycle time - Max hold).

Table 29. FIFO Mode Receive AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
RX_CLK clock period	t _{FIR}	—	8.0	—	ns	—
RX_CLK duty cycle	t _{FIRH} /t _{FIRH}	45	50	55	%	—
RX_CLK peak-to-peak jitter	t _{FIRJ}	—	—	250	ps	—
Rise time RX_CLK (20%–80%)	t _{FIRR}	—	—	0.75	ns	—
Fall time RX_CLK (80%-20%)	t _{FIRF}	—	—	0.75	ns	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{FIRDV}	1.5	—	—	ns	—
RX_CLK to RXD[7:0], RX_DV, RX_ER hold time	t _{FIRDX}	0.5	—	—	ns	—

Timing diagrams for FIFO appear in Figure 11 and Figure 12.



Figure 12. FIFO Receive AC Timing Diagram



Ethernet Management Interface Electrical Characteristics

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in "Section 8, "Enhanced Three-Speed Ethernet (eTSEC), MII Management."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 40.

Parameter	Symbol	Min	Мах	Unit	Notes
Supply voltage (3.3 V)	OV _{DD}	3.135	3.465	V	_
Output high voltage ($OV_{DD} = Min, I_{OH} = -1.0 mA$)	V _{OH}	2.10	3.60	V	
Output low voltage (OV _{DD} = Min, I _{OL} = 1.0 mA)	V _{OL}	GND	0.50	V	
Input high voltage	V _{IH}	1.95	_	V	_
Input low voltage	V _{IL}	_	0.90	V	
Input high current (OV _{DD} = Max, V _{IN} = 2.1 V)	I _{IH}	_	40	μA	1
Input low current (OV _{DD} = Max, V_{IN} = 0.5 V)	IIL	-600		μA	_

Table 40. MII Management DC Electrical Characteristics

Note:

1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

Table 41 provides the MII management AC timing specifications.

Table 41. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	—	2.5	—	MHz	2
MDC period	t _{MDC}	—	400	—	ns	—
MDC clock pulse width high	t _{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t _{MDKHDX}	$(16 \times t_{plb_clk}) - 3$	—	$(16 \times t_{plb_clk}) + 3$	ns	3, 4
MDIO to MDC setup time	t _{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t _{MDDXKH}	0	—	—	ns	—
MDC rise time	t _{MDCR}	—	—	10	ns	—



JTAG

12 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8544E.

12.1 JTAG DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the JTAG interface.

Table 49. JTAG DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	
Low-level input voltage	V _{IL}	-0.3	0.8	V	
Input current (OV _{IN} = 0 V or OV _{IN} = OV _{DD})	I _{IN}	—	±5	μA	1
High-level output voltage ($OV_{DD} = min, I_{OH} = -2 mA$)	V _{OH}	2.4	—	V	_
Low-level output voltage ($OV_{DD} = min, I_{OL} = 2 mA$)	V _{OL}	—	0.4	V	_

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} .

12.2 JTAG AC Electrical Specifications

Table 50 provides the JTAG AC timing specifications as defined in Figure 34 through Figure 37.

Table 50. JTAG AC Timing Specifications (Independent of SYSCLK)¹

At recommended operating conditions (see Table 3).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f _{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t _{JTG}	30	_	ns	—
JTAG external clock pulse width measured at 1.4 V	t _{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t _{JTGR} & t _{JTGF}	0	2	ns	—
TRST assert time	t _{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t _{JTDVKH} t _{JTIVKH}	4 0		ns	4
Input hold times: Boundary-scan data TMS, TDI	t _{JTDXKH} t _{JTIXKH}	20 25	_	ns	4
Valid times: Boundary-scan data TDO	t _{JTKLDV} t _{JTKLOV}	4 4	20 25	ns	5
Output hold times: Boundary-scan data TDO	t _{jtkldx} t _{jtklox}	2.5 4		ns	5



Figure 38 provides the AC test load for the I^2C .



Figure 38. I²C AC Test Load

Figure 39 shows the AC timing diagram for the I^2C bus.



Figure 39. I²C Bus AC Timing Diagram

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8544E.

14.1 GPIO DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the GPIO interface.

Table 53. GPIO DO	Electrical	Characteristics
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Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage	V _{IL}	-0.3	0.8	V	—
Input current ($V_{IN} = 0 V \text{ or } V_{IN} = V_{DD}$)	I _{IN}	—	±5	μA	1
High-level output voltage ($OV_{DD} = mn, I_{OH} = -2 mA$)	V _{OH}	2.4	—	V	—
Low-level output voltage ($OV_{DD} = min, I_{OL} = 2 mA$)	V _{OL}	—	0.4	V	

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

High-Speed Serial Interfaces (HSSI)

- The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range:
 - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
 - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
 - If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n}_{\text{REF}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
 - This requirement is described in detail in the following sections.



Figure 45. Receiver of SerDes Reference Clocks

16.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8544E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- Differential Mode
 - The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.



Figure 49 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8544E SerDes reference clock input's DC requirement.



Figure 49. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 50 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8544E SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features $50-\Omega$ termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.



Figure 50. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 51 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8544E SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 51



16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 57 describes some AC parameters common to SGMII, and PCI Express protocols.

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V _{IH}	+200	_	mV	2
Differential Input Low Voltage	V _{IL}	_	-200	mV	2
Rising edge rate (SD <i>n</i> _REF_CLK) to falling edge rate (SD <i>n</i> _REF_CLK) matching	Rise-Fall Matching	_	20	%	1, 4

Table 57. SerDes Reference Clock Common AC Parameters

Notes:

- 1. Measurement taken from single ended waveform.
- 2. Measurement taken from differential waveform.
- 3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus SD*n*_REF_CLK). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 53.
- 4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for SDn_REF_CLK. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets SDn_REF_CLK falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SDn_REF_CLK should be compared to the fall edge rate of SDn_REF_CLK, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 54.



Figure 53. Differential Measurement Points for Rise and Fall Time



Table 59. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
T _{crosslink}	Crosslink random timeout	0		1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 58 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 56.)
- 3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of T_{TX-JITTER-MAX} = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The T_{TX-EYE-MEDIAN-to-MAX-JITTER} median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- 4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 58.) Note that the series capacitors C_{TX} is optional for the return loss measurement.
- 5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 58 for both V_{TX-D+} and V_{TX-D-} .
- 6. See Section 4.3.1.8 of the PCI Express Base Specifications, Rev 1.0a.
- 7. See Section 4.2.6.3 of the PCI Express Base Specifications, Rev 1.0a.

17.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 56 is specified using the passive compliance/test measurement load (see Figure 58) in place of any real PCI Express interconnect +RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).



Package Description

18.2 Mechanical Dimensions of the MPC8544E FC-PBGA

Figure 59 shows the mechanical dimensions and bottom surface nomenclature of the MPC8544E, 783 FC-PBGA package without a lid.



Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensions and tolerances per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 5. Parallelism measurement shall exclude any effect of mark on top surface of package.
- 6. Capacitors may not be present on all parts. Care must be taken not to short exposed metal capacitor pads.
- 7. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

Figure 59. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8544E FC-PBGA without a Lid



Package Description

Table 62. MPC8544E Pinout Listing (continued)

		(,		
Signal	Package Pin Number	Pin Type	Power Supply	Notes
6.The value of LA[28:31] du resistors. See Section 1	ring reset sets the CCB clock to SYSCLK PLL ration 9.2. "CCB/SYSCLK PLL Ratio."	o. These pins requ	ire 4.7-k Ω pull-up (or pull-down

- 7.The value of LALE, LGPL2, and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 19.3, "e500 Core PLL Ratio."
- 8. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. Therefore, this pin will be described as an I/O for boundary scan.
- 9. For proper state of these signals during reset, DMA_DACK[1] must be pulled down to GND through a resistor. DMA_DACK[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on DMA_DACK[0].
- 10. This output is actively driven during reset rather than being three-stated during reset.
- 11. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 12. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
- 13. Anode and cathode of internal thermal diode.
- 14.Treat pins AC7, T5, V2, and M7 as spare configuration pins cfg_spare[0:3]. The spare pins are unused POR config pins. It is highly recommended that the customer provide the capability of setting these pins low (that is, pull-down resistor which is not currently stuffed) in order to support new config options should they arise between revisions.
- 15.If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
- 16. This pin is only an output in FIFO mode when used as Rx flow control.

17.Do not connect.

18. These are test signals for factory use only and must be pulled up (100 Ω to 1 k Ω) to OV_{DD} for normal machine operation.

- 19.Independent supplies derived from board $\ensuremath{\mathsf{V}_{\text{DD}}}$.
- 20.Recommend a pull-up resistor (1 K~) be placed on this pin to OV_{DD} .
- 21. The following pins must not be pulled down during power-on reset: HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], and ASLEEP.
- 22. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven.
- 23.General-purpose POR configuration of user system.
- 24.When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the address pins as No Connect or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the address pins are not connected to any other PCI device. The PCI block will drive the address pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
- 25.MDIC0 is grounded through an 18.2-Ω precision 1% resistor and MDIC1 is connected GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
- 26.For SGMII mode.

27.Connect to GND.

28. For systems that boot from a local bus (GPCM)-controlled flash, a pull-up on LGPL4 is required.



Clocking

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the CCB bus frequency, since the CCB frequency must equal the DDR data rate.

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	16:1	1000	8:1
0001	Reserved	1001	9:1
0010	0010 Reserved		10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1
0101	5:1	1101	Reserved
0110	0110 6:1 1*		Reserved
0111	Reserved	1111	Reserved

Table	65.	ССВ	Clock	Ratio
Table	00.	000	Olock	nauo

19.3 e500 Core PLL Ratio

Table 66 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE, and LGPL2 at power up, as shown in Table 66.

Table 6	6. e500	Core to	ССВ	Clock Ratio
	0.0000			

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	
000	4:1	100	2:1	
001	Reserved	101	5:2	
010	Reserved	110	3:1	
011	3:2	111	7:2	

19.4 PCI Clocks

For specifications on the PCI_CLK, refer to the PCI 2.2 Local Bus Specifications.

The use of PCI_CLK is optional if SYSCLK is in the range of 33–66 MHz. If SYSCLK is outside this range then use of PCI_CLK is required as a separate PCI clock source, asynchronous with respect to SYSCLK.



Device Nomenclature

Option 2

- If PCI arbiter is disabled during POR,
- All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-k Ω resistor(s).
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-k Ω resistor.

21.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following list shows the termination recommendation:

- For LDP[0:3]: tie them to ground or the power supply rail via a 4.7-k Ω resistor.
- For LPBSE: tie it to the power supply rail via a 4.7-k Ω resistor (pull-up resistor).

22 Device Nomenclature

Ordering information for the parts fully covered by this hardware specifications document is provided in Section 22.3, "Part Marking." Contact your local Freescale sales office or regional marketing team for order information.

22.1 Industrial and Commercial Tier Qualification

The MPC8544E device has been tested to meet the industrial tier qualification. Table 74 provides a description for commercial and industrial qualifications.

Tier ¹	Typical Application Use Time	Power-On Hours	Example of Typical Applications
Commercial	5 years	Part-time/ Full-Time	PC's, consumer electronics, office automation, SOHO networking, portable telecom products, PDAs, etc.
Industrial	10 years	Typically Full-Time	Installed telecom equipment, work stations, servers, warehouse equipment, etc.

Table 74. Commercial and Industrial Description

Note:

1. Refer to Table 2 for operating temperature ranges. Temperature is independent of tier and varies per product.



22.2 Nomenclature of Parts Fully Addressed by this Document

Table 75 provides the Freescale part numbering nomenclature for the MPC8544E.

Table 75. Device Nomenclature

MPC	nnnn	Ε	С	НХ	AA	X	В
Product Code	Part Identifier	Encryption Acceleration	Temperature Range	Package ¹	Processor Frequency ²	Platform Frequency	Revision Level
MPC	8544	Blank = not included E = included	B or Blank = Industrial Tier standard temp range(0° to 105°C) C = Industrial Tier Extended temp range(-40° to 105°C)	VT = FC-PBGA (lead-free) VJ = lead-free FC-PBGA	AL = 667 MHz AN = 800 MHz AQ = 1000 MHz AR = 1067 MHz	F = 333 MHz G = 400 MHz J = 533 MHz	Blank = Rev. 1.1 1.1.1 A = Rev. 2.1

Notes:

- 1. See Section 18, "Package Description," for more information on available package types.
- Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
- 3. The VT part number is ROHS-compliant, with the permitted exception of the C4 die bumps.
- 4. The VJ part number is entirely lead-free. This includes the C4 die bumps.

22.3 Part Marking

Parts are marked as in the example shown in Figure 70.



Notes:

MMMMM is the 5-digit mask number.

ATWLYYWW is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 70. Part Marking for FC-PBGA Device



Document Revision History

23 Document Revision History

This table provides a revision history for the MPC8544E hardware specification.

Revision Date Substantive Change(s) 8 09/2015 • In Table 10 and Table 12, removed the output leakage current rows and removed table note 4. 7 06/2014 • In Table 75, "Device Nomenclature," added full Pb-free part code. • In Table 75, "Device Nomenclature," added footnotes 3 and 4. 05/2011 6 Updated the value of t_{JTKLDX} to 2.5 ns from 4ns in Table 50. 5 01/2011 • Updated Table 75. 4 09/2010 • Modified local bus information in Section 1.1, "Key Features," to show max local bus frequency as 133 MHz. Added footnote 28 to Table 62. • Updated solder-ball parameter in Table 61. 11/2009 • Update Section 20.3.4, "Temperature Diode," 3 • Update Table 61 Package Parameters from 95.5%sn to 96.5%sn 2 01/2009 • Update power number table to include 1067 MHz/533 MHz power numbers. Remove Part number tables from Hardware spec. The part numbers are available on Freescale web site product page. Removed I/O power numbers from the Hardware spec. and added the table to bring-up guide application note. • Update t_{DDKHMP}, t_{DDKHME} in Table 18. • Updated RX_CLK duty cycle min, and max value to meet the industry standard GMII duty cycle.

• Update paragraph Section 21.3, "Decoupling Recommendations."

• Update Section 22, "Device Nomenclature," with regards to Commercial Tier.

Update in Table 48 Local Bus General Timing Parameters—PLL Bypassed

Update in Table 18 DDR SDRAM Output AC Timing Specifications tMCK Max value

• In Table 40, removed note 1 and renumbered remaining note.

Improvement to Section 16, "High-Speed Serial Interfaces (HSSI)

• Update Figure 5 DDR Output Timing Diagram.

Update Figure 59 Mechanical Dimensions

Table 76. MPC8544E Document Revision History

1

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06/2008

04/2008

Initial release.