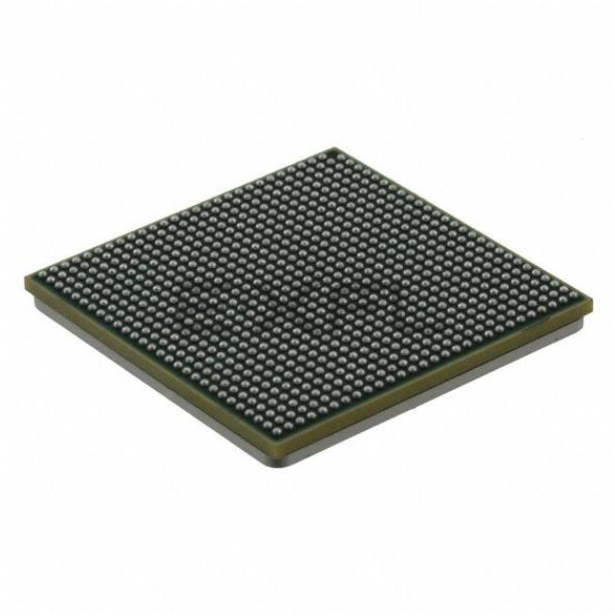

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544ecvjanga

Table 28. FIFO Mode Transmit AC Timing Specification (continued)

(continued)At recommended operating conditions with L/TVDD of 3.3 V – 5% or 2.5 V – 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
Fall time TX_CLK (80% 20%)	t_{FITF}			0.75	ns	
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5		3.0	ns	1

Note:

1. Data valid t_{FITDV} to GTX_CLK Min setup time is a function of clock period and max hold time. (Min setup = Cycle time Max hold).

Table 29. FIFO Mode Receive AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V – 5% or 2.5 V – 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
RX_CLK clock period	t_{FIR}		8.0		ns	
RX_CLK duty cycle	t_{FIRH}/t_{FIRH}	45	50	55	%	
RX_CLK peak-to-peak jitter	t_{FIRJ}			250	ps	
Rise time RX_CLK (20% 80%)	t_{FIRR}			0.75	ns	
Fall time RX_CLK (80% 20%)	t_{FIRF}			0.75	ns	
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5			ns	
RX_CLK to RXD[7:0], RX_DV, RX_ER hold time	t_{FIRDX}	0.5			ns	

Timing diagrams for FIFO appear in Figure 11 and Figure 12.

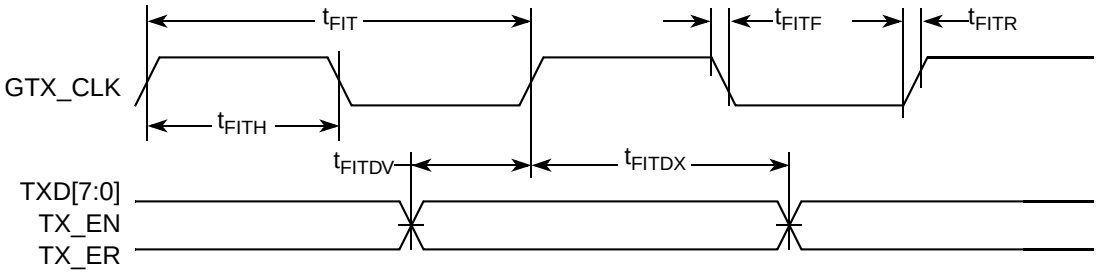

Figure 11. FIFO Transmit AC Timing Diagram

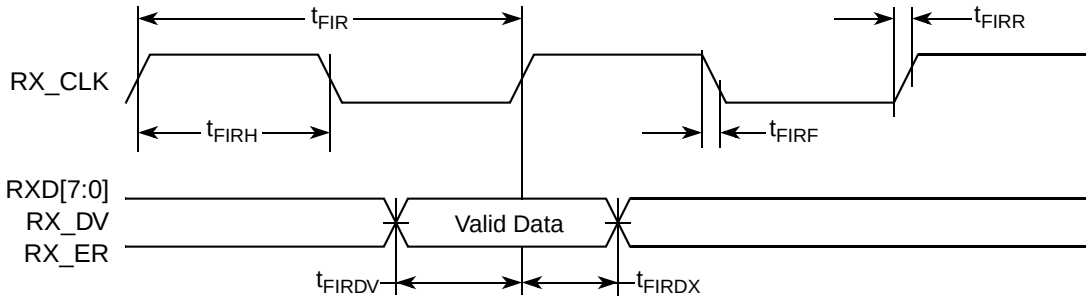

Figure 12. FIFO Receive AC Timing Diagram

— For **external DC-coupled** connection, as described in Section 16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 46 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS*n*. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS*n*). Figure 47 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- **Single-ended Mode**
  — The reference clock can also be single-ended. The SD*n*_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD}n\text{_REF_CLK}}$ either left unconnected or tied to ground.
  — The SD*n*_REF_CLK input average voltage must be between 200 and 400 mV. Figure 48 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD}n\text{_REF_CLK}}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

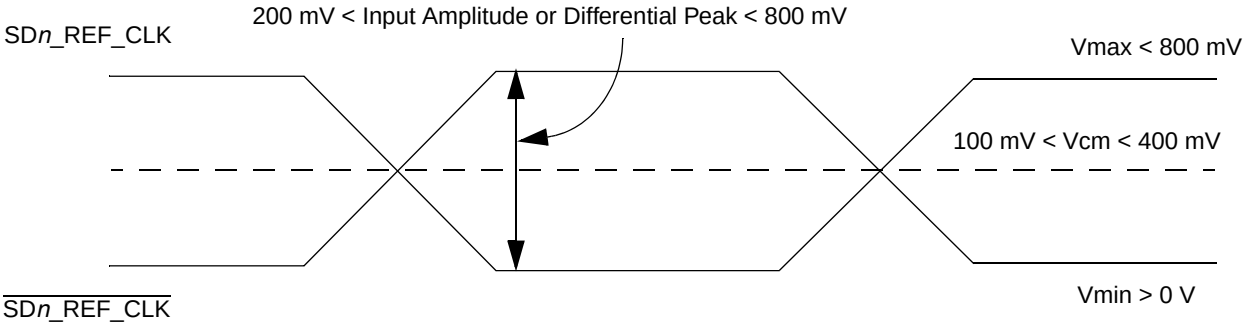

Figure 46. Differential Reference Clock Input DC Requirements (External DC-Coupled)

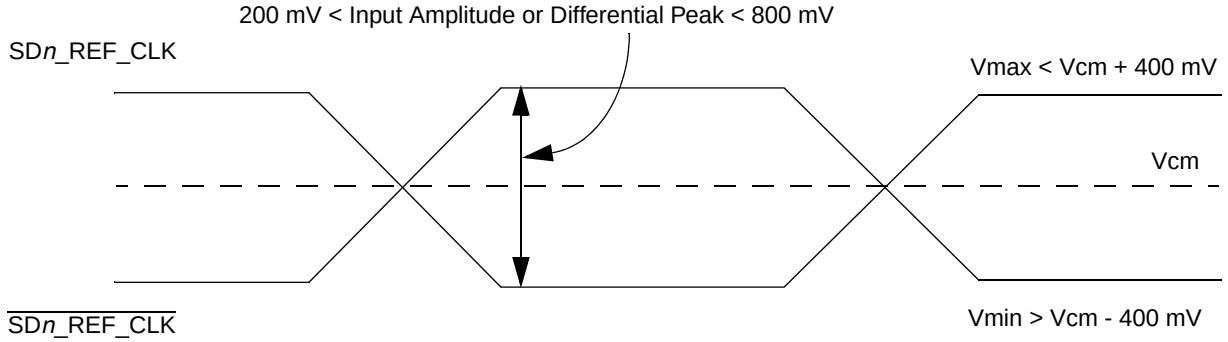

Figure 47. Differential Reference Clock Input DC Requirements (External AC-Coupled)

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
AVDD_SRDS	W28	Power for SRDSPLL (1.0 V)		19
AVDD_SRDS2	AG1	Power for SRDSPLL (1.0 V)		19
SENSEVDD	W11	O	V_{DD}	12
SENSEVSS	W10			12
Analog Signals				
MVREF	A28	Reference voltage signal for DDR	MVREF	
SD1_IMP_CAL_RX	M26		200 Ω to GND	
SD1_IMP_CAL_TX	AE28		100 Ω to GND	
SD1_PLL_TPA	V26		AVDD_SRDS ANALOG	17
SD2_IMP_CAL_RX	AH3	I	200 Ω to GND	
SD2_IMP_CAL_TX	Y1	I	100 Ω to GND	
SD2_PLL_TPA	AH1	O	AVDD_SRDS2 ANALOG	17
No Connect Pins				
NC	C19, D7, D10, K13, L6, K9, B6, F12, J7, M19, M25, N19, N24, P19, R19, AB19, T12, W3, M12, W5, P12, T19, W1, W7, L13, U19, W4, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V19, W2, W6, W8, T11, U11, W12, W13, W14, W15, W16, W17, W18, W19, W27, V25, Y17, Y18, Y19, AA18, AA19, AB20, AB21, AB22, AB23, J9			

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5}}/\overline{\text{DMA_REQ2}}$ is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA_REQ2}}$.
2. Recommend a weak pull-up resistor (2 10 K Ω) be placed on this pin to OV_{DD}.
3. This pin must always be pulled high.
4. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull-up or active driver is needed. TSEC3_TXD[3] (cfg_srds_sgmii_refclk) is an exception, because the default value of this configuration signal is low (0). Thus, no external pull-down resistor is needed for selecting the default configuration value.
5. Treat these pins as no connects (NC) unless using debug address functionality.