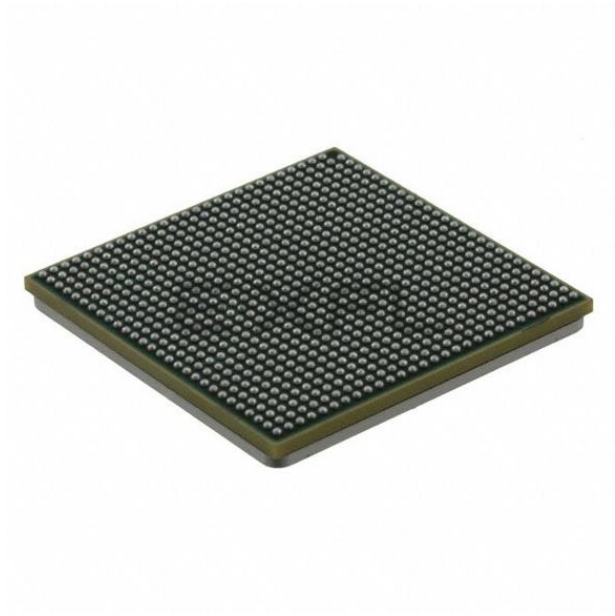

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544edvtang

  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache

- OCeaN switch fabric
  - Full crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both the local and remote masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Support for scatter and gather transfers
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no snoop)
  - Ability to start and flow control each DMA channel from external 3-pin interface
  - Ability to launch DMA from single write transaction
- PCI controller
  - PCI 2.2 compatible
  - One 32-bit PCI port with support for speeds from 16 to 66 MHz
  - Host and agent mode support
  - 64-bit dual address cycle (DAC) support
  - Supports PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses
  - Supports posting of processor-to-PCI and PCI-to-memory writes
  - PCI 3.3-V compatible
  - Selectable hardware-enforced coherency

6.1 DDR SDRAM DC Electrical Characteristics

Table 10 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8544E when GV_{DD}(typ) = 1.8 V.

Table 10. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.26	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.24	V	—
Output high current (V_{OUT} = 1.26 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.33 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

Table 11 provides the DDR2 I/O capacitance when GV_{DD}(typ) = 1.8 V.

Table 11. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 12 provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 12. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.31	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.3	V	—
Output high current (V_{OUT} = 1.8 V)	I_{OH}	–16.2	—	mA	—

Figure 5 shows the DDR SDRAM output timing diagram.

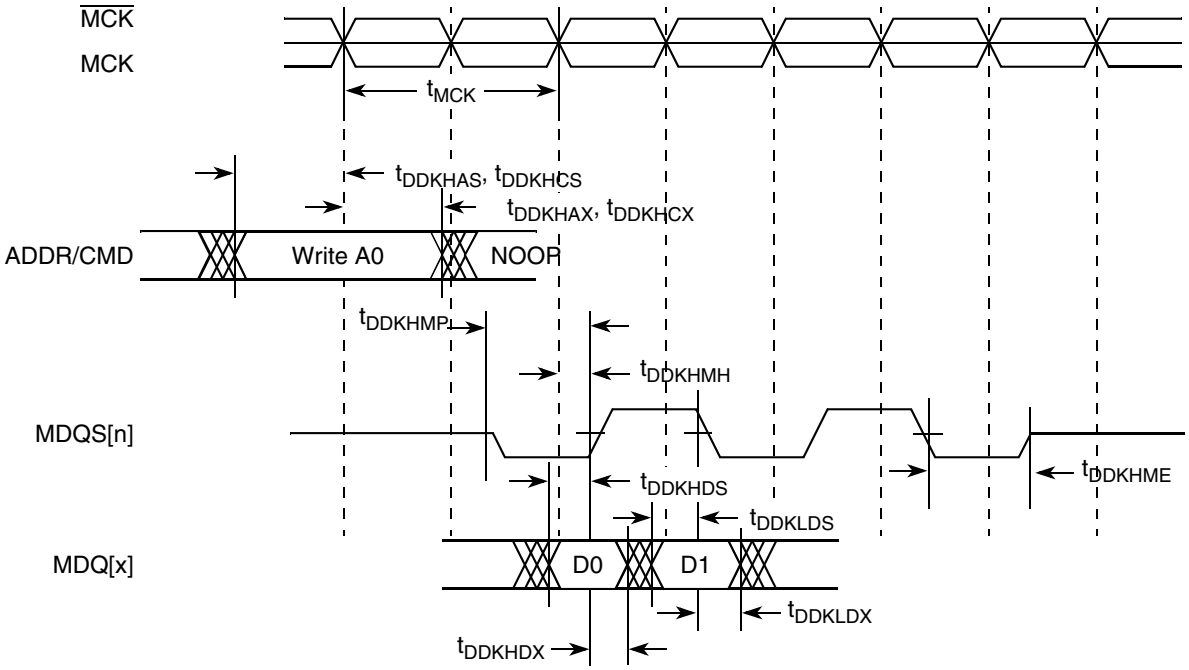


Figure 5. DDR and DDR2 SDRAM Output Timing Diagram

Figure 6 provides the AC test load for the DDR bus.

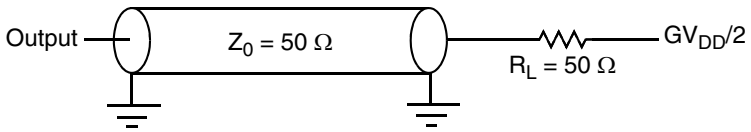


Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8544E.

7.1 DUART DC Electrical Characteristics

Table 19 provides the DC electrical characteristics for the DUART interface.

Table 19. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA	1
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—

Table 24. DC Transmitter Electrical Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage[2,3,5]	$\|V_{OD}\|$	323	500	725	mV	Equalization setting: 1.0x
		296	459	665		Equalization setting: 1.09x
		269	417	604		Equalization setting: 1.2x
		243	376	545		Equalization setting: 1.33x
		215	333	483		Equalization setting: 1.5x
		189	292	424		Equalization setting: 1.71x
		162	250	362		Equalization setting: 2.0x
Output offset voltage	V_{OS}	425	500	577.5	mV	1, 4
Output impedance (single ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between 0 and 1	$\Delta\|V_{OD}\|$	—	—	25	mV	—
Change in V_{OS} between 0 and 1	ΔV_{OS}	—	—	25	mV	—
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	—

Notes:

1. This will not align to DC-coupled SGMII.
2. $|V_{OD}| = |V_{SD2\_TXn} - V_{\overline{SD2\_TXn}}|$. $|V_{OD}|$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*|V_{OD}|$.
3. The $|V_{OD}|$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**CD** (for SerDes 2 lane 2 and 3) bit field of MPC8544E SerDes 2 control register 1:
   - The MSbit (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude—power up default);
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in this table.
4. V_{OS} is also referred to as output common mode voltage.
5. The $|V_{OD}|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0 V, no common mode offset variation (V_{OS} = 500 mV), SerDes2 transmitter is terminated with 100-Ω differential load between SD2_TX[n] and SD2_TX[n].

Figure 7 shows an example of a 4-wire AC-coupled SGMII serial link connection.

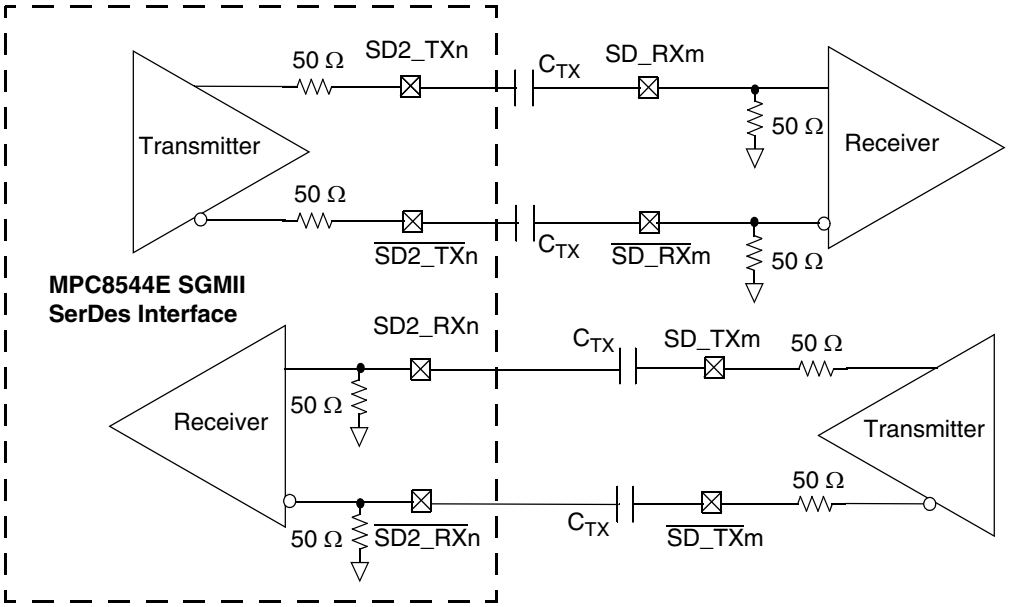


Figure 7. 4-Wire AC-Coupled SGMII Serial Link Connection Example

Figure 8 shows an SGMII transmitter DC measurement circuit.

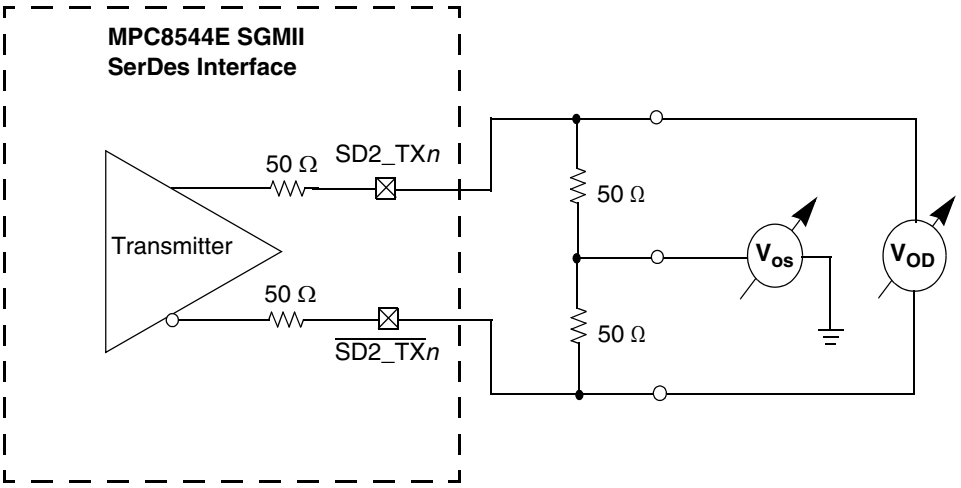


Figure 8. SGMII Transmitter DC Measurement Circuit

Table 25 shows the DC receiver electrical characteristics.

Table 25. DC Receiver Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD_SRDS2}	0.9	1.0	1.05	V	—
DC input voltage range	—	—	—	—	—	1

8.6.1 MII Transmit AC Timing Specifications

Table 32 provides the MII transmit AC timing specifications.

Table 32. MII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns	—
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns	—
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%	—
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns	—
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns	—
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 16 shows the MII transmit AC timing diagram.

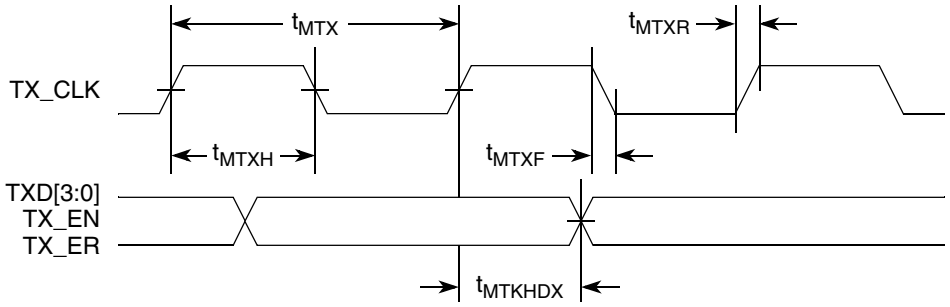


Figure 16. MII Transmit AC Timing Diagram

8.6.2 MII Receive AC Timing Specifications

Table 33 provides the MII receive AC timing specifications.

Table 33. MII Receive AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V ± 5%.or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns	—
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns	—
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%	—

8.7.5 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.7.5.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 38.

Table 38. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns	—
REF_CLK duty cycle	t_{RMTH}	35	50	65	%	—
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps	—
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns	—
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	1.0	—	10.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 23 shows the RMII transmit AC timing diagram.

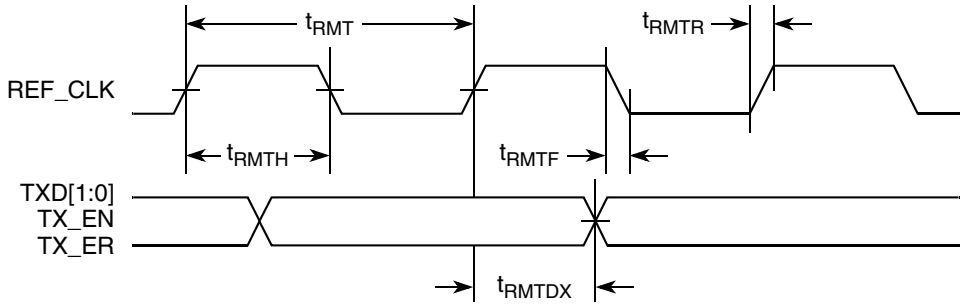


Figure 23. RMII Transmit AC Timing Diagram

Table 41. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns).
4. t_{plb_clk} is the platform (CCB) clock.

Figure 26 shows the MII management AC timing diagram.

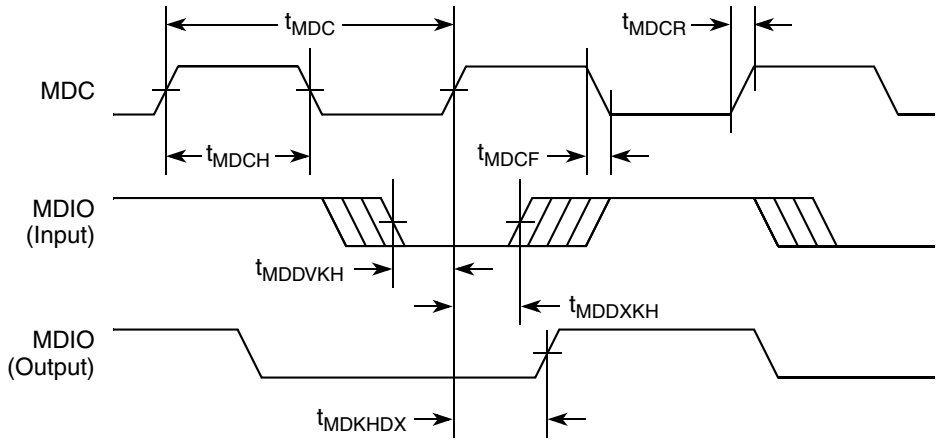


Figure 26. MII Management Interface Timing Diagram

Table 47. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC) (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 1.8-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

Figure 27 provides the AC test load for the local bus.

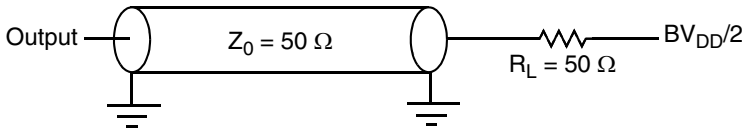


Figure 27. Local Bus AC Test Load

Figure 42 shows the PCI input AC timing conditions.

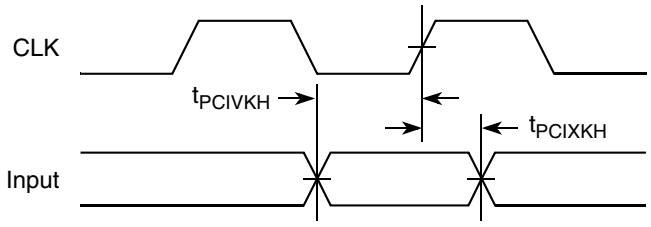


Figure 42. PCI Input AC Timing Measurement Conditions

Figure 43 shows the PCI output AC timing conditions.

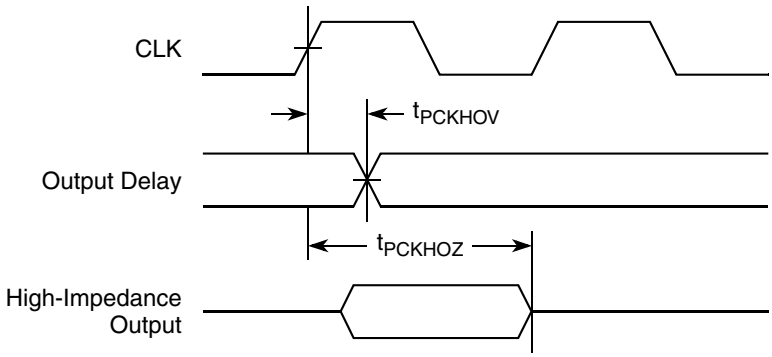


Figure 43. PCI Output AC Timing Measurement Condition

16 High-Speed Serial Interfaces (HSSI)

The MPC8544E features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications.The SerDes1 dedicated for PCI Express data transfers. The SerDes2 can be used for PCI Express and/or SGMII application. This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 44 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

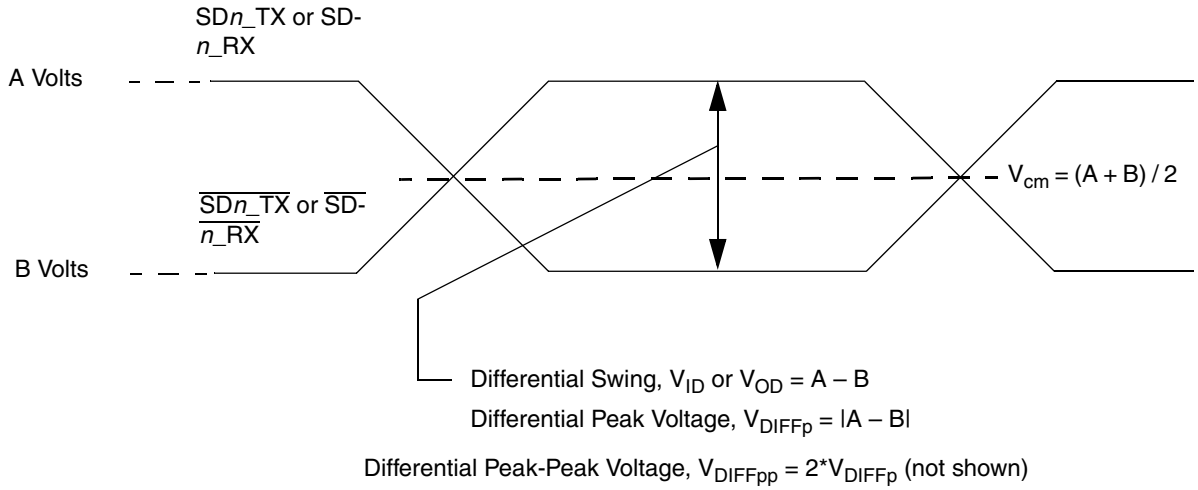


Figure 44. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$ for PCI Express1, PCI Express2. SD2_REF_CLK, and $\overline{\text{SD2\_REF\_CLK}}$ for the PCI Express3 or SGMII interface, respectively. The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 45 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XV_{DD_SRDS2} are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure
  - The SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 45. Each differential clock input (SD*n*_REF_CLK or $\overline{\text{SD}n\text{\_REF\_CLK}}$) has a 50-Ω termination to SGND_SRDS*n* (xcorevss) followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.

Table 59. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}RCV\text{-}DETECT}$	Amount of voltage change allowed during receiver detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.
$V_{TX\text{-}DC\text{-}CM}$	TX DC common mode voltage	0	—	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
$I_{TX\text{-}SHORT}$	TX short circuit current limit	—	—	90	mA	The total current the transmitter can provide when shorted to its ground.
$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum time spent in electrical idle	50	—	—	UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set.
$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical Idle ordered set	—	—	20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from LO.
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Maximum time to transition to valid TX specifications after leaving an electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle.
$RL_{TX\text{-}DIFF}$	Differential return loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$RL_{TX\text{-}CM}$	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance.
$Z_{TX\text{-}DC}$	Transmitter DC impedance	40	—	—	Ω	Required TX D+ as well as D– DC Impedance during all states.
$L_{TX\text{-}SKEW}$	Lane-to-lane output skew	—	—	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single link.
C_{TX}	AC coupling capacitor	75	—	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 57). Note that the series capacitors, CTX, are optional for the return loss measurement.

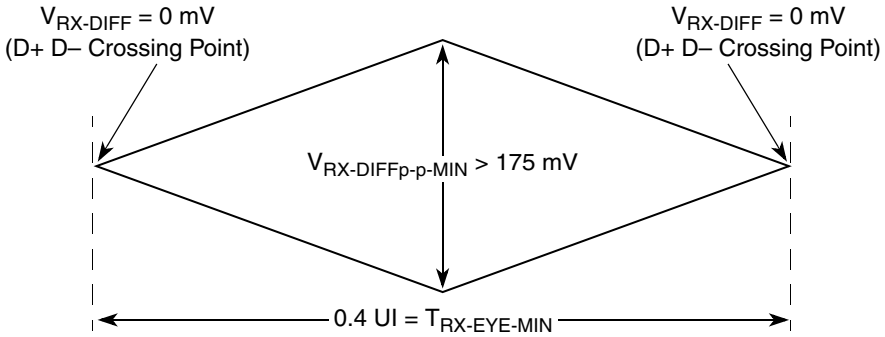


Figure 57. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 58.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

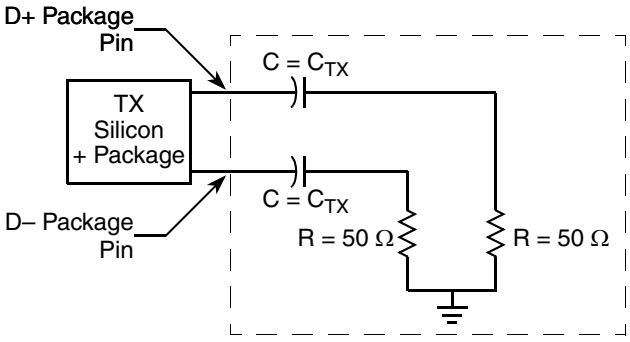


Figure 58. Compliance Test/Measurement Load

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Ethernet Management Interface				
EC_MDC	AC7	O	OV_{DD}	4, 8, 14
EC_MDIO	Y9	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	T2	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	U10, U9, T10, T9, U8, T8, T7, T6	I	LV_{DD}	—
TSEC1_TXD[7:0]	T5, U5, V5, V3, V2, V1, U2, U1	O	LV_{DD}	4, 8, 14
TSEC1_COL	R5	I	LV_{DD}	—
TSEC1_CRS	T4	I/O	LV_{DD}	16
TSEC1_GTX_CLK	T1	O	LV_{DD}	—
TSEC1_RX_CLK	V7	I	LV_{DD}	—
TSEC1_RX_DV	U7	I	LV_{DD}	—
TSEC1_RX_ER	R9	I	LV_{DD}	4, 8
TSEC1_TX_CLK	V6	I	LV_{DD}	—
TSEC1_TX_EN	U4	O	LV_{DD}	22
TSEC1_TX_ER	T3	O	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_RXD[7:0]	P11, N11, M11, L11, R8, N10, N9, P10	I	LV_{DD}	—
TSEC3_TXD[7:0]	M7, N7, P7, M8, L7, R6, P6, M6	O	LV_{DD}	4, 8, 14
TSEC3_COL	M9	I	LV_{DD}	—
TSEC3_CRS	L9	I/O	LV_{DD}	16
TSEC3_GTX_CLK	R7	O	LV_{DD}	—
TSEC3_RX_CLK	P9	I	LV_{DD}	—
TSEC3_RX_DV	P8	I	LV_{DD}	—
TSEC3_RX_ER	R11	I	LV_{DD}	—
TSEC3_TX_CLK	L10	I	LV_{DD}	—
TSEC3_TX_EN	N6	O	LV_{DD}	22
TSEC3_TX_ER	L8	O	LV_{DD}	4, 8
DUART				
$\overline{\text{UART\_CTS}}$[0:1]	AH8, AF6	I	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[0:1]	AG8, AG9	O	OV_{DD}	—

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
UART_SIN[0:1]	AG7, AH6	I	OV_{DD}	—
UART_SOUT[0:1]	AH7, AF7	O	OV_{DD}	—
I^2C interface				
IIC1_SCL	AG21	I/O	OV_{DD}	20
IIC1_SDA	AH21	I/O	OV_{DD}	20
IIC2_SCL	AG13	I/O	OV_{DD}	20
IIC2_SDA	AG14	I/O	OV_{DD}	20
SerDes 1				
SD1_RX[0:7]	N28, P26, R28, T26, Y26, AA28, AB26, AC28	I	XV_{DD}	—
$\overline{\text{SD1\_RX}}$[0:7]	N27, P25, R27, T25, Y25, AA27, AB25, AC27	I	XV_{DD}	—
SD1_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	O	XV_{DD}	—
$\overline{\text{SD1\_TX}}$[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	O	XV_{DD}	—
SD1_PLL_TPD	V28	O	XV_{DD}	17
SD1_REF_CLK	U28	I	XV_{DD}	—
$\overline{\text{SD1\_REF\_CLK}}$	U27	I	XV_{DD}	—
SD1_TST_CLK	T22		—	—
$\overline{\text{SD1\_TST\_CLK}}$	T23		—	—
SerDes 2				
SD2_RX[0]	AD25	I	XV_{DD}	—
SD2_RX[2]	AD1	I	XV_{DD}	26
SD2_RX[3]	AB2	I	XV_{DD}	26
$\overline{\text{SD2\_RX}}$[0]	AD26	I	XV_{DD}	—
$\overline{\text{SD2\_RX}}$[2]	AC1	I	XV_{DD}	26
$\overline{\text{SD2\_RX}}$[3]	AA2	I	XV_{DD}	26
SD2_TX[0]	AA21	O	XV_{DD}	—
SD2_TX[2]	AC4	O	XV_{DD}	26
SD2_TX[3]	AA5	O	XV_{DD}	26
$\overline{\text{SD2\_TX}}$[0]	AA20	O	XV_{DD}	—
$\overline{\text{SD2\_TX}}$[2]	AB4	O	XV_{DD}	26
$\overline{\text{SD2\_TX}}$[3]	Y5	O	XV_{DD}	26
SD2_PLL_TPD	AG3	O	XV_{DD}	17
SD2_REF_CLK	AE2	I	XV_{DD}	—

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
V_{DD}	L16, L14, M13, M15, M17, N12, N14, N16, N18, P13, P15, P17, R12, R14, R16, R18, T13, T15, T17, U12, U14, U16, U18,	Power for core (1.0 V)	V_{DD}	—
SVDD_SRDS	M27, N25, P28, R24, R26, T24, T27, U25, W24, W26, Y24, Y27, AA25, AB28, AD27	Core power for SerDes 1 transceivers (1.0 V)	SV_{DD}	—
SVDD_SRDS2	AB1, AC26, AD2, AE26, AG2	Core power for SerDes 2 transceivers (1.0 V)	SV_{DD}	—
XVDD_SRDS	M21, N23, P20, R22, T20, U23, V21, W22, Y20	Pad power for SerDes 1 transceivers (1.0 V)	XV_{DD}	—
XVDD_SRDS2	Y6, AA6, AA23, AF5, AG5	Pad power for SerDes 2 transceivers (1.0 V)	XV_{DD}	—
XGND_SRDS	M20, M24, N22, P21, R23, T21, U22, V20, W23, Y21	—	—	—
XGND_SRDS2	Y4, AA4, AA22, AD4, AE4, AH4	—	—	—
SGND_SRDS	M28, N26, P24, P27, R25, T28, U24, U26, V24, W25, Y28, AA24, AA26, AB24, AB27, AC24, AD28	—	—	—
AGND_SRDS	V27	SerDes PLL GND	—	—
SGND_SRDS2	Y2, AA1, AB3, AC2, AC3, AC25, AD3, AD24, AE3, AE1, AE25, AF3, AH2	—	—	—
AGND_SRDS2	AF1	SerDes PLL GND	—	—
AVDD_LBIU	C28	Power for local bus PLL (1.0 V)	—	19
AVDD_PCI1	AH20	Power for PCI PLL (1.0 V)	—	19
AVDD_CORE	AH14	Power for e500 PLL (1.0 V)	—	19
AVDD_PLAT	AH18	Power for CCB PLL (1.0 V)	—	19

19.5 Security Controller PLL Ratio

Table 67 shows the SEC frequency ratio.

Table 67. SEC Frequency Ratio

Signal Name	Value (Binary)	CCB CLK:SEC CLK
LWE_B	0	2:1[1]
	1	3:1[2]

Notes:
1. In 2:1 mode the CCB frequency must be operating ≤ 400 MHz.
2. In 3:1 mode any valid CCB can be used. The 3:1 mode is the default ratio for security block.

19.6 Frequency Options

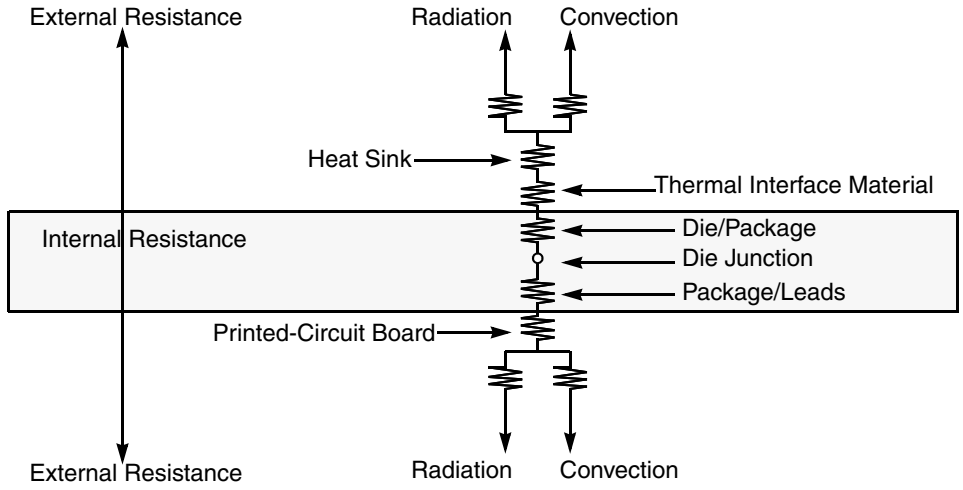
19.6.1 SYSCLK to Platform Frequency Options

Table 68 shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 68. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)						
	33.33	41.66	66.66	83	100	111	133.33
	Platform /CCB Frequency (MHz)						
2							—
3					—	333	400
4			—	333	400	445	533
5			333	415	500		
6			400	500			
8		333	533				
9		375					
10	333	417					
12	400	500					
16	533						

Figure 62 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance.)

Figure 62. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

20.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 63 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 69. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors built on Power Architecture™ technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic. The arrangement shown in Figure 69 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 68, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 68 is common to all known emulators.

23 Document Revision History

This table provides a revision history for the MPC8544E hardware specification.

Table 76. MPC8544E Document Revision History

Revision	Date	Substantive Change(s)
8	09/2015	• In Table 10 and Table 12, removed the output leakage current rows and removed table note 4.
7	06/2014	• In Table 75, “Device Nomenclature,” added full Pb-free part code. • In Table 75, “Device Nomenclature,” added footnotes 3 and 4.
6	05/2011	• Updated the value of t_{JTKLDX} to 2.5 ns from 4ns in Table 50.
5	01/2011	• Updated Table 75.
4	09/2010	• Modified local bus information in Section 1.1, “Key Features,” to show max local bus frequency as 133 MHz. • Added footnote 28 to Table 62. • Updated solder-ball parameter in Table 61.
3	11/2009	• Update Section 20.3.4, “Temperature Diode,” • Update Table 61 Package Parameters from 95.5%sn to 96.5%sn
2	01/2009	• Update power number table to include 1067 MHz/533 MHz power numbers. • Remove Part number tables from Hardware spec. The part numbers are available on Freescale web site product page. • Removed I/O power numbers from the Hardware spec. and added the table to bring-up guide application note. • Update t_{DDKHMP}, t_{DDKHME} in Table 18. • Updated RX_CLK duty cycle min, and max value to meet the industry standard GMII duty cycle. • Update paragraph Section 21.3, “Decoupling Recommendations.” • Update Figure 5 DDR Output Timing Diagram. • In Table 40, removed note 1 and renumbered remaining note. • Update Section 22, “Device Nomenclature,” with regards to Commercial Tier.
1	06/2008	Update in Table 18 DDR SDRAM Output AC Timing Specifications tMCK Max value Improvement to Section 16, “High-Speed Serial Interfaces (HSSI) Update Figure 59 Mechanical Dimensions Update in Table 48 Local Bus General Timing Parameters—PLL Bypassed
0	04/2008	Initial release.