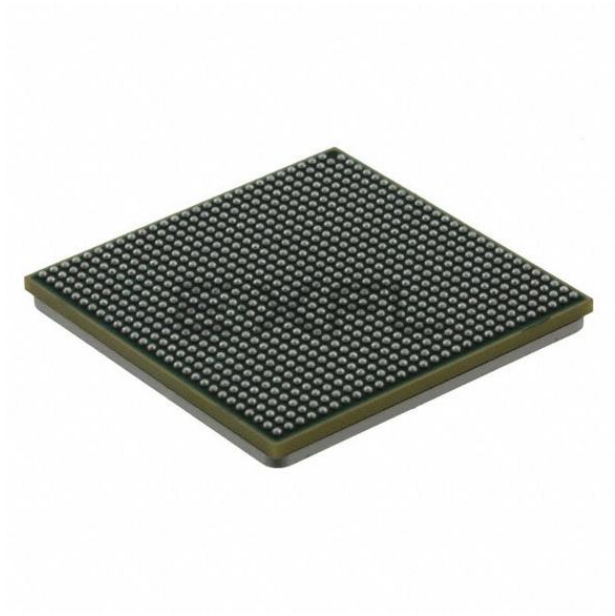

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 800MHz |
| Co-Processors/DSP | Signal Processing; SPE, Security; SEC |
| RAM Controllers | DDR, DDR2, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544evjanga |

**Table 2. Recommended Operating Conditions (continued)**

| Characteristic | | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|---|
| Three-speed Ethernet I/O voltage | | $LV_{DD}$ (eTSEC1) | 3.3 V ± 165 mV<br>2.5 V ± 125 mV | V | 4 |
| | | $TV_{DD}$ (eTSEC3) | 3.3 V ± 165 mV<br>2.5 V ± 125 mV | | |
| PCI, DUART, PCI Express, system control and power management, $I^2C$, and JTAG I/O voltage | | $OV_{DD}$ | 3.3 V ± 165 mV | V | 3 |
| Local bus I/O voltage | | $BV_{DD}$ | 3.3 V ± 165 mV<br>2.5 V ± 125 mV<br>1.8 V ± 90 mV | V | 5 |
| Input voltage | DDR and DDR2 DRAM signals | $MV_{IN}$ | GND to $GV_{DD}$ | V | 2 |
| | DDR and DDR2 DRAM reference | $MV_{REF}$ | GND to $GV_{DD}/2$ | V | 2 |
| | Three-speed Ethernet signals | $LV_{IN}$<br>$TV_{IN}$ | GND to $LV_{DD}$<br>GND to $TV_{DD}$ | V | 4 |
| | Local bus signals | $BV_{IN}$ | GND to $BV_{DD}$ | V | 5 |
| | PCI, Local bus, DUART, SYSCLK, system control and power management, $I^2C$, and JTAG signals | $OV_{IN}$ | GND to $OV_{DD}$ | V | 3 |
| Junction temperature range | | $T_j$ | 0 to 105 | °C | — |

**Notes:**

1. This voltage is the input to the filter discussed in Section 21.2, "PLL Power Supply Filtering," and not necessarily the voltage at the $AV_{DD}$ pin, which may be reduced from $V_{DD}$ by the filter.
2. **Caution:** $MV_{IN}$ must not exceed $GV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** $OV_{IN}$ must not exceed $OV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** $T/LV_{IN}$ must not exceed $T/ LV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution:** $BV_{IN}$ must not exceed $BV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Figure 7 shows an example of a 4-wire AC-coupled SGMII serial link connection.

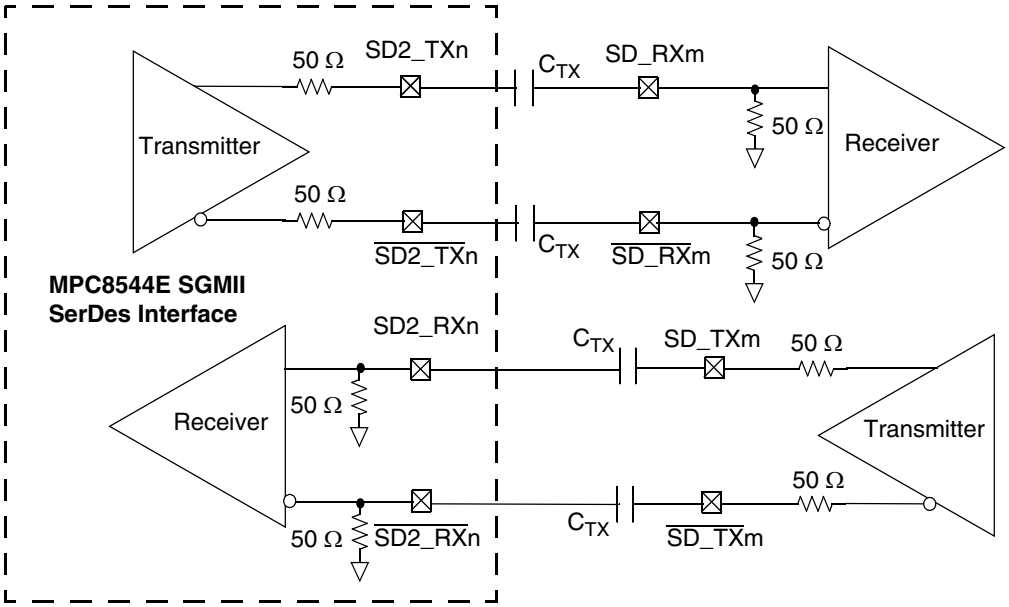


**Figure 7. 4-Wire AC-Coupled SGMII Serial Link Connection Example**

Figure 8 shows an SGMII transmitter DC measurement circuit.

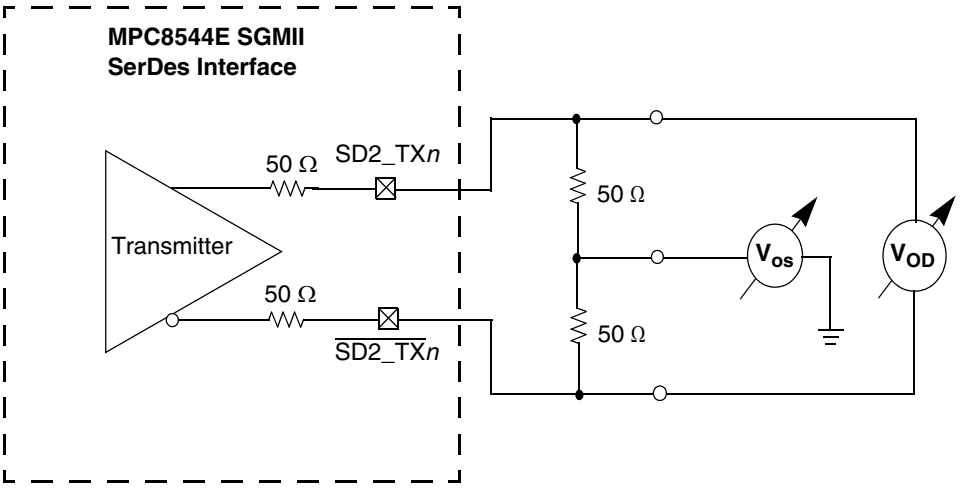


**Figure 8. SGMII Transmitter DC Measurement Circuit**

Table 25 shows the DC receiver electrical characteristics.

**Table 25. DC Receiver Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD\_SRDS2}$ | 0.9 | 1.0 | 1.05 | V | — |
| DC input voltage range | — | — | — | — | — | 1 |

### 8.7.1 TBI Transmit AC Timing Specifications

Table 34 provides the TBI transmit AC timing specifications.

**Table 34. TBI Transmit AC Timing Specifications**

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| GTX_CLK clock period | $t_{GTX}$ | — | 8.0 | — | ns | — |
| GTX_CLK to TCG[9:0] delay time | $t_{TTKHDX}$ | 0.2 | — | 5.0 | ns | 2 |
| GTX_CLK rise (20%–80%) | $t_{TTXR}$ | — | — | 1.0 | ns | — |
| GTX_CLK fall time (80%–20%) | $t_{TTXF}$ | — | — | 1.0 | ns | — |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state )(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TTKHDV}$ symbolizes the TBI transmit timing (TT) with respect to the time from $t_{TTX}$ (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, $t_{TTKHDX}$ symbolizes the TBI transmit timing (TT) with respect to the time from $t_{TTX}$ (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{TTX}$ represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Data valid $t_{TTKHDV}$ to GTX_CLK Min setup time is a function of clock period and max hold time (Min setup = cycle time – Max delay).

Figure 19 shows the TBI transmit AC timing diagram.

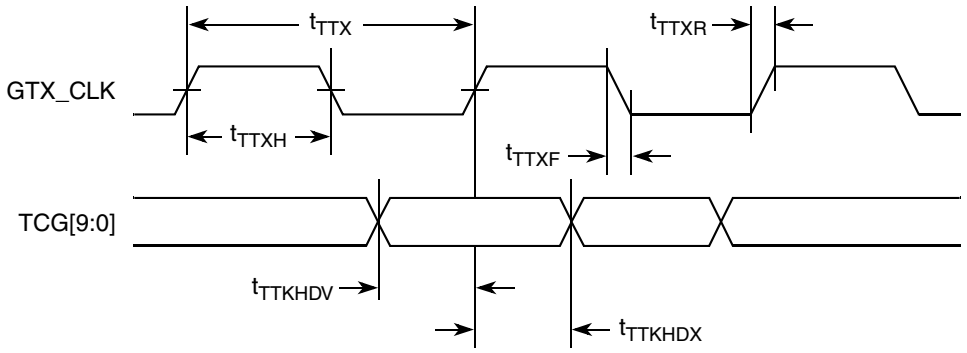


**Figure 19. TBI Transmit AC Timing Diagram**

### 8.7.2 TBI Receive AC Timing Specifications

Table 35 provides the TBI receive AC timing specifications.

**Table 35. TBI Receive AC Timing Specifications**

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| PMA_RX_CLK[0:1] clock period | $t_{TRX}$ | — | 16.0 | — | ns | — |
| PMA_RX_CLK[0:1] skew | $t_{SKTRX}$ | 7.5 | — | 8.5 | ns | — |

### 8.7.5.2 RMII Receive AC Timing Specifications

Table 39 shows the RMII receive AC timing specifications.

**Table 39. RMII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 3.3 V ± 5%.or 2.5 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| REF_CLK clock period | $t_{RMR}$ | 15.0 | 20.0 | 25.0 | ns | — |
| REF_CLK duty cycle | $t_{RMRH}$ | 35 | 50 | 65 | % | — |
| REF_CLK peak-to-peak jitter | $t_{RMRJ}$ | — | — | 250 | ps | — |
| Rise time REF_CLK (20%–80%) | $t_{RMRR}$ | 1.0 | — | 2.0 | ns | — |
| Fall time REF_CLK (80%–20%) | $t_{RMRF}$ | 1.0 | — | 2.0 | ns | — |
| RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge | $t_{RMRDV}$ | 4.0 | — | — | ns | — |
| RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge | $t_{RMRDX}$ | 2.0 | — | — | ns | — |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 24 provides the AC test load for eTSEC.

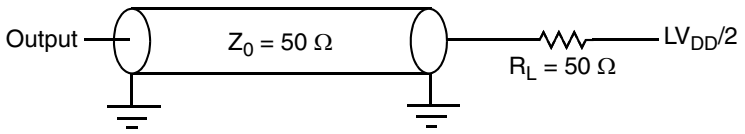


**Figure 24. eTSEC AC Test Load**

Figure 25 shows the RMII receive AC timing diagram.

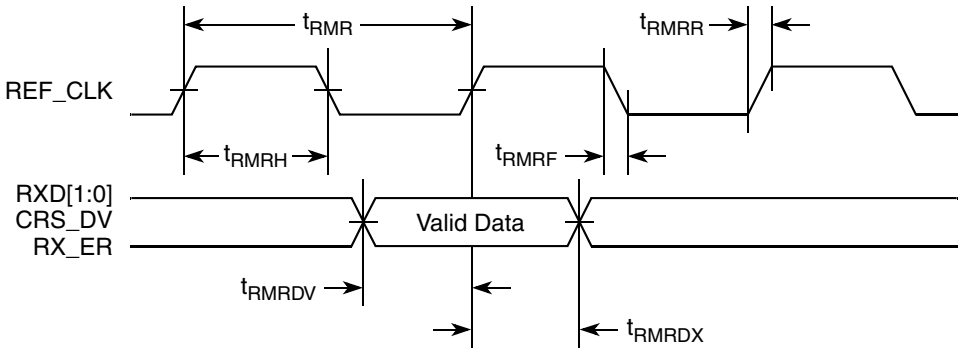


**Figure 25. RMII Receive AC Timing Diagram**

**Table 41. MII Management AC Timing Specifications (continued)**

At recommended operating conditions with $OV_{DD}$ is 3.3 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | — |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns).
4. $t_{plb\_clk}$ is the platform (CCB) clock.

Figure 26 shows the MII management AC timing diagram.

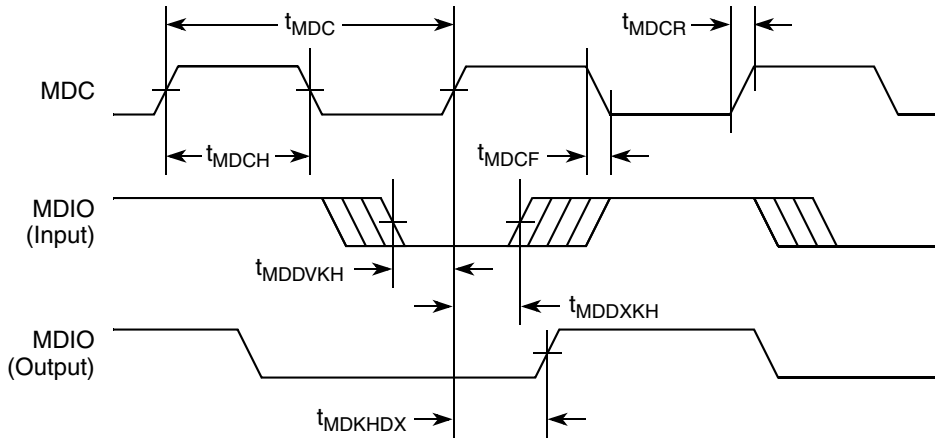


**Figure 26. MII Management Interface Timing Diagram**

# 10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8544E.

## 10.1 Local Bus DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD}$ = 3.3 V DC.

**Table 42. Local Bus DC Electrical Characteristics (3.3 V DC)**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $BV_{DD}$ + 0.3 | V | — |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V | — |
| Input current ($BV_{IN}$ = 0 V or $BV_{IN}$ = $BOV_{DD}$) | $I_{IN}$ | — | ±5 | μA | 1 |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**
1. The symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1 and Table 2.

Table 43 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD}$ = 2.5 V DC.

**Table 43. Local Bus DC Electrical Characteristics (2.5 V DC)**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 1.70 | $BV_{DD}$ + 0.3 | V | — |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.7 | V | — |
| Input current ($BV_{IN}$ = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±15 | μA | 1 |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –1 mA) | $V_{OH}$ | 2.0 | — | V | — |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 1 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**
1. The symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1 and Table 2.

Table 44 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD}$ = 1.8 V DC.

**Table 44. Local Bus DC Electrical Characteristics (1.8 V DC)**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 1.3 | $BV_{DD}$ + 0.3 | V | — |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.6 | V | — |
| Input current ($BV_{IN}$ = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±15 | μA | 1 |

**Table 48. Local Bus General Timing Parameters—PLL Bypassed (continued)**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus clock to data valid for LAD/LDP | $t_{LBKLOV2}$ | — | 1.6 | ns | 4 |
| Local bus clock to address valid for LAD, and LALE | $t_{LBKLOV3}$ | — | 1.6 | ns | 4 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKLOX1}$ | –4.1 | — | ns | 4 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKLOX2}$ | –4.1 | — | ns | 4 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKLOZ1}$ | — | 1.4 | ns | 7 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKLOZ2}$ | — | 1.4 | ns | 7 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one (1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which proceeds LCLK by $t_{LBKHKT}$.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from $BV_{DD}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of $t_{LBOTOT}$ is the measurement of the minimum time between the negation of LALE and any change in LAD.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

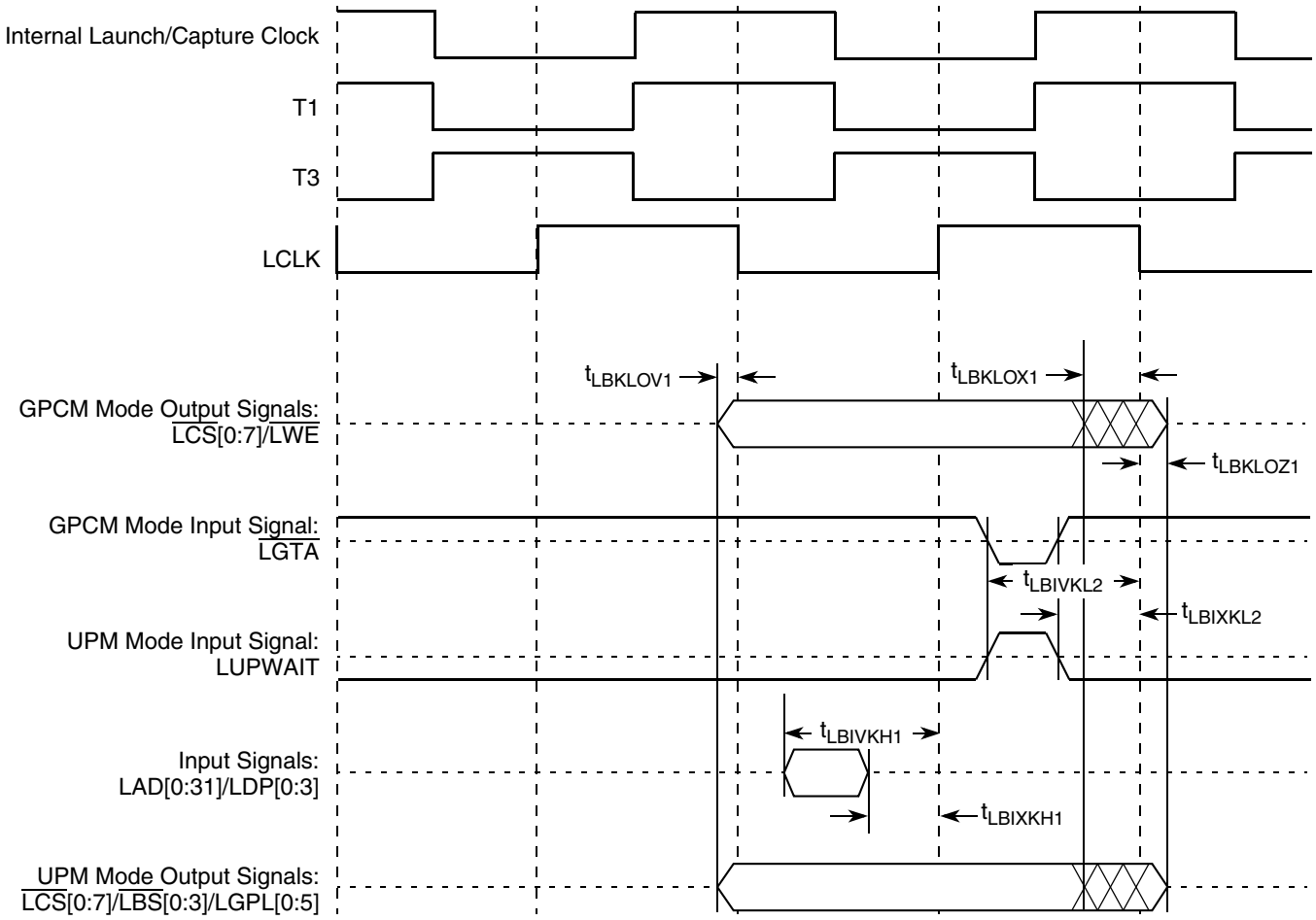


**Figure 31. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)**

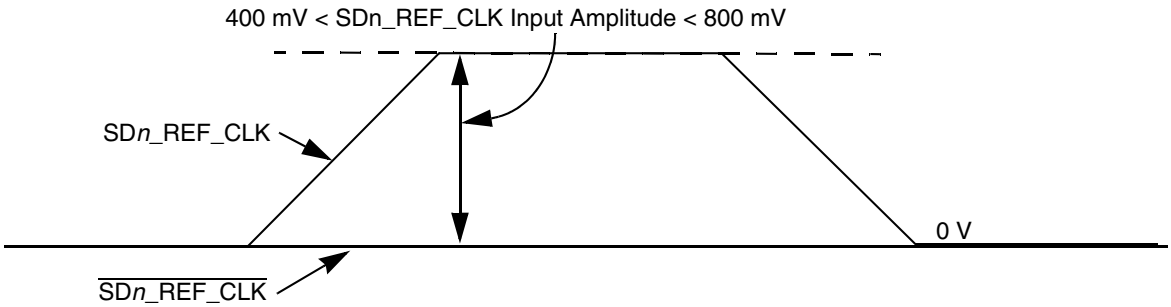


**Figure 48. Single-Ended Reference Clock Input DC Requirements**

### 16.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

**NOTE**

Figure 49 through Figure 52 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8544E SerDes reference clock receiver requirement provided in this document.

assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8544E SerDes reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

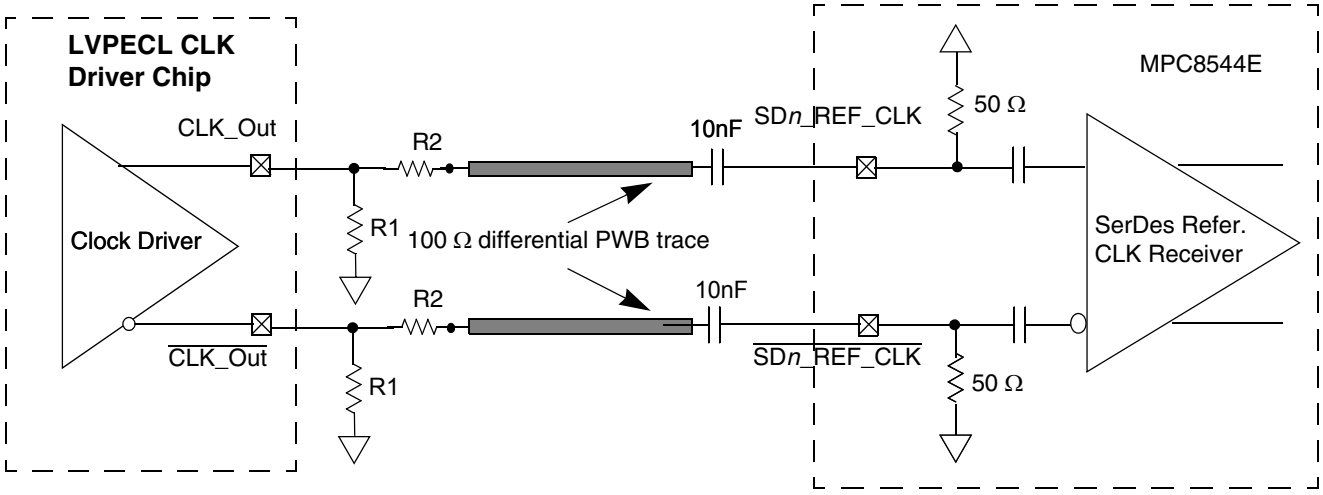


**Figure 51. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)**

Figure 52 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8544E SerDes reference clock input's DC requirement.

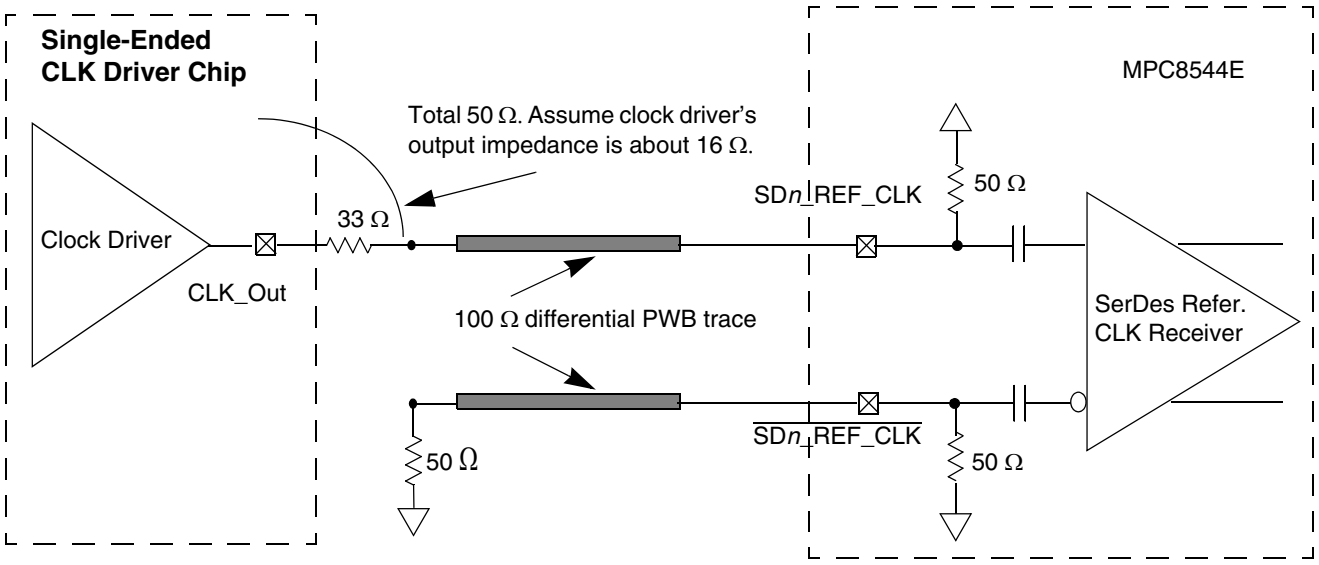


**Figure 52. Single-Ended Connection (Reference Only)**

### 17.4.1 Differential Transmitter (TX) Output

Table 59 defines the specifications for the differential output at all transmitters. The parameters are specified at the component pins.

**Table 59. Differential Transmitter (TX) Output Specifications**

| Symbol | Parameter | Min | Nom | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| UI | Unit interval | 399.88 | 400 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1. |
| $V_{TX-DIFFp-p}$ | Differential peak-to-peak output voltage | 0.8 | — | 1.2 | V | $V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$. See Note 2. |
| $V_{TX-DE-RATIO}$ | De- emphasized differential output voltage (ratio) | –3.0 | –3.5 | –4.0 | dB | Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2. |
| $T_{TX-EYE}$ | Minimum TX eye width | 0.70 | — | — | UI | The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3. |
| $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and maximum deviation from the median. | — | — | 0.15 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3. |
| $T_{TX-RISE}$, $T_{TX-FALL}$ | D+/D– TX output rise/fall time | 0.125 | — | — | UI | See Notes 2 and 5. |
| $V_{TX-CM-ACp}$ | RMS AC peak common mode output voltage | — | — | 20 | mV | $V_{TX-CM-ACp} = RMS(\|V_{TXD+} - V_{TXD-}\|/2 - V_{TX-CM-DC})$<br>$V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$<br>See Note 2. |
| $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$ | Absolute delta of DC common mode voltage during LO and electrical idle | 0 | — | 100 | mV | $\|V_{TX-CM-DC\ (during\ LO)} - V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}\| <= 100$ mV<br>$V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$ [LO]<br>$V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$ [Electrical Idle]<br>See Note 2. |
| $V_{TX-CM-DC-LINE-DELTA}$ | Absolute delta of DC common mode between D+ and D– | 0 | — | 25 | mV | $\|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\| <= 25$ mV<br>$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $\|V_{TX-D+}\|$<br>$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $\|V_{TX-D-}\|$<br>See Note 2. |
| $V_{TX-IDLE-DIFFp}$ | Electrical idle differential peak output voltage | 0 | — | 20 | mV | $V_{TX-IDLE-DIFFp} = \|V_{TX-IDLE-D+} - V_{TX-IDLE-D-}\| <= 20$ mV<br>See Note 2. |

**Table 59. Differential Transmitter (TX) Output Specifications (continued)**

| Symbol | Parameter | Min | Nom | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $V_{TX\text{-}RCV\text{-}DETECT}$ | Amount of voltage change allowed during receiver detection | — | — | 600 | mV | The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6. |
| $V_{TX\text{-}DC\text{-}CM}$ | TX DC common mode voltage | 0 | — | 3.6 | V | The allowed DC common mode voltage under any conditions. See Note 6. |
| $I_{TX\text{-}SHORT}$ | TX short circuit current limit | — | — | 90 | mA | The total current the transmitter can provide when shorted to its ground. |
| $T_{TX\text{-}IDLE\text{-}MIN}$ | Minimum time spent in electrical idle | 50 | — | — | UI | Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set. |
| $T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$ | Maximum time to transition to a valid electrical idle after sending an electrical Idle ordered set | — | — | 20 | UI | After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from LO. |
| $T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$ | Maximum time to transition to valid TX specifications after leaving an electrical idle condition | — | — | 20 | UI | Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle. |
| $RL_{TX\text{-}DIFF}$ | Differential return loss | 12 | — | — | dB | Measured over 50 MHz to 1.25 GHz. See Note 4. |
| $RL_{TX\text{-}CM}$ | Common mode return loss | 6 | — | — | dB | Measured over 50 MHz to 1.25 GHz. See Note 4. |
| $Z_{TX\text{-}DIFF\text{-}DC}$ | DC differential TX impedance | 80 | 100 | 120 | Ω | TX DC differential mode low impedance. |
| $Z_{TX\text{-}DC}$ | Transmitter DC impedance | 40 | — | — | Ω | Required TX D+ as well as D– DC Impedance during all states. |
| $L_{TX\text{-}SKEW}$ | Lane-to-lane output skew | — | — | 500 + 2 UI | ps | Static skew between any two transmitter lanes within a single link. |
| $C_{TX}$ | AC coupling capacitor | 75 | — | 200 | nF | All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. |

**Table 60. Differential Receiver (RX) Input Specifications (continued)**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and maximum deviation from the median | — | — | 0.3 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7. |
| $V_{RX-CM-ACp}$ | AC peak common mode input voltage | — | — | 150 | mV | $V_{RX-CM-ACp} = \lvert V_{RXD+} - V_{RXD-}\rvert \div 2 - V_{RX-CM-DC}$<br>$V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} - V_{RX-D-}\rvert/2$<br>See Note 2. |
| $RL_{RX-DIFF}$ | Differential return loss | 15 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 and –300 mV, respectively. See Note 4. |
| $RL_{RX-CM}$ | Common mode return loss | 6 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4. |
| $Z_{RX-DIFF-DC}$ | DC differential input impedance | 80 | 100 | 120 | Ω | RX DC differential mode impedance. See Note 5. |
| $Z_{RX-DC}$ | DC input impedance | 40 | 50 | 60 | Ω | Required RX D+ as well as D– DC impedance (50 ± 20% tolerance).<br>See Notes 2 and 5. |
| $Z_{RX-HIGH-IMP-DC}$ | Powered down DC input impedance | 200 k | — | — | Ω | Required RX D+ as well as D– DC impedance when the receiver terminations do not have power. See Note 6. |
| $V_{RX-IDLE-DET-DIFFp-p}$ | Electrical idle detect threshold | 65 | — | 175 | mV | $V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-}\rvert$<br>Measured at the package pins of the receiver. |
| $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ | Unexpected electrical idle enter detect threshold integration time | — | — | 10 | ms | An unexpected electrical idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition. |

**Table 62. MPC8544E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| LCS6/DMA_DACK2 | J16 | O | $BV_{DD}$ | 1 |
| LCS7/DMA_DDONE2 | L18 | O | $BV_{DD}$ | 1 |
| LWE0/LBS0/LSDDQM[0] | J22 | O | $BV_{DD}$ | 4, 8 |
| LWE1/LBS1/LSDDQM[1] | H22 | O | $BV_{DD}$ | 4, 8 |
| LWE2/LBS2/LSDDQM[2] | H23 | O | $BV_{DD}$ | 4, 8 |
| LWE3/LBS3/LSDDQM[3] | H21 | O | $BV_{DD}$ | 4, 8 |
| LALE | J26 | O | $BV_{DD}$ | 4, 7, 8 |
| LBCTL | J25 | O | $BV_{DD}$ | 4, 7, 8 |
| LGPL0/LSDA10 | J20 | O | $BV_{DD}$ | 4, 8 |
| LGPL1/LSDWE | K20 | O | $BV_{DD}$ | 4, 8 |
| LGPL2/LOE/LSDRAS | G20 | O | $BV_{DD}$ | 4, 7, 8 |
| LGPL3/LSDCAS | H18 | O | $BV_{DD}$ | 4, 8 |
| LGPL4/LGTA/LUPWAIT/ LPBSE | L20 | I/O | $BV_{DD}$ | 28 |
| LGPL5 | K19 | O | $BV_{DD}$ | 4, 8 |
| LCKE | L17 | O | $BV_{DD}$ | — |
| LCLK[0:2] | H24, J24, H25 | O | $BV_{DD}$ | — |
| LSYNC_IN | D27 | I | $BV_{DD}$ | — |
| LSYNC_OUT | D28 | O | $BV_{DD}$ | — |
| **DMA** | | | | |
| DMA_DACK[0:1] | Y13, Y12 | O | $OV_{DD}$ | 4, 8, 9 |
| DMA_DREQ[0:1] | AA10, AA11 | I | $OV_{DD}$ | — |
| DMA_DDONE[0:1] | AA7, Y11 | O | $OV_{DD}$ | — |
| **Programmable Interrupt Controller** | | | | |
| UDE | AH15 | I | $OV_{DD}$ | — |
| MCP | AG18 | I | $OV_{DD}$ | — |
| IRQ[0:7] | AG22, AF17, AD21, AF19, AG17, AF16, AC23, AC22 | I | $OV_{DD}$ | — |
| IRQ[8] | AC19 | I | $OV_{DD}$ | — |
| IRQ[9]/DMA_DREQ3 | AG20 | I | $OV_{DD}$ | 1 |
| IRQ[10]/DMA_DACK3 | AE27 | I/O | $OV_{DD}$ | 1 |
| IRQ[11]/DMA_DDONE3 | AE24 | I/O | $OV_{DD}$ | 1 |
| IRQ_OUT | AD14 | O | $OV_{DD}$ | 2 |

**Table 62. MPC8544E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **Ethernet Management Interface** | | | | |
| EC_MDC | AC7 | O | $OV_{DD}$ | 4, 8, 14 |
| EC_MDIO | Y9 | I/O | $OV_{DD}$ | — |
| **Gigabit Reference Clock** | | | | |
| EC_GTX_CLK125 | T2 | I | $LV_{DD}$ | — |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 1)** | | | | |
| TSEC1_RXD[7:0] | U10, U9, T10, T9, U8, T8, T7, T6 | I | $LV_{DD}$ | — |
| TSEC1_TXD[7:0] | T5, U5, V5, V3, V2, V1, U2, U1 | O | $LV_{DD}$ | 4, 8, 14 |
| TSEC1_COL | R5 | I | $LV_{DD}$ | — |
| TSEC1_CRS | T4 | I/O | $LV_{DD}$ | 16 |
| TSEC1_GTX_CLK | T1 | O | $LV_{DD}$ | — |
| TSEC1_RX_CLK | V7 | I | $LV_{DD}$ | — |
| TSEC1_RX_DV | U7 | I | $LV_{DD}$ | — |
| TSEC1_RX_ER | R9 | I | $LV_{DD}$ | 4, 8 |
| TSEC1_TX_CLK | V6 | I | $LV_{DD}$ | — |
| TSEC1_TX_EN | U4 | O | $LV_{DD}$ | 22 |
| TSEC1_TX_ER | T3 | O | $LV_{DD}$ | — |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 3)** | | | | |
| TSEC3_RXD[7:0] | P11, N11, M11, L11, R8, N10, N9, P10 | I | $LV_{DD}$ | — |
| TSEC3_TXD[7:0] | M7, N7, P7, M8, L7, R6, P6, M6 | O | $LV_{DD}$ | 4, 8, 14 |
| TSEC3_COL | M9 | I | $LV_{DD}$ | — |
| TSEC3_CRS | L9 | I/O | $LV_{DD}$ | 16 |
| TSEC3_GTX_CLK | R7 | O | $LV_{DD}$ | — |
| TSEC3_RX_CLK | P9 | I | $LV_{DD}$ | — |
| TSEC3_RX_DV | P8 | I | $LV_{DD}$ | — |
| TSEC3_RX_ER | R11 | I | $LV_{DD}$ | — |
| TSEC3_TX_CLK | L10 | I | $LV_{DD}$ | — |
| TSEC3_TX_EN | N6 | O | $LV_{DD}$ | 22 |
| TSEC3_TX_ER | L8 | O | $LV_{DD}$ | 4, 8 |
| **DUART** | | | | |
| $\overline{\text{UART\_CTS}}$[0:1] | AH8, AF6 | I | $OV_{DD}$ | — |
| $\overline{\text{UART\_RTS}}$[0:1] | AG8, AG9 | O | $OV_{DD}$ | — |

**Table 62. MPC8544E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| AVDD_SRDS | W28 | Power for SRDSPLL (1.0 V) | — | 19 |
| AVDD_SRDS2 | AG1 | Power for SRDSPLL (1.0 V) | — | 19 |
| SENSEVDD | W11 | O | $V_{DD}$ | 12 |
| SENSEVSS | W10 | — | — | 12 |
| **Analog Signals** | | | | |
| MVREF | A28 | Reference voltage signal for DDR | MVREF | — |
| SD1_IMP_CAL_RX | M26 | — | 200Ω to GND | — |
| SD1_IMP_CAL_TX | AE28 | — | 100Ω to GND | — |
| SD1_PLL_TPA | V26 | — | AVDD_SRDS ANALOG | 17 |
| SD2_IMP_CAL_RX | AH3 | I | 200 Ω to GND | — |
| SD2_IMP_CAL_TX | Y1 | I | 100 Ω to GND | — |
| SD2_PLL_TPA | AH1 | O | AVDD_SRDS2 ANALOG | 17 |
| **No Connect Pins** | | | | |
| NC | C19, D7, D10, K13, L6, K9, B6, F12, J7, M19, M25, N19, N24, P19, R19, AB19, T12, W3, M12, W5, P12, T19, W1, W7, L13, U19, W4, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V19, W2, W6, W8, T11, U11, W12, W13, W14, W15, W16, W17, W18, W19, W27, V25, Y17, Y18, Y19, AA18, AA19, AB20, AB21, AB22, AB23, J9 | — | — | — |

**Notes:**

1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5}}/\overline{\text{DMA\_REQ2}}$ is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA\_REQ2}}$.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to $OV_{DD}$.
3. This pin must always be pulled high.
4. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull-up or active driver is needed. TSEC3_TXD[3] (cfg_srds_sgmii_refclk) is an exception, because the default value of this configuration signal is low (0). Thus, no external pull-down resistor is needed for selecting the default configuration value.
5. Treat these pins as no connects (NC) unless using debug address functionality.

Table 71 provides the thermal resistance with heat sink in open flow.

**Table 71. Thermal Resistance with Heat Sink in Open Flow**

| Heat Sink with Thermal Grease | Air Flow | Thermal Resistance (°C/W) |
|---|---|---|
| Wakefield 53 × 53 × 25 mm pin fin | Natural convection | 6.1 |
| Wakefield 53 × 53 × 25 mm pin fin | 1 m/s | 3.0 |
| Aavid 35 × 31 × 23 mm pin fin | Natural convection | 8.1 |
| Aavid 35 × 31 × 23 mm pin fin | 1 m/s | 4.3 |
| Aavid 30 × 30 × 9.4 mm pin fin | Natural convection | 11.6 |
| Aavid 30 × 30 × 9.4 mm pin fin | 1 m/s | 6.7 |
| Aavid 43 × 41 × 16.5 mm pin fin | Natural convection | 8.3 |
| Aavid 43 × 41 × 16.5 mm pin fin | 1 m/s | 4.3 |

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease. For system thermal modeling, the MPC8544E thermal model without a lid is shown in Figure 60. The substrate is modeled as a block 29 × 29 × 1.18 mm with an in-plane conductivity of 18.0 W/m•K and a through-plane conductivity of 1.0 W/m•K. The solder balls and air are modeled as a single block 29 × 29 × 0.58 mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 7.6 × 8.4 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 6.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to Figure 59 for actual dimensions.

## 20.2 Recommended Thermal Model

Table 72 shows the MPC8544E thermal model.

**Table 72. MPC8544EThermal Model**

| Conductivity | Value | Units |
|---|---|---|
| **Die (7.6 × 8.4 × 0.75mm)** | | |
| Silicon | Temperature dependent | — |
| **Bump/Underfill (7.6 × 8.4 × 0.070 mm) Collapsed Thermal Resistance** | | |
| Kz | 6.5 | W/m•K |
| **Substrate (29 × 29 × 1.18 mm)** | | |
| Kx | 18 | W/m•K |
| Ky | 18 | |
| Kz | 1.0 | |

## 21.10 Guidelines for High-Speed Interface Termination

This section provides guidelines for when the SerDes interface is either not used at all or only partly used.

### 21.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins.

The following pins must be left unconnected (float):

- SD_TX[0:7]
- $\overline{\text{SD\_TX}}$[0:7]

The following pins must be connected to GND:

- SD_RX[0:7]
- $\overline{\text{SD\_RX}}$[0:7]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

### 21.10.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[0:7]
- $\overline{\text{SD\_TX}}$[0:7]

The following pins must be connected to GND if not used:

- SD_RX[0:7]
- $\overline{\text{SD\_RX}}$[0:7]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

## 21.11 Guideline for PCI Interface Termination

PCI termination, if not used at all, is done as follows.

Option 1

- If PCI arbiter is enabled during POR,
- All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating.
- All PCI control pins can be grouped together and tied to $OV_{DD}$ through a single 10-kΩ resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

Option 2

- If PCI arbiter is disabled during POR,
- All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to $OV_{DD}$ through a single (or multiple) 10-kΩ resistor(s).
- All PCI control pins can be grouped together and tied to $OV_{DD}$ through a single 10-kΩ resistor.

## 21.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following list shows the termination recommendation:

- For LDP[0:3]: tie them to ground or the power supply rail via a 4.7-kΩ resistor.
- For LPBSE: tie it to the power supply rail via a 4.7-kΩ resistor (pull-up resistor).

# 22 Device Nomenclature

Ordering information for the parts fully covered by this hardware specifications document is provided in Section 22.3, "Part Marking." Contact your local Freescale sales office or regional marketing team for order information.

## 22.1 Industrial and Commercial Tier Qualification

The MPC8544E device has been tested to meet the industrial tier qualification. Table 74 provides a description for commercial and industrial qualifications.

**Table 74. Commercial and Industrial Description**

| Tier[1] | Typical Application Use Time | Power-On Hours | Example of Typical Applications |
|---|---|---|---|
| Commercial | 5 years | Part-time/ Full-Time | PC's, consumer electronics, office automation, SOHO networking, portable telecom products, PDAs, etc. |
| Industrial | 10 years | Typically Full-Time | Installed telecom equipment, work stations, servers, warehouse equipment, etc. |

**Note:**
1. Refer to Table 2 for operating temperature ranges. Temperature is independent of tier and varies per product.

# 23 Document Revision History

This table provides a revision history for the MPC8544E hardware specification.

**Table 76. MPC8544E Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 8 | 09/2015 | • In Table 10 and Table 12, removed the output leakage current rows and removed table note 4. |
| 7 | 06/2014 | • In Table 75, “Device Nomenclature,” added full Pb-free part code.<br>• In Table 75, “Device Nomenclature,” added footnotes 3 and 4. |
| 6 | 05/2011 | • Updated the value of $t_{JTKLDX}$ to 2.5 ns from 4ns in Table 50. |
| 5 | 01/2011 | • Updated Table 75. |
| 4 | 09/2010 | • Modified local bus information in Section 1.1, “Key Features,” to show max local bus frequency as 133 MHz.<br>• Added footnote 28 to Table 62.<br>• Updated solder-ball parameter in Table 61. |
| 3 | 11/2009 | • Update Section 20.3.4, “Temperature Diode,”<br>• Update Table 61 Package Parameters from 95.5%sn to 96.5%sn |
| 2 | 01/2009 | • Update power number table to include 1067 MHz/533 MHz power numbers.<br>• Remove Part number tables from Hardware spec. The part numbers are available on Freescale web site product page.<br>• Removed I/O power numbers from the Hardware spec. and added the table to bring-up guide application note.<br>• Update $t_{DDKHMP}$, $t_{DDKHME}$ in Table 18.<br>• Updated RX_CLK duty cycle min, and max value to meet the industry standard GMII duty cycle.<br>• Update paragraph Section 21.3, “Decoupling Recommendations.”<br>• Update Figure 5 DDR Output Timing Diagram.<br>• In Table 40, removed note 1 and renumbered remaining note.<br>• Update Section 22, “Device Nomenclature,” with regards to Commercial Tier. |
| 1 | 06/2008 | Update in Table 18 DDR SDRAM Output AC Timing Specifications tMCK Max value<br>Improvement to Section 16, “High-Speed Serial Interfaces (HSSI)<br>Update Figure 59 Mechanical Dimensions<br>Update in Table 48 Local Bus General Timing Parameters—PLL Bypassed |
| 0 | 04/2008 | Initial release. |