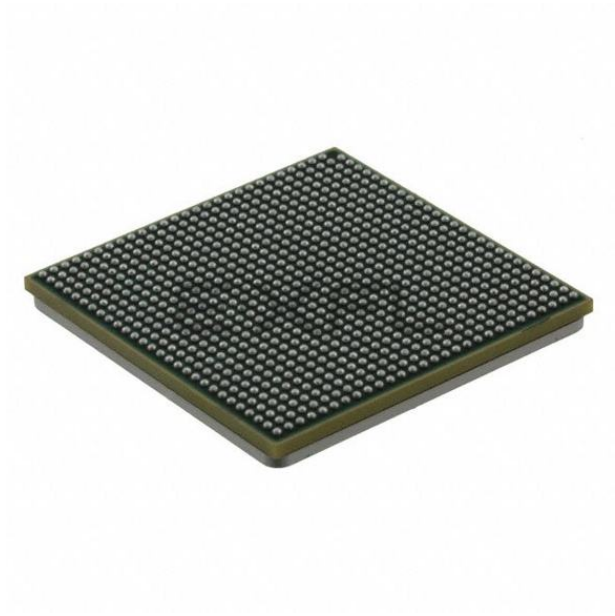

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.067GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544evjarja

Table 1. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Notes
DDR and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage		LV_{DD} (eTSEC1)	–0.3 to 3.63 –0.3 to 2.75	V	—
		TV_{DD} (eTSEC3)	–0.3 to 3.63 –0.3 to 2.75	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR/DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2
	DDR/DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	2
	Local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	V	—
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	2
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	2
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause.
2. (M,L,O)V_{IN}, and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for this device. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.0 ± 50 mV	V	—
PLL supply voltage	AV_{DD}	1.0 ± 50 mV	V	1
Core power supply for SerDes transceivers	SV_{DD}	1.0 ± 50 mV	V	—
Pad power supply for SerDes transceivers	XV_{DD}	1.0 ± 50 mV	V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	2

Table 2. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Three-speed Ethernet I/O voltage		LV_{DD} (eTSEC1)	3.3 V ± 165 mV 2.5 V ± 125 mV	V	4
		TV_{DD} (eTSEC3)	3.3 V ± 165 mV 2.5 V ± 125 mV		
PCI, DUART, PCI Express, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	3
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	5
Input voltage	DDR and DDR2 DRAM signals	MV_{IN}	GND to GV_{DD}	V	2
	DDR and DDR2 DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	2
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	4
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	5
	PCI, Local bus, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	3
Junction temperature range		T_j	0 to 105	°C	—

Notes:

1. This voltage is the input to the filter discussed in Section 21.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** T/LV_{IN} must not exceed T/ LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution:** BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Characteristics.”

8.2 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RTBI, RMII, and FIFO drivers and receivers comply with the DC parametric attributes specified in Table 21 and Table 22. The potential applied to the input of a GMII, MII, TBI, RTBI, RMII, and FIFO receiver may exceed the potential of the receiver’s power supply (that is, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 21. GMII, MII, TBI, RMII and FIFO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.135	3.465	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	—	0.5	V	—
Input high voltage	V_{IH}	1.95	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	40	μA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	3

Notes:
1. LV_{DD} supports eTSEC1.
2. TV_{DD} supports eTSEC3.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 22. GMII, MII, RMII, RGMII, RTBI, TBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.375	2.625	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.7	V	—
Input current (V_{IN} = 0, V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IN}	—	±15	μA	1, 2, 3

Notes:
1. LV_{DD} supports eTSEC1.
2. TV_{DD} supports eTSEC3.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 25. DC Receiver Electrical Characteristics (continued)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Input differential voltage	LSTS = 0	V_{rx_diffpp}	100	—	1200	mV	2, 4
	LSTS = 1		175	—			
Loss of signal threshold	LSTS = 0	VI_{os}	30	—	100	mV	3, 4
	LSTS = 1		65	—	175		
Input AC common mode voltage		V_{cm_acpp}	—	—	100	mV	5.
Receiver differential input impedance		Zrx_diff	80	—	120	Ω	—
Receiver common mode input impedance		Zrx_cm	20	—	35	Ω	—
Common mode input voltage		Vcm	xcorevss	—	xcorevss	V	6

Notes:
1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to Section 17.4.3, "Differential Receiver (RX) Input Specifications," for further explanation.
4. The LSTS shown in this table refers to the LSTS**CD** bit field of MPC8544E SerDes 2 control register 1.
5. $V_{CM\_ACp\text{-}p}$ is also referred to as peak-to-peak AC common mode voltage.
6. On-chip termination to SGND_SRDS2 (xcorevss).

8.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) or at the receiver inputs (SD2_RX[n] and $\overline{\text{SD2\_RX}}$[n]) as depicted in Figure 10, respectively.

8.4.1 SGMII Transmit AC Timing Specifications

Table 26 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 26. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XVDD_SRDS2 = 1.0 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	J_D	—	—	0.17	UI p-p	—
Total jitter	J_T	—	—	0.35	UI p-p	—
Unit interval	U_I	799.92	800	800.08	ps	2
V_{OD} fall time (80%–20%)	t_{fall}	50	—	120	ps	—
V_{OD} rise time (20%–80%)	t_{rise}	50	—	120	ps	—

Notes;
1. Source synchronous clock is not supported.
2. Each UI value is 800 ps ± 100 ppm.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 36.

Table 36. TBI Single-Clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns	—
RX_CLK duty cycle	t_{TRRH}	40	50	60	%	—
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps	—
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	1.0	ns	—
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	1.0	ns	—
RCG[9:0] setup time to RX_CLK rising edge	t_{TRRDV}	2.0	—	—	ns	—
RCG[9:0] hold time to RX_CLK rising edge	t_{TRRDX}	1.0	—	—	ns	—

A timing diagram for TBI receive appears in Figure 21.

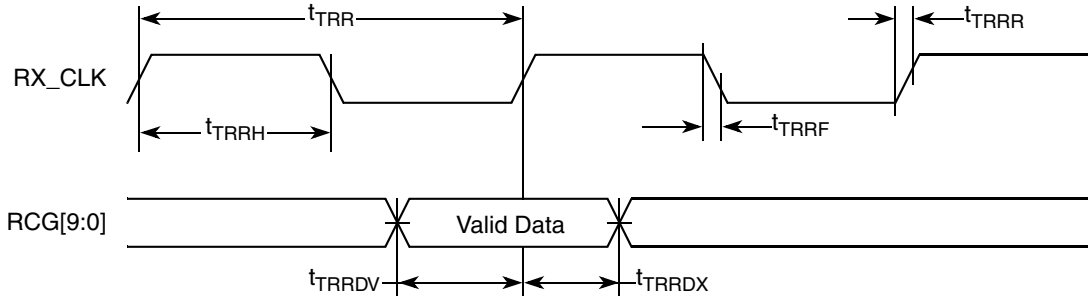

Figure 21. TBI Single-Clock Mode Receive AC Timing Diagram

8.7.4 RGMII and RTBI AC Timing Specifications

Table 37 presents the RGMII and RTBI AC timing specifications.

Table 37. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.8	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—

Table 37. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by design.

Figure 22 shows the RGMII and RTBI AC timing and multiplexing diagrams.

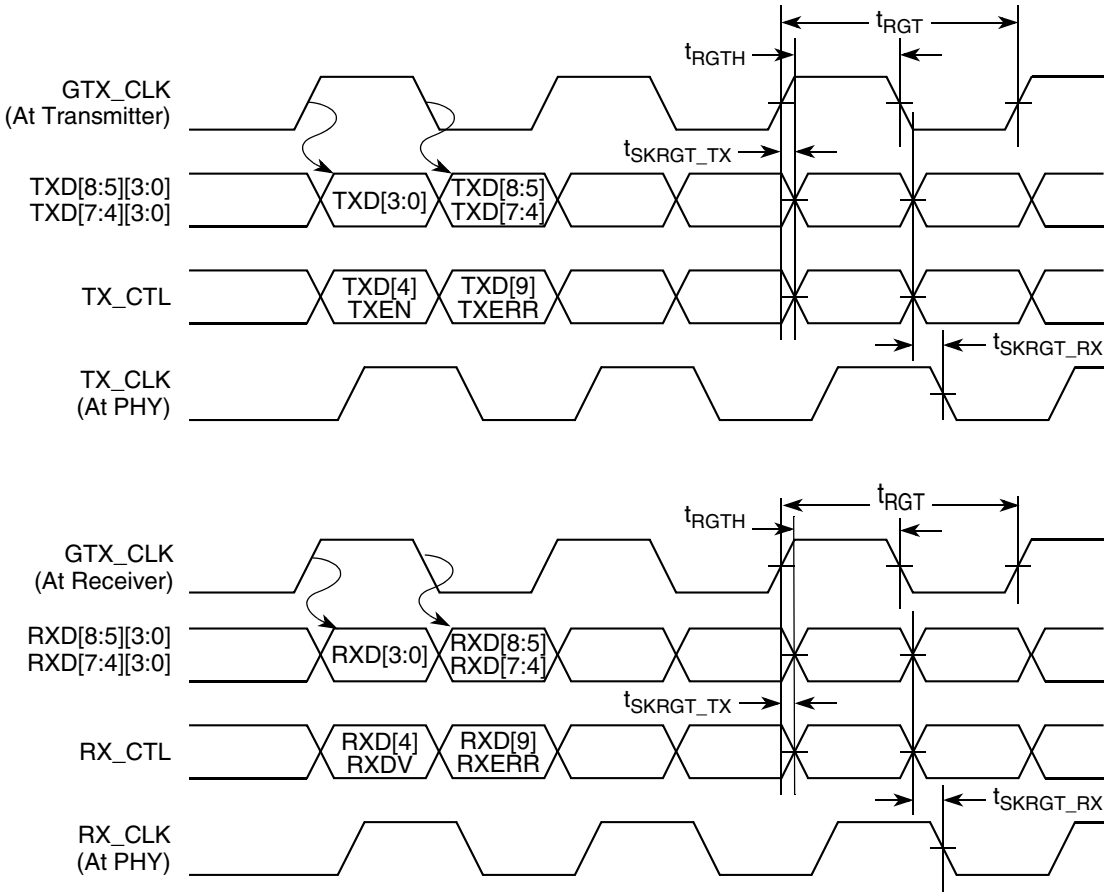

Figure 22. RGMII and RTBI AC Timing and Multiplexing Diagrams

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8544E.

10.1 Local Bus DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 3.3 V DC.

Table 42. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	BV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (BV_{IN} = 0 V or BV_{IN} = BOV_{DD})	I_{IN}	—	±5	μA	1
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1 and Table 2.

Table 43 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 2.5 V DC.

Table 43. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	1.70	BV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.7	V	—
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±15	μA	1
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:
1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1 and Table 2.

Table 44 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 1.8 V DC.

Table 44. Local Bus DC Electrical Characteristics (1.8 V DC)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	1.3	BV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.6	V	—
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±15	μA	1

Table 44. Local Bus DC Electrical Characteristics (1.8 V DC) (continued)

Parameter	Symbol	Min	Max	Unit	Notes
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.45	V	—

10.2 Local Bus AC Electrical Specifications

Table 45 describes the general timing parameters of the local bus interface at BV_{DD} = 3.3 V. For information about the frequency range of local bus see Section 19.1, "Clock Ranges."

Table 45. Local Bus General Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	2.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.85	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.9	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.8	ns	—
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.7	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.7	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5

Table 46. Local Bus General Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

Table 47 describes the general timing parameters of the local bus interface at BV_{DD} = 1.8 V DC.

Table 47. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	2.6	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t_{LBOTOT}	1.2	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	3.2	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	3.2	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	3.2	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.9	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.9	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5

Table 47. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC) (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 1.8-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

Figure 27 provides the AC test load for the local bus.

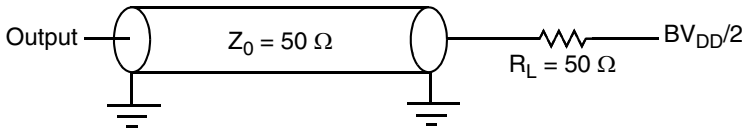

Figure 27. Local Bus AC Test Load

Figure 28 through Figure 33 show the local bus signals.

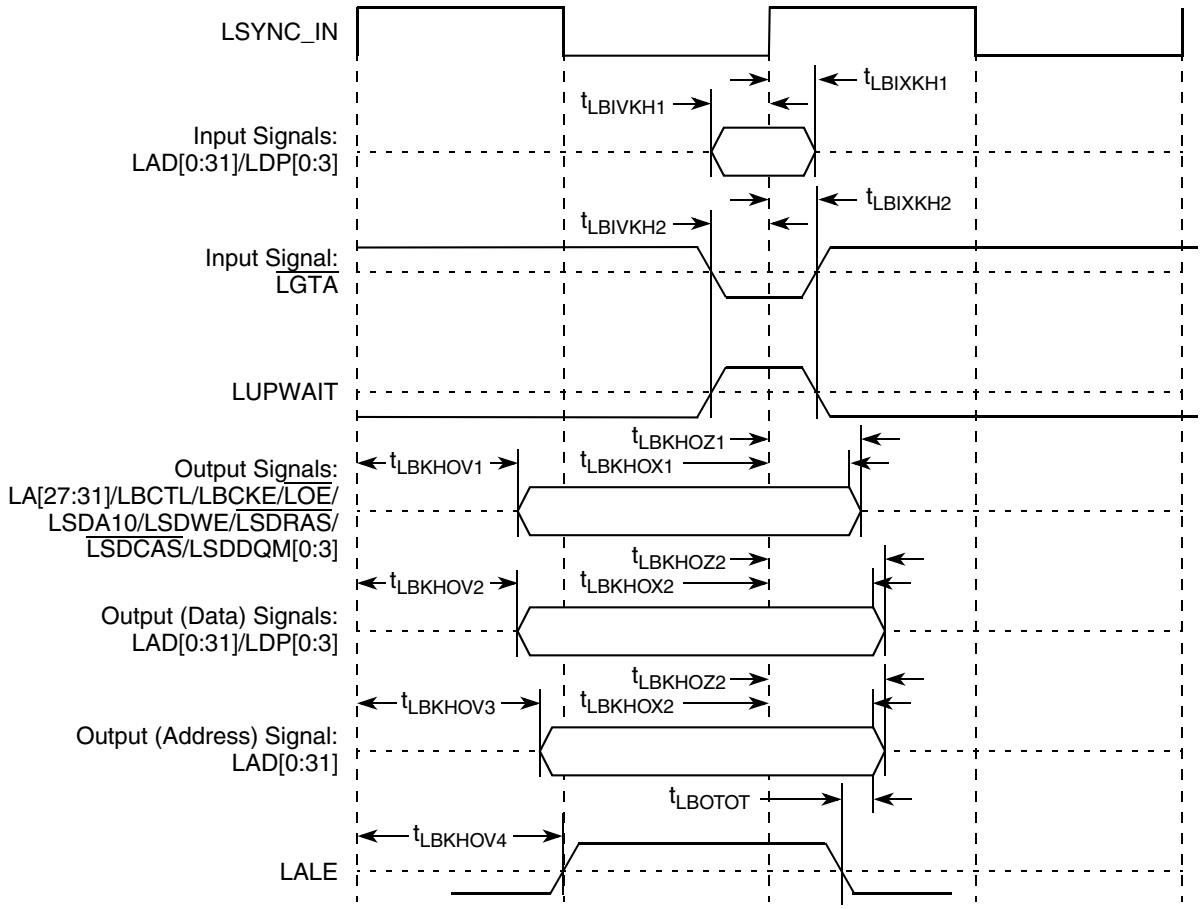

Figure 28. Local Bus Signals (PLL Enabled)

Table 48 describes the general timing parameters of the local bus interface at V_{DD} = 3.3 V DC with PLL disabled.

Table 48. Local Bus General Timing Parameters—PLL Bypassed

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	1.2	4.9	ns	—
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	7.4	—	ns	4, 5
LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	6.75	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	–0.2	—	ns	4, 5
LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	–0.2	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	1.6	ns	—

Figure 38 provides the AC test load for the I^2C.

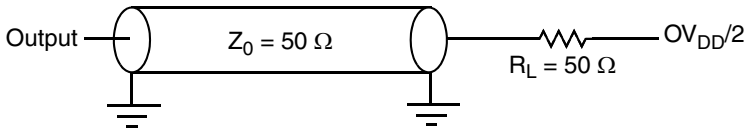

Figure 38. I^2C AC Test Load

Figure 39 shows the AC timing diagram for the I^2C bus.

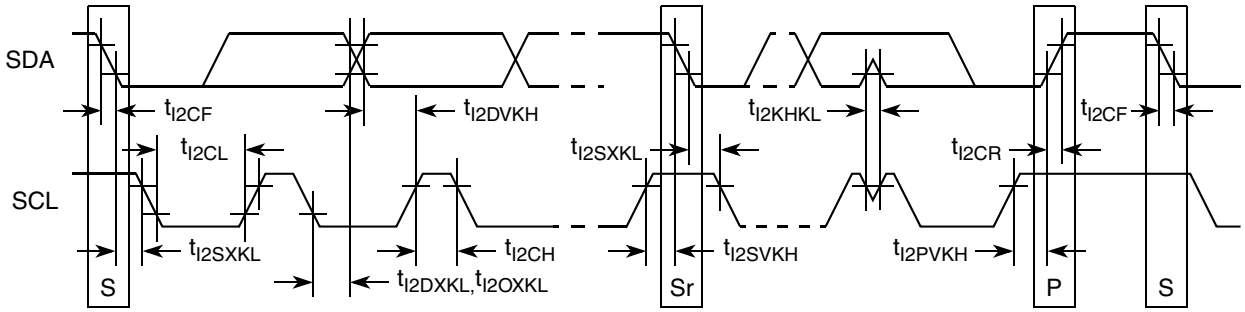

Figure 39. I^2C Bus AC Timing Diagram

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8544E.

14.1 GPIO DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the GPIO interface.

Table 53. GPIO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA	1
High-level output voltage (OV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

Figure 42 shows the PCI input AC timing conditions.

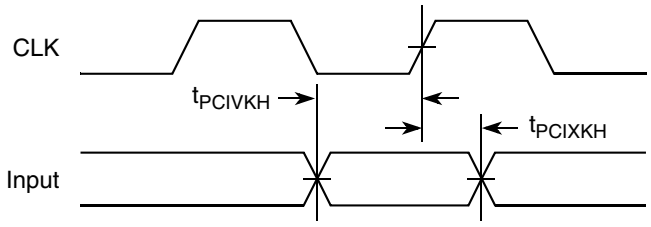

Figure 42. PCI Input AC Timing Measurement Conditions

Figure 43 shows the PCI output AC timing conditions.

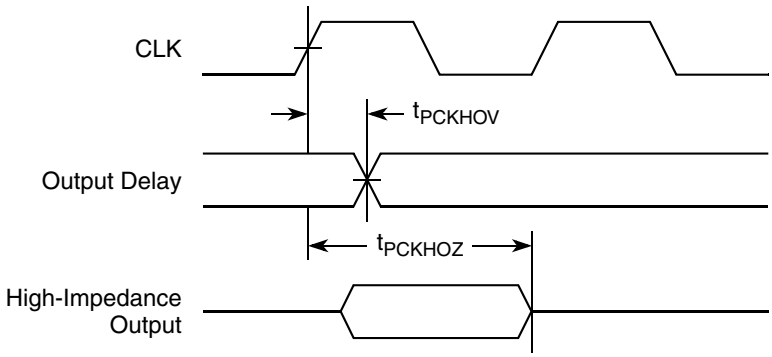

Figure 43. PCI Output AC Timing Measurement Condition

16 High-Speed Serial Interfaces (HSSI)

The MPC8544E features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications.The SerDes1 dedicated for PCI Express data transfers. The SerDes2 can be used for PCI Express and/or SGMII application. This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 44 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8544E SerDes reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

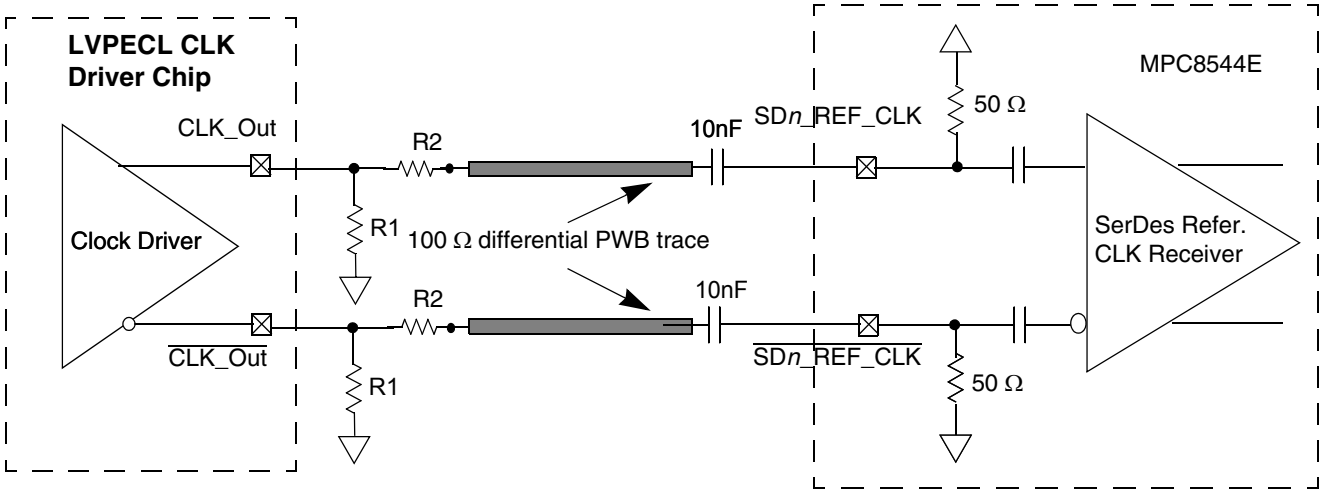

Figure 51. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 52 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8544E SerDes reference clock input's DC requirement.

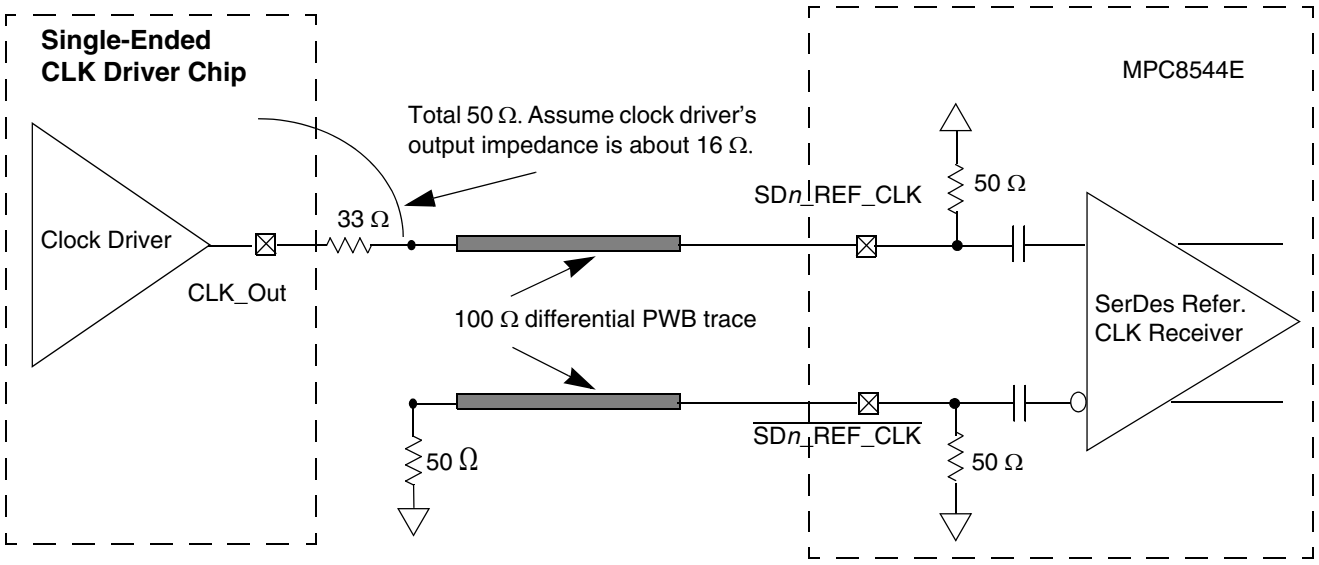

Figure 52. Single-Ended Connection (Reference Only)

Table 59. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}RCV\text{-}DETECT}$	Amount of voltage change allowed during receiver detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.
$V_{TX\text{-}DC\text{-}CM}$	TX DC common mode voltage	0	—	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
$I_{TX\text{-}SHORT}$	TX short circuit current limit	—	—	90	mA	The total current the transmitter can provide when shorted to its ground.
$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum time spent in electrical idle	50	—	—	UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set.
$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical Idle ordered set	—	—	20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from LO.
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Maximum time to transition to valid TX specifications after leaving an electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle.
$RL_{TX\text{-}DIFF}$	Differential return loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$RL_{TX\text{-}CM}$	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance.
$Z_{TX\text{-}DC}$	Transmitter DC impedance	40	—	—	Ω	Required TX D+ as well as D– DC Impedance during all states.
$L_{TX\text{-}SKEW}$	Lane-to-lane output skew	—	—	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single link.
C_{TX}	AC coupling capacitor	75	—	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

Table 60. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$L_{TX-SKEW}$	Total skew	—	—	20	ns	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 58 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 57). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 58). Note that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5-ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 57 is specified using the passive compliance/test measurement load (see Figure 58) in place of any real PCI Express RX component.

In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 58) will be larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 57) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

6.The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 19.2, "CCB/SYSCLK PLL Ratio."

7.The value of LALE, LGPL2, and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 19.3, "e500 Core PLL Ratio."

8.Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. Therefore, this pin will be described as an I/O for boundary scan.

9.For proper state of these signals during reset, $\overline{\text{DMA\_DACK}}$[1] must be pulled down to GND through a resistor. $\overline{\text{DMA\_DACK}}$[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on $\overline{\text{DMA\_DACK}}$[0].

10.This output is actively driven during reset rather than being three-stated during reset.

11.These JTAG pins have weak internal pull-up P-FETs that are always enabled.

12.These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.

13.Anode and cathode of internal thermal diode.

14.Treat pins AC7, T5, V2, and M7 as spare configuration pins cfg_spare[0:3]. The spare pins are unused POR config pins. It is highly recommended that the customer provide the capability of setting these pins low (that is, pull-down resistor which is not currently stuffed) in order to support new config options should they arise between revisions.

15.If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

16.This pin is only an output in FIFO mode when used as Rx flow control.

17.Do not connect.

18.These are test signals for factory use only and must be pulled up (100 Ω to 1 kΩ) to OV_{DD} for normal machine operation.

19.Independent supplies derived from board V_{DD}.

20.Recommend a pull-up resistor (1 K~) be placed on this pin to OV_{DD}.

21.The following pins must not be pulled down during power-on reset: $\overline{\text{HRESET\_REQ}}$, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], and ASLEEP.

22.This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven.

23.General-purpose POR configuration of user system.

24.When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the address pins as No Connect or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the address pins are not connected to any other PCI device. The PCI block will drive the address pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.

25.MDIC0 is grounded through an 18.2-Ω precision 1% resistor and MDIC1 is connected GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.

26.For SGMII mode.

27.Connect to GND.

28.For systems that boot from a local bus (GPCM)-controlled flash, a pull-up on LGPL4 is required.

International Electronic Research Corporation (IERC)818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI)408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-thermal.com

Tyco Electronics800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering603-635-2800
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Advanced Thermal Solutions, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8544E to function in various environments.

20.3.1 Internal Package Conduction Resistance

For the packaging technology, shown in Table 70, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 61). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

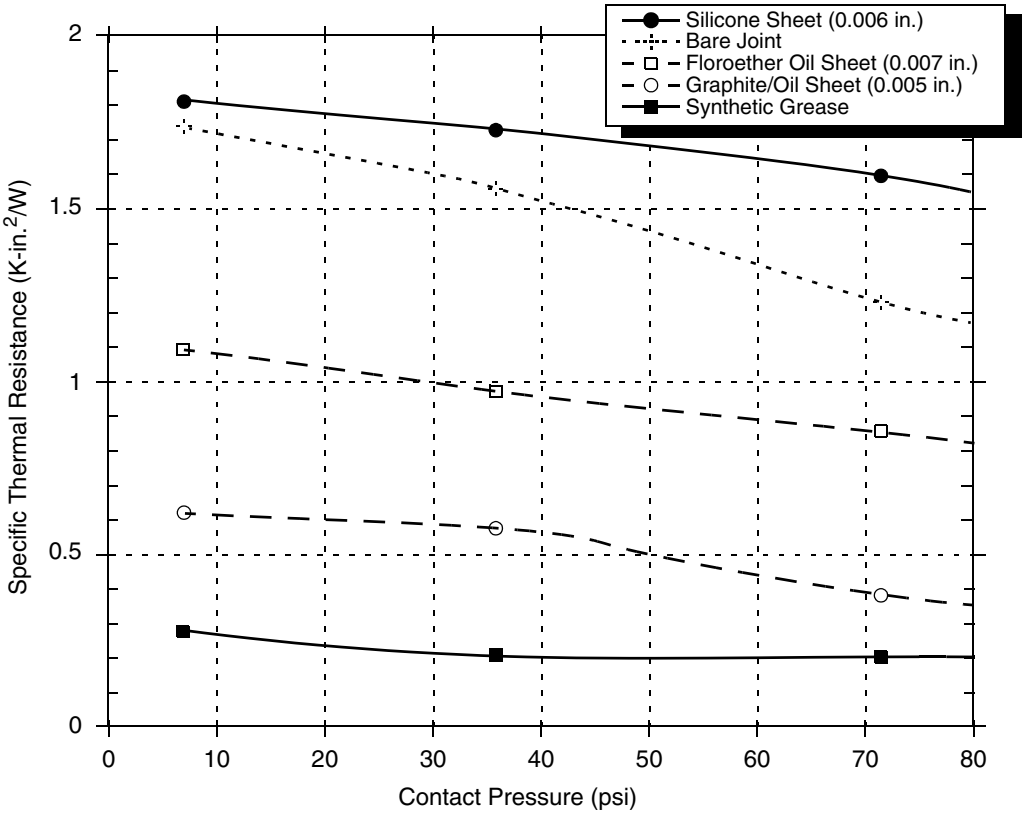

Figure 63. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation800-248-2481
Corporate Center
P.O.Box 999
Midland, MI 48686-0997
Internet: www.dow.com

Shin-Etsu MicroSi, Inc.888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

The Bergquist Company800-347-4572
18930 West 78th St.

Option 2

- If PCI arbiter is disabled during POR,
- All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-kΩ resistor(s).
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-kΩ resistor.

21.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following list shows the termination recommendation:

- For LDP[0:3]: tie them to ground or the power supply rail via a 4.7-kΩ resistor.
- For LPBSE: tie it to the power supply rail via a 4.7-kΩ resistor (pull-up resistor).

22 Device Nomenclature

Ordering information for the parts fully covered by this hardware specifications document is provided in Section 22.3, "Part Marking." Contact your local Freescale sales office or regional marketing team for order information.

22.1 Industrial and Commercial Tier Qualification

The MPC8544E device has been tested to meet the industrial tier qualification. Table 74 provides a description for commercial and industrial qualifications.

Table 74. Commercial and Industrial Description

Tier[1]	Typical Application Use Time	Power-On Hours	Example of Typical Applications
Commercial	5 years	Part-time/ Full-Time	PC's, consumer electronics, office automation, SOHO networking, portable telecom products, PDAs, etc.
Industrial	10 years	Typically Full-Time	Installed telecom equipment, work stations, servers, warehouse equipment, etc.

Note:
1. Refer to Table 2 for operating temperature ranges. Temperature is independent of tier and varies per product.