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Table 2. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Three-speed Ethernet I/O voltage		LV_{DD} (eTSEC1)	3.3 V $\pm$ 165 mV 2.5 V $\pm$ 125 mV	V	4
		TV_{DD} (eTSEC3)	3.3 V $\pm$ 165 mV 2.5 V $\pm$ 125 mV		
PCI, DUART, PCI Express, system control and power management, I ² C, and JTAG I/O voltage		OV_{DD}	3.3 V $\pm$ 165 mV	V	3
Local bus I/O voltage		BV_{DD}	3.3 V $\pm$ 165 mV 2.5 V $\pm$ 125 mV 1.8 V $\pm$ 90 mV	V	5
Input voltage	DDR and DDR2 DRAM signals	MV_{IN}	GND to GV_{DD}	V	2
	DDR and DDR2 DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	2
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	4
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	5
	PCI, Local bus, DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	3
Junction temperature range		T_j	0 to 105	°C	—

Notes:

1. This voltage is the input to the filter discussed in [Section 21.2, “PLL Power Supply Filtering,”](#) and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** T/LV_{IN} must not exceed T/LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution:** BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

4.1 System Clock Timing

Table 5 provides the system clock (SYSCLK) AC timing specifications for the MPC8544E.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	$t_{\text{KH}}, t_{\text{KL}}$	0.6	1.0	2.1	ns	2
SYSCLK duty cycle	$t_{\text{KHK}}/t_{\text{SYSCLK}}$	40	—	60	%	—
SYSCLK jitter	—	—	—	± 150	ps	3, 4

Notes:

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, “CCB/SYSCLK PLL Ratio,” and Section 19.3, “e500 Core PLL Ratio,” for ratio settings.
- Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
- This represents the total input jitter—short- and long-term.
- The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 5 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC8544E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8544E is compatible with spread spectrum sources if the recommendations listed in Table 6 are observed.

Table 6. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Max	Unit	Notes
Frequency modulation	20	60	kHz	—
Frequency spread	0	1.0	%	1

Note:

- SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 5.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

Table 18. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MDQS postamble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/MCK referenced measurements are made from the crossing of the two signals ± 0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except $\overline{MCK}/\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8544E PowerQUICC III Integrated Communications Processor Reference Manual*, for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz.

NOTE

For the ADDR/CMD setup and hold specifications in [Table 18](#), it is assumed that the clock control register is set to adjust the memory clocks by $\frac{1}{2}$ applied cycle.

[Figure 4](#) shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

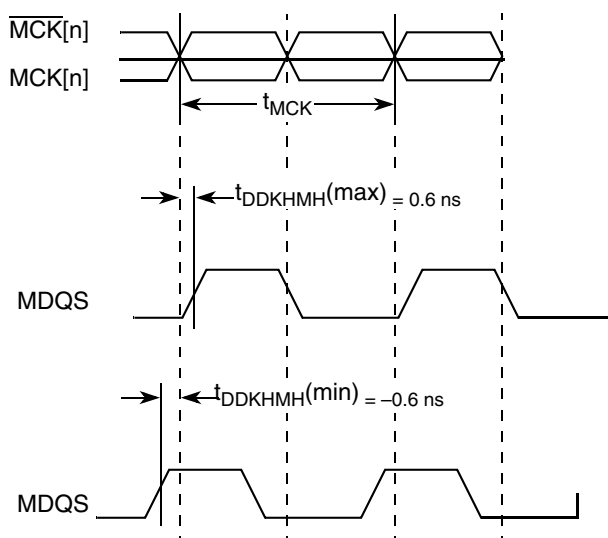

Figure 4. Timing Diagram for t_{DDKHMH}

Table 19. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Low-level output voltage ($OV_{DD} = \min$, $I_{OL} = 2 \text{ mA}$)	V_{OL}	—	0.4	V	—

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

7.2 DUART AC Electrical Specifications

[Table 20](#) provides the AC timing parameters for the DUART interface.

Table 20. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	CCB clock/1,048,576	baud	1
Maximum baud rate	CCB clock/16	baud	2
Oversample rate	16	—	3

Notes:

- CCB clock refers to the platform clock.
- Actual attainable baud rate will be limited by the latency of interrupt processing.
- The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—SGMII/GMII/MII/TBI/RGMII/RTBI/RMII/FIFO Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), 8-bit FIFO interface (FIFO), serial gigabit media independent interface (SGMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The 8-bit FIFO interface can operate at 3.3 or 2.5 V. The RGMII and RTBI interfaces are defined for 2.5 V, while the MII, GMII, TBI, and RMII interfaces can be operated at 3.3 or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The SGMII interfaces follow the *Serial Gigabit Media-Independent Interface (SGMII) Specification Version 1.8*. The electrical characteristics for MDIO and MDC are specified in [Section 9, “Ethernet Management Interface Electrical](#)

Table 25. DC Receiver Electrical Characteristics (continued)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Input differential voltage	LSTS = 0	V_{RX_diffpp}	100	—	1200	mV	2, 4
	LSTS = 1		175	—			
Loss of signal threshold	LSTS = 0	V_{Ios}	30	—	100	mV	3, 4
	LSTS = 1		65	—	175		
Input AC common mode voltage		V_{cm_acpp}	—	—	100	mV	5.
Receiver differential input impedance		Z_{rx_diff}	80	—	120	Ω	—
Receiver common mode input impedance		Z_{rx_cm}	20	—	35	Ω	—
Common mode input voltage		Vcm	xcorevss	—	xcorevss	V	6

Notes:

1. Input must be externally AC-coupled.
2. $V_{RX_DIFFP-p}$ is also referred to as peak-to-peak input differential voltage
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to [Section 17.4.3, "Differential Receiver \(RX\) Input Specifications,"](#) for further explanation.
4. The LSTS shown in this table refers to the LSTSCD bit field of MPC8544E SerDes 2 control register 1.
5. V_{CM_ACP-p} is also referred to as peak-to-peak AC common mode voltage.
6. On-chip termination to SGND_SRDS2 (xcorevss).

8.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{SD2_TX[n]}$) or at the receiver inputs (SD2_RX[n] and $\overline{SD2_RX[n]}$) as depicted in [Figure 10](#), respectively.

8.4.1 SGMII Transmit AC Timing Specifications

[Table 26](#) provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 26. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XVDD_SRDS2 = 1.0 V $\pm$ 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	J_D	—	—	0.17	UI p-p	—
Total jitter	J_T	—	—	0.35	UI p-p	—
Unit interval	U_I	799.92	800	800.08	ps	2
V_{OD} fall time (80%–20%)	t_{fall}	50	—	120	ps	—
V_{OD} rise time (20%–80%)	t_{rise}	50	—	120	ps	—

Notes;

1. Source synchronous clock is not supported.
2. Each UI value is 800 ps $\pm$ 100 ppm.

8.4.2 SGMII Receive AC Timing Specifications

Table 27 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 9 shows the SGMII receiver input compliance mask eye diagram.

Table 27. SGMII Receiver AC Timing Specifications

At recommended operating conditions with XVDD_SRDS2 = 1.0 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Sinusoidal jitter tolerance	J_{sin}	0.1	—	—	UI p-p	1
Total jitter tolerance	J_T	0.65	—	—	UI p-p	1
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit interval	UI	799.92	800	800.08	ps	2
AC coupling capacitor	C_{TX}	5	—	200	nF	3

Notes:

1. Measured at receiver.
2. Each UI value is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It's recommended to be placed near the device transmitter outputs.

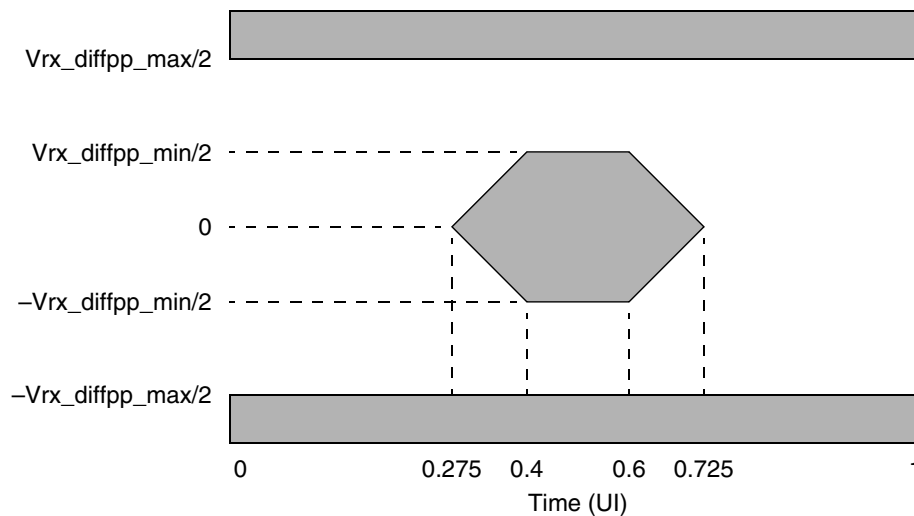


Figure 9. Receive Input Compliance Mask

8.7.1 TBI Transmit AC Timing Specifications

Table 34 provides the TBI transmit AC timing specifications.

Table 34. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V $\pm$ 5% or 2.5 V $\pm$ 5%

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
GTX_CLK to TCG[9:0] delay time	t_{TTKHDV}	0.2	—	5.0	ns	2
GTX_CLK rise (20%–80%)	t_{TTXR}	—	—	1.0	ns	—
GTX_CLK fall time (80%–20%)	t_{TTXF}	—	—	1.0	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Data valid t_{TTKHDV} to GTX_CLK Min setup time is a function of clock period and max hold time (Min setup = cycle time – Max delay).

Figure 19 shows the TBI transmit AC timing diagram.

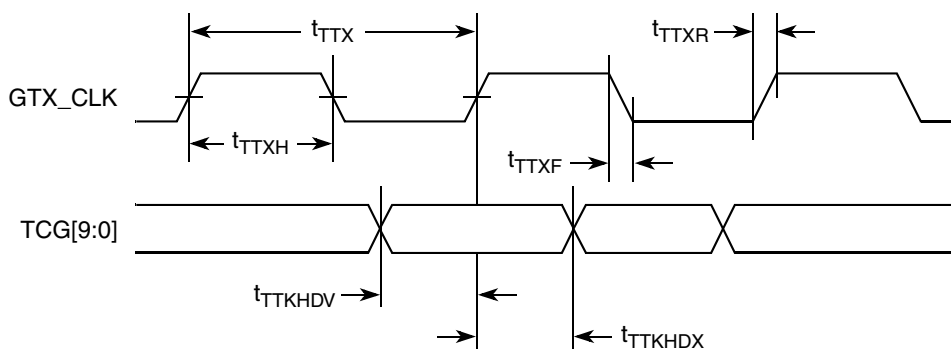


Figure 19. TBI Transmit AC Timing Diagram

8.7.2 TBI Receive AC Timing Specifications

Table 35 provides the TBI receive AC timing specifications.

Table 35. TBI Receive AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V $\pm$ 5% or 2.5 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
PMA_RX_CLK[0:1] clock period	t_{TRX}	—	16.0	—	ns	—
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns	—

12 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8544E.

12.1 JTAG DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the JTAG interface.

Table 49. JTAG DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V	—
Low-level input voltage	V_{IL}	−0.3	0.8	V	—
Input current ($OV_{IN} = 0$ V or $OV_{IN} = OV_{DD}$)	I_{IN}	—	±5	μA	1
High-level output voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2$ mA)	V_{OH}	2.4	—	V	—
Low-level output voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2$ mA)	V_{OL}	—	0.4	V	—

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} .

12.2 JTAG AC Electrical Specifications

Table 50 provides the JTAG AC timing specifications as defined in Figure 34 through Figure 37.

Table 50. JTAG AC Timing Specifications (Independent of SYSCLK)¹

At recommended operating conditions (see Table 3).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times:				ns	4
Boundary-scan data TMS, TDI	t_{JTDVKH} t_{JTIVKH}	4 0	— —		
Input hold times:				ns	4
Boundary-scan data TMS, TDI	t_{JTDXKH} t_{JTIXKH}	20 25	— —		
Valid times:				ns	5
Boundary-scan data TDO	t_{JTKLDV} t_{JTKLOV}	4 4	20 25		
Output hold times:				ns	5
Boundary-scan data TDO	t_{JTKLDX} t_{JTKLOX}	2.5 4	— —		

14.2 GPIO AC Electrical Specifications

Table 54 provides the GPIO input and output AC timing specifications.

Table 54. GPIO Input AC Timing Specifications

Parameter	Symbol	Typ	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Note:

- GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 40 provides the AC test load for the GPIO.

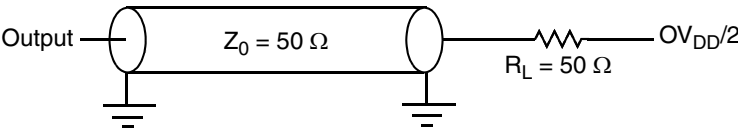


Figure 40. GPIO AC Test Load

15 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8544E.

15.1 PCI DC Electrical Characteristics

Table 55 provides the DC electrical characteristics for the PCI interface.

Table 55. PCI DC Electrical Characteristics ¹

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V	—
Low-level input voltage	V_{IL}	-0.3	0.8	V	—
Input current ($V_{IN} = 0$ V or $V_{IN} = V_{DD}$)	I_{IN}	—	± 5	μA	2
High-level output voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2\text{mA}$)	V_{OH}	2.4	—	V	—
Low-level output voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2$ mA)	V_{OL}	—	0.4	V	—

Notes:

- Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

Figure 42 shows the PCI input AC timing conditions.

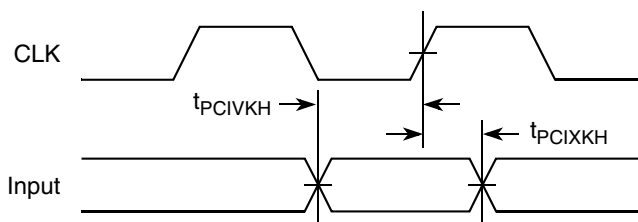


Figure 42. PCI Input AC Timing Measurement Conditions

Figure 43 shows the PCI output AC timing conditions.

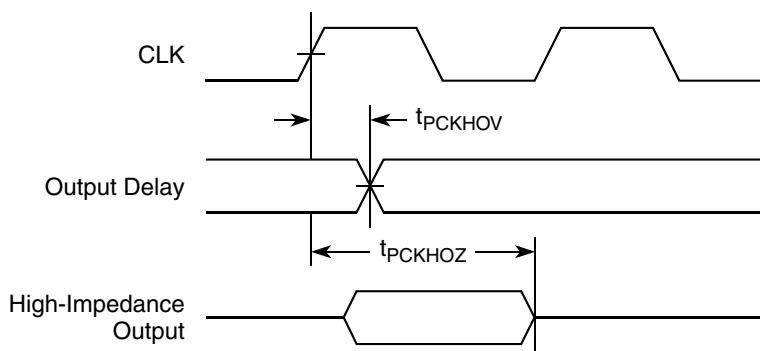


Figure 43. PCI Output AC Timing Measurement Condition

16 High-Speed Serial Interfaces (HSSI)

The MPC8544E features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 dedicated for PCI Express data transfers. The SerDes2 can be used for PCI Express and/or SGMII application. This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 44 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SDn_TX and $\overline{SDn_TX}$) or a receiver input (SDn_RX and $\overline{SDn_RX}$). Each signal swings between A Volts and B Volts where $A > B$.

16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 57 describes some AC parameters common to SGMII, and PCI Express protocols.

Table 57. SerDes Reference Clock Common AC Parameters

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate (SDn_REF_CLK) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus SDn_REF_CLK). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 53.
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for SDn_REF_CLK . It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets SDn_REF_CLK falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SDn_REF_CLK should be compared to the fall edge rate of SDn_REF_CLK , the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 54.

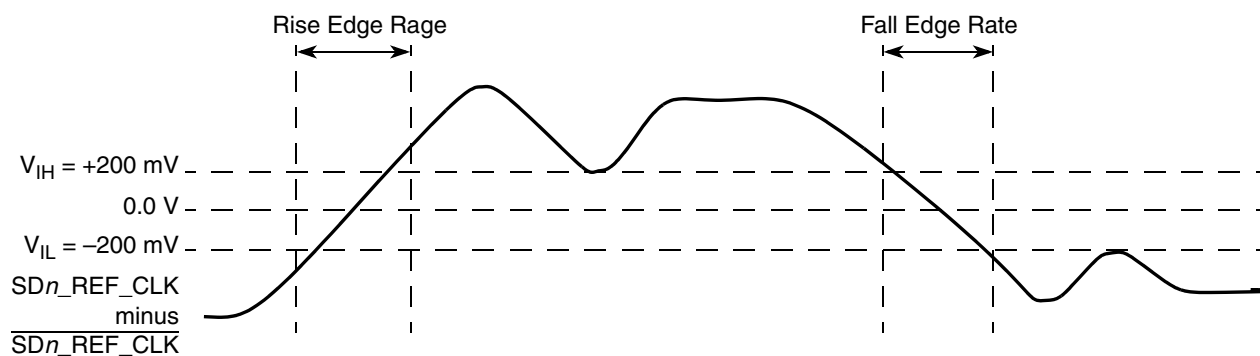


Figure 53. Differential Measurement Points for Rise and Fall Time

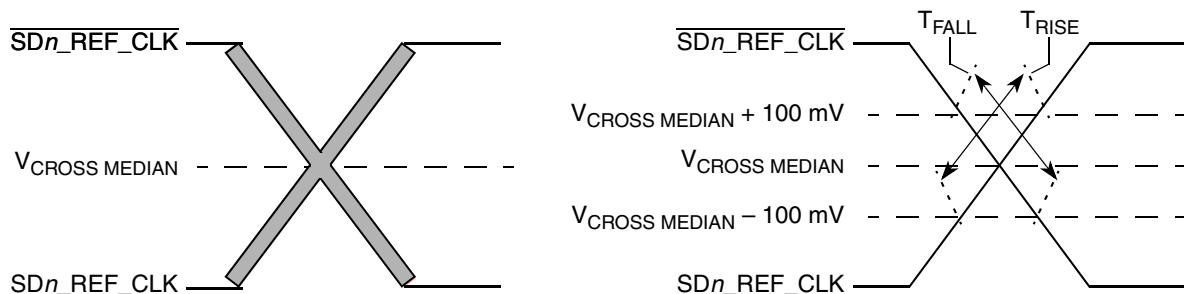


Figure 54. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- [Section 8.3.1, “The DBWO Signal”](#)
- [Section 17.2, “AC Requirements for PCI Express SerDes Clocks”](#)

16.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/SD1_REF_CLK $\bar$ were designed to work with a spread spectrum clock (+0 to –0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/SD2_REF_CLK $\bar$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

16.3 SerDes Transmitter and Receiver Reference Circuits

Figure 55 shows the reference circuits for SerDes data lane’s transmitter and receiver.

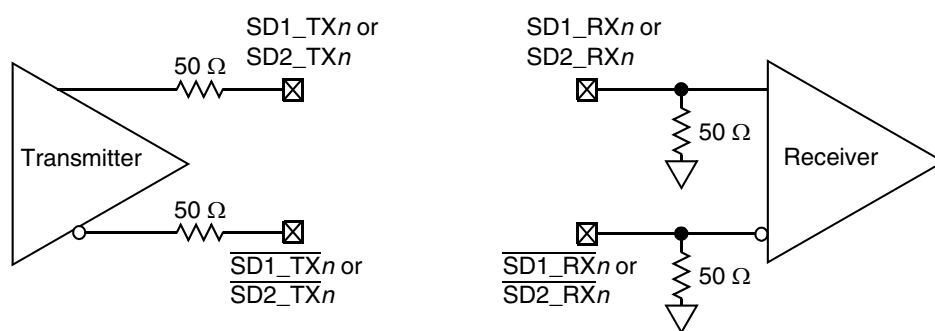


Figure 55. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in the section below (PCI Express or SGMII) in this document based on the application usage:

- [Section 8.3, “SGMII Interface Electrical Characteristics”](#)
- [Section 17, “PCI Express”](#)

Please note that external AC Coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in specification of each protocol section.

Table 60. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7.
$V_{RX-CM-ACp}$	AC peak common mode input voltage	—	—	150	mV	$V_{RX-CM-ACp} = V_{RXD+} - V_{RXD-} \div 2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)} \text{ of } V_{RX-D+} - V_{RX-D-} /2$ See Note 2.
$RL_{RX-DIFF}$	Differential return loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 and –300 mV, respectively. See Note 4.
RL_{RX-CM}	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4.
$Z_{RX-DIFF-DC}$	DC differential input impedance	80	100	120	Ω	RX DC differential mode impedance. See Note 5.
Z_{RX-DC}	DC input impedance	40	50	60	Ω	Required RX D+ as well as D– DC impedance ($50 \pm 20\%$ tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered down DC input impedance	200 k	—	—	Ω	Required RX D+ as well as D– DC impedance when the receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ Measured at the package pins of the receiver.
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	—	—	10	ms	An unexpected electrical idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

18.3 Pinout Listings

Table 62 provides the pinout listing for the MPC8544E 783 FC-PBGA package.

NOTE

The naming convention of TSEC1 and TSEC3 is used to allow the splitting voltage rails for the eTSEC blocks and to ease the port of existing PowerQUICC III software.

NOTE

The $\overline{\text{DMA_DACK}}[0:1]$ and $\overline{\text{TEST_SEL}}$ pins must be set to a proper state during POR configuration. Please refer to Table 62 for more details.

Table 62. MPC8544E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI1_AD[31:0]	AE8, AD8, AF8, AH12, AG12, AB9, AC9, AE9, AD10, AE10, AC11, AB11, AB12, AC12, AF12, AE11, Y14, AE15, AC15, AB15, AA15, AD16, Y15, AB16, AF18, AE18, AC17, AE19, AD19, AB17, AB18, AA16	I/O	OV _{DD}	—
PCI1_C_ $\overline{\text{BE}}$ [3:0]	AC10, AE12, AA14, AD17	I/O	OV _{DD}	—
$\overline{\text{PCI1_GNT}}[4:1]$	AE7, AG11, AH11, AC8	O	OV _{DD}	4, 8, 24
$\overline{\text{PCI1_GNT0}}$	AE6	I/O	OV _{DD}	—
$\overline{\text{PCI1_IRDY}}$	AF13	I/O	OV _{DD}	2
PCI1_PAR	AB14	I/O	OV _{DD}	—
$\overline{\text{PCI1_PERR}}$	AE14	I/O	OV _{DD}	2
$\overline{\text{PCI1_SERR}}$	AC14	I/O	OV _{DD}	2
$\overline{\text{PCI1_STOP}}$	AA13	I/O	OV _{DD}	2
$\overline{\text{PCI1_TRDY}}$	AD13	I/O	OV _{DD}	2
$\overline{\text{PCI1_REQ}}[4:1]$	AF9, AG10, AH10, AD6	I	OV _{DD}	—
$\overline{\text{PCI1_REQ0}}$	AB8	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	—
$\overline{\text{PCI1_DEVSEL}}$	AC13	I/O	OV _{DD}	2
$\overline{\text{PCI1_FRAME}}$	AD12	I/O	OV _{DD}	2
PCI1_IDSEL	AG6	I	OV _{DD}	—

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
AVDD_SRDS	W28	Power for SRDSPLL (1.0 V)	—	19
AVDD_SRDS2	AG1	Power for SRDSPLL (1.0 V)	—	19
SENSEVDD	W11	O	V _{DD}	12
SENSEVSS	W10	—	—	12
Analog Signals				
MVREF	A28	Reference voltage signal for DDR	MVREF	—
SD1_IMP_CAL_RX	M26	—	200Ω to GND	—
SD1_IMP_CAL_TX	AE28	—	100Ω to GND	—
SD1_PLL_TPA	V26	—	AVDD_SRDS ANALOG	17
SD2_IMP_CAL_RX	AH3	I	200 Ω to GND	—
SD2_IMP_CAL_TX	Y1	I	100 Ω to GND	—
SD2_PLL_TPA	AH1	O	AVDD_SRDS2 ANALOG	17
No Connect Pins				
NC	C19, D7, D10, K13, L6, K9, B6, F12, J7, M19, M25, N19, N24, P19, R19, AB19, T12, W3, M12, W5, P12, T19, W1, W7, L13, U19, W4, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V19, W2, W6, W8, T11, U11, W12, W13, W14, W15, W16, W17, W18, W19, W27, V25, Y17, Y18, Y19, AA18, AA19, AB20, AB21, AB22, AB23, J9	—	—	—

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, LCS5/DMA_REQ2 is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as DMA_REQ2.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to OV_{DD}.
3. This pin must always be pulled high.
4. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull-up or active driver is needed. TSEC3_TXD[3] (cfg_srds_sgmii_refclk) is an exception, because the default value of this configuration signal is low (0). Thus, no external pull-down resistor is needed for selecting the default configuration value.
5. Treat these pins as no connects (NC) unless using debug address functionality.

International Electronic Research Corporation (IERC) 818-842-7277
 413 North Moss St.
 Burbank, CA 91502
 Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
 Loroco Sites
 671 East Brokaw Road
 San Jose, CA 95112
 Internet: www.mei-thermal.com

Tyco Electronics 800-522-6752
 Chip Coolers™
 P.O. Box 3668
 Harrisburg, PA 17105-3668
 Internet: www.chipcoolers.com

Wakefield Engineering 603-635-2800
 33 Bridge St.
 Pelham, NH 03076
 Internet: www.wakefield.com

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Advanced Thermal Solutions, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8544E to function in various environments.

20.3.1 Internal Package Conduction Resistance

For the packaging technology, shown in [Table 70](#), the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Chanhassen, MN 55317
 Internet: www.bergquistcompany.com
 Thermagon Inc. 888-246-9050
 4707 Detroit Ave.
 Cleveland, OH 44102
 Internet: www.thermagon.com

20.3.3 Heat Sink Selection Examples

The following section provides a heat sink selection example using one of the commercially available heat sinks.

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_I + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

where

T_J is the die-junction temperature

T_I is the inlet cabinet ambient temperature

T_R is the air temperature rise within the computer cabinet

θ_{JC} is the junction-to-case thermal resistance

θ_{INT} is the adhesive or interface material thermal resistance

θ_{SA} is the heat sink base-to-ambient thermal resistance

P_D is the power dissipated by the device

During operation the die-junction temperatures (T_J) should be maintained within the range specified in [Table 2](#). The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_I) may range from 30° to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (θ_{INT}) may be about 1°C/W. Assuming a T_I of 30°C, a T_R of 5°C, a FC-PBGA package $\theta_{JC} = 0.1$, and a power consumption (P_D) of 5, the following expression for T_J is obtained:

$$\text{Die-junction temperature: } T_J = 30^\circ\text{C} + 5^\circ\text{C} + (0.1^\circ\text{C/W} + 1.0^\circ\text{C/W} + \theta_{SA}) \times P_D$$

The heat sink-to-ambient thermal resistance (θ_{SA}) versus airflow velocity for a Thermalloy heat sink #2328B is shown in [Figure 64](#).

Assuming an air velocity of 1 m/s, we have an effective θ_{SA+} of about 5°C/W, thus

$$T_J = 30^\circ + 5^\circ\text{C} + (0.1^\circ\text{C/W} + 1.0^\circ\text{C/W} + 5^\circ\text{C/W}) \times 5$$

resulting in a die-junction temperature of approximately 66, which is well within the maximum operating temperature of the component.

Note the following:

- AV_{DD_SRDS} should be a filtered version of SV_{DD} .
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8544E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} ; and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types and quantity of bulk capacitors.

21.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least $10 \times 10\text{-nF}$ SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1- μF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10- μF , low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100- μF , low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.

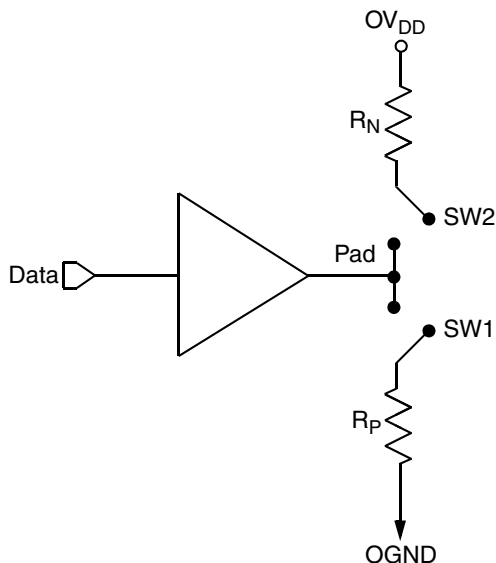


Figure 67. Driver Impedance Measurement

Table 73 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD} , nominal OV_{DD} , 90°C.

Table 73. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	W
R_P	43 Target	25 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table 1.

21.8 Configuration Pin Muxing

The MPC8544E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{HRESET}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{HRESET}$ is asserted, is latched when $\overline{HRESET}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{HRESET}$ (and for platform /system clocks after $\overline{HRESET}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has

22.2 Nomenclature of Parts Fully Addressed by this Document

Table 75 provides the Freescale part numbering nomenclature for the MPC8544E.

Table 75. Device Nomenclature

<i>MPC</i>	<i>nnnn</i>	<i>E</i>	<i>C</i>	<i>HX</i>	<i>AA</i>	<i>X</i>	<i>B</i>
Product Code	Part Identifier	Encryption Acceleration	Temperature Range	Package ¹	Processor Frequency ²	Platform Frequency	Revision Level
MPC	8544	Blank = not included E = included	B or Blank = Industrial Tier standard temp range(0° to 105°C) C = Industrial Tier Extended temp range(–40° to 105°C)	VT = FC-PBGA (lead-free) VJ = lead-free FC-PBGA	AL = 667 MHz AN = 800 MHz AQ = 1000 MHz AR = 1067 MHz	F = 333 MHz G = 400 MHz J = 533 MHz	Blank = Rev. 1.1 1.1.1 A = Rev. 2.1

Notes:

1. See [Section 18, “Package Description,”](#) for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. The VT part number is ROHS-compliant, with the permitted exception of the C4 die bumps.
4. The VJ part number is entirely lead-free. This includes the C4 die bumps.

22.3 Part Marking

Parts are marked as in the example shown in [Figure 70](#).



Notes:

- MMMMM is the 5-digit mask number.
- ATWLYYWW is the traceability code.
- CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 70. Part Marking for FC-PBGA Device