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4.1 System Clock Timing

Table 5 provides the system clock (SYSCLK) AC timing specifications for the MPC8544E.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	$t_{\text{KH}}, t_{\text{KL}}$	0.6	1.0	2.1	ns	2
SYSCLK duty cycle	$t_{\text{KHK}}/t_{\text{SYSCLK}}$	40	—	60	%	—
SYSCLK jitter	—	—	—	± 150	ps	3, 4

Notes:

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, “CCB/SYSCLK PLL Ratio,” and Section 19.3, “e500 Core PLL Ratio,” for ratio settings.
- Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
- This represents the total input jitter—short- and long-term.
- The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 5 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC8544E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8544E is compatible with spread spectrum sources if the recommendations listed in Table 6 are observed.

Table 6. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Max	Unit	Notes
Frequency modulation	20	60	kHz	—
Frequency spread	0	1.0	%	1

Note:

- SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 5.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

Table 12. DDR SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 2.5\text{ V}$ (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output low current ($V_{OUT} = 0.42\text{ V}$)	I_{OL}	16.2	—	mA	—

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
- MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .

Table 13 provides the DDR I/O capacitance when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 13. DDR SDRAM Capacitance for $GV_{DD}(typ) = 2.5\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

- This parameter is sampled. $GV_{DD} = 2.5\text{ V} \pm 0.125\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the current draw characteristics for MV_{REF} .

Table 14. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:

- The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 15 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 15. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.25$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.25$	—	V	—

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 18 provides the output AC timing specifications for the DDR SDRAM interface.

Table 18. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/ $\overline{\text{MCK}}[n]$ crossing	t_{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		—
333 MHz		2.40	—		—
$\overline{\text{MCS}}[n]$ output setup with respect to MCK	t_{DDKHCS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		—
333 MHz		2.40	—		—
$\overline{\text{MCS}}[n]$ output hold with respect to MCK	t_{DDKHCX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		—
333 MHz		2.40	—		—
MCK to MDQS Skew	t_{DDKMHM}	−0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	$t_{\text{DDKHDS}},$ t_{DDKLDS}			ps	5
533 MHz		538	—		7
400 MHz		700	—		—
333 MHz		900	—		—
MDQ/MECC/MDM output hold with respect to MDQS	$t_{\text{DDKHDX}},$ t_{DDKLDX}			ps	5
533 MHz		538	—		7
400 MHz		700	—		—
333 MHz		900	—		—
MDQS preamble	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6

8.4.2 SGMII Receive AC Timing Specifications

Table 27 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 9 shows the SGMII receiver input compliance mask eye diagram.

Table 27. SGMII Receiver AC Timing Specifications

At recommended operating conditions with XVDD_SRDS2 = 1.0 V \pm 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Sinusoidal jitter tolerance	J_{sin}	0.1	—	—	UI p-p	1
Total jitter tolerance	J_T	0.65	—	—	UI p-p	1
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit interval	UI	799.92	800	800.08	ps	2
AC coupling capacitor	C_{TX}	5	—	200	nF	3

Notes:

1. Measured at receiver.
2. Each UI value is 800 ps \pm 100 ppm.
3. The external AC coupling capacitor is required. It's recommended to be placed near the device transmitter outputs.

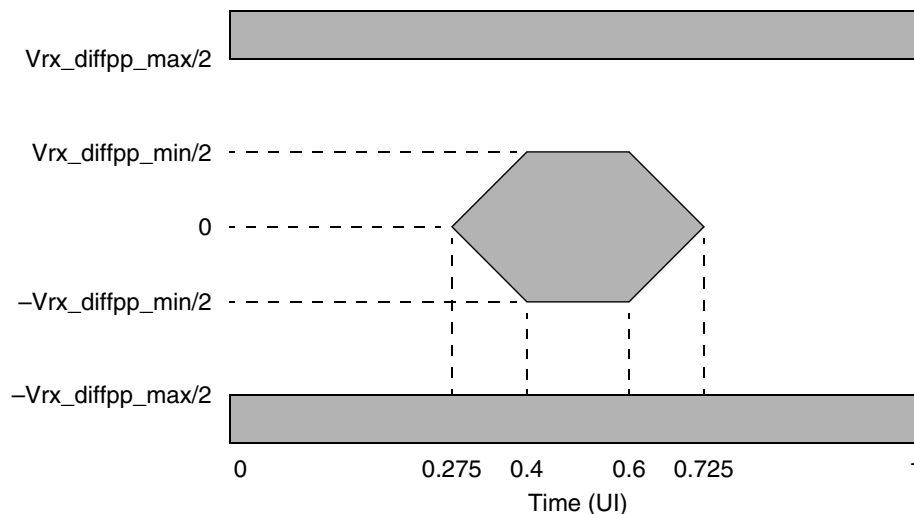


Figure 9. Receive Input Compliance Mask

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in “[Section 8, “Enhanced Three-Speed Ethernet \(eTSEC\), MII Management.”](#)”

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in [Table 40](#).

Table 40. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage (3.3 V)	OV_{DD}	3.135	3.465	V	—
Output high voltage ($OV_{DD} = \text{Min}$, $I_{OH} = -1.0 \text{ mA}$)	V_{OH}	2.10	3.60	V	—
Output low voltage ($OV_{DD} = \text{Min}$, $I_{OL} = 1.0 \text{ mA}$)	V_{OL}	GND	0.50	V	—
Input high voltage	V_{IH}	1.95	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current ($OV_{DD} = \text{Max}$, $V_{IN} = 2.1 \text{ V}$)	I_{IH}	—	40	μA	1
Input low current ($OV_{DD} = \text{Max}$, $V_{IN} = 0.5 \text{ V}$)	I_{IL}	–600	—	μA	—

Note:

1. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

9.2 MII Management AC Electrical Specifications

[Table 41](#) provides the MII management AC timing specifications.

Table 41. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb_clk}) - 3$	—	$(16 \times t_{plb_clk}) + 3$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—

Table 45. Local Bus General Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	—	2.5	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from BV_{DD}/2 of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to 0.4 × BV_{DD} of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.

Table 46 describes the general timing parameters of the local bus interface at BV_{DD} = 2.5 V.

Table 46. Local Bus General Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	12	ns	2
Local bus duty cycle	t _{LBKH} /t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	2.4	—	ns	3, 4
LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.8	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t _{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	2.8	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	2.8	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	2.8	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}	—	2.8	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	—	2.6	ns	5

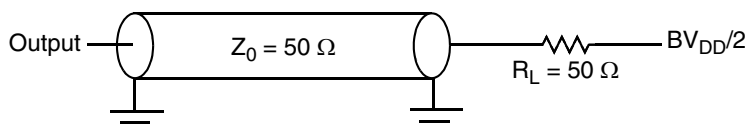
Table 47. Local Bus General Timing Parameters ($BV_{DD} = 1.8 \text{ V DC}$) (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 1.8-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

Figure 27 provides the AC test load for the local bus.


Figure 27. Local Bus AC Test Load

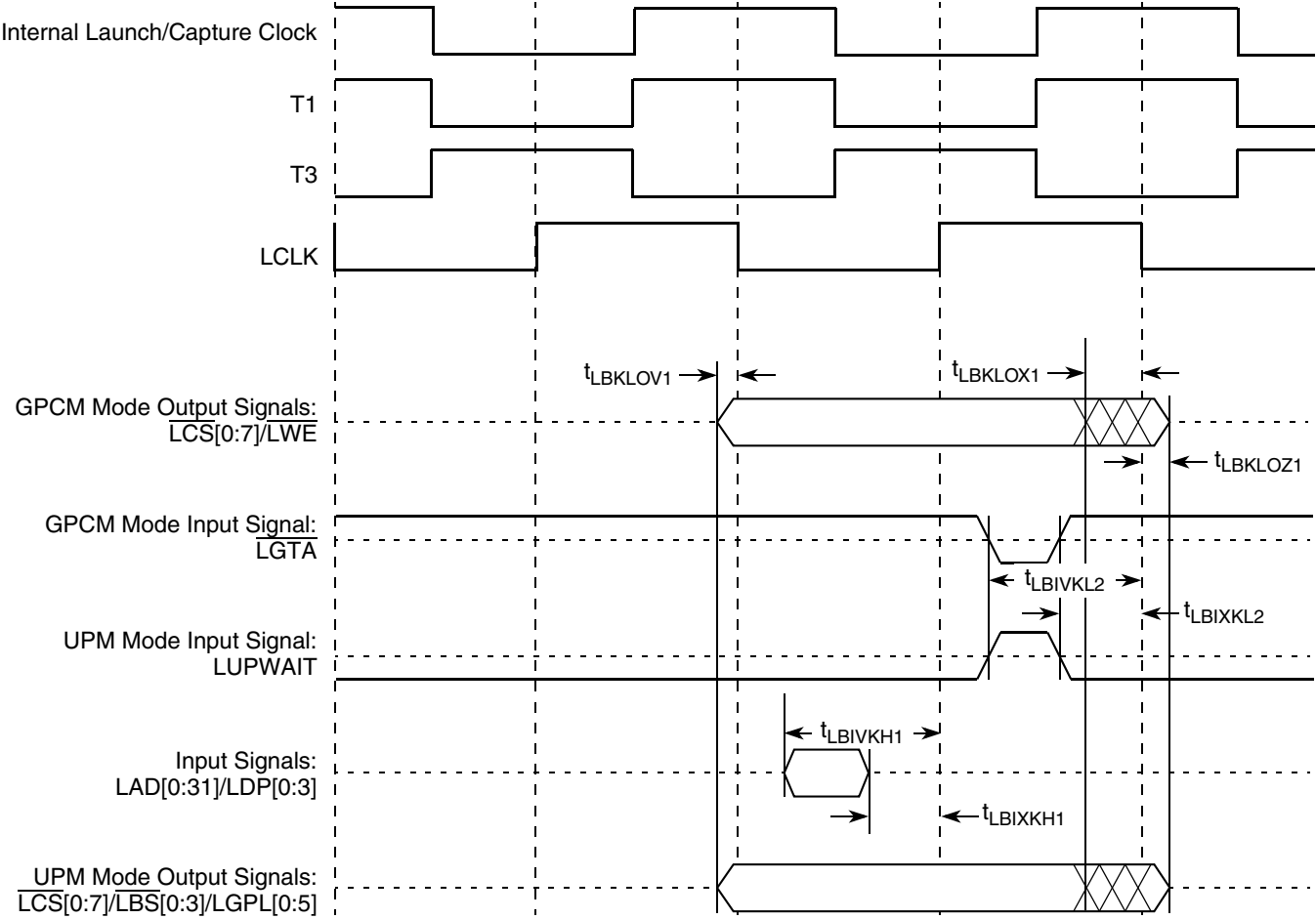


Figure 31. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

Figure 37 provides the boundary-scan timing diagram.

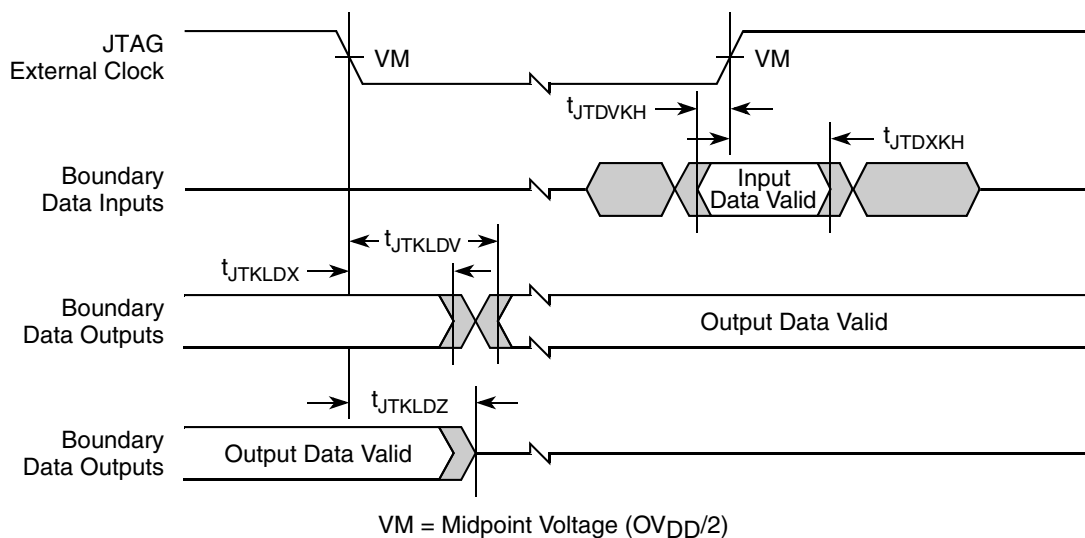


Figure 37. Boundary-Scan Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8544E.

13.1 I²C DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the I²C interfaces.

Table 51. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V _{IH}	0.7 × OV _{DD}	OV _{DD} + 0.3	V	—
Input low voltage level	V _{IL}	−0.3	0.3 × OV _{DD}	V	—
Low level output voltage	V _{OL}	0	0.2 × OV _{DD}	V	1
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between 0.1 × OV _{DD} and 0.9 × OV _{DD} (max))	I _I	−10	10	μA	3
Capacitance for each I/O pin	C _I	—	10	pF	—

Notes:

- Output voltage (open drain or open collector) condition = 3 mA sink current.
- Refer to the *MPC8544E PowerQUICC III Integrated Communications Host Processor Reference Manual* for information on the digital filter used.
- I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

15.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. Table 56 provides the PCI AC timing specifications at 66 MHz.

Table 56. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	—	7.4	ns	2, 3
Output hold from SYSCLK	t_{PCKHOX}	2.0	—	ns	2
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4
Input setup to SYSCLK	t_{PCIVKH}	3.7	—	ns	2, 5
Input hold from SYSCLK	t_{PCIXKH}	0.5	—	ns	2, 5
$\overline{REQ64}$ to \overline{HRESET} ⁹ setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	6, 7
\overline{HRESET} to $\overline{REQ64}$ hold time	t_{PCRHRX}	0	50	ns	7
\overline{HRESET} high to first \overline{FRAME} assertion	t_{PCRHFV}	10	—	clocks	8
Rise time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—
Fall time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
- All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Input timings are measured at the pin.
- The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 19, "Clocking."
- The setup and hold time is with respect to the rising edge of \overline{HRESET} .
- The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
- The reset assertion timing requirement for \overline{HRESET} is 100 μs .

Figure 41 provides the AC test load for PCI.

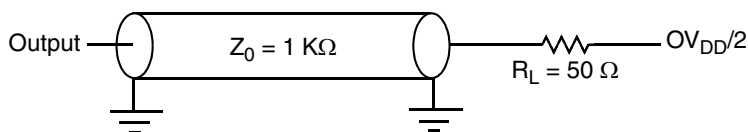


Figure 41. PCI AC Test Load

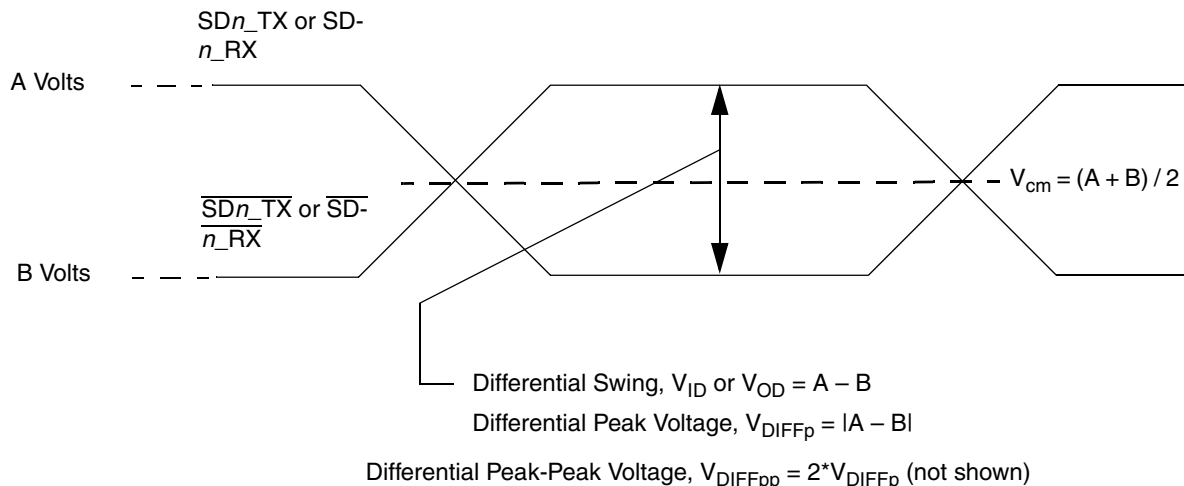


Figure 44. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and \overline{TD} , has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or \overline{TD}) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFpp}) is 1000 mV p-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are $\overline{SD1_REF_CLK}$ and $\overline{SD1_REF_CLK}$ for PCI Express1, PCI Express2. $\overline{SD2_REF_CLK}$, and $\overline{SD2_REF_CLK}$ for the PCI Express3 or SGMII interface, respectively. The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 45 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XV_{DD_SRDS2} are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure
 - The $\overline{SDn_REF_CLK}$ and $\overline{SDn_REF_CLK}$ are internally AC-coupled differential inputs as shown in Figure 45. Each differential clock input ($\overline{SDn_REF_CLK}$ or $\overline{SDn_REF_CLK}$) has a 50- Ω termination to $\overline{SGND_SRDSn}$ (xcorevss) followed by on-chip AC-coupling.
 - The external reference clock driver must be able to drive this termination.

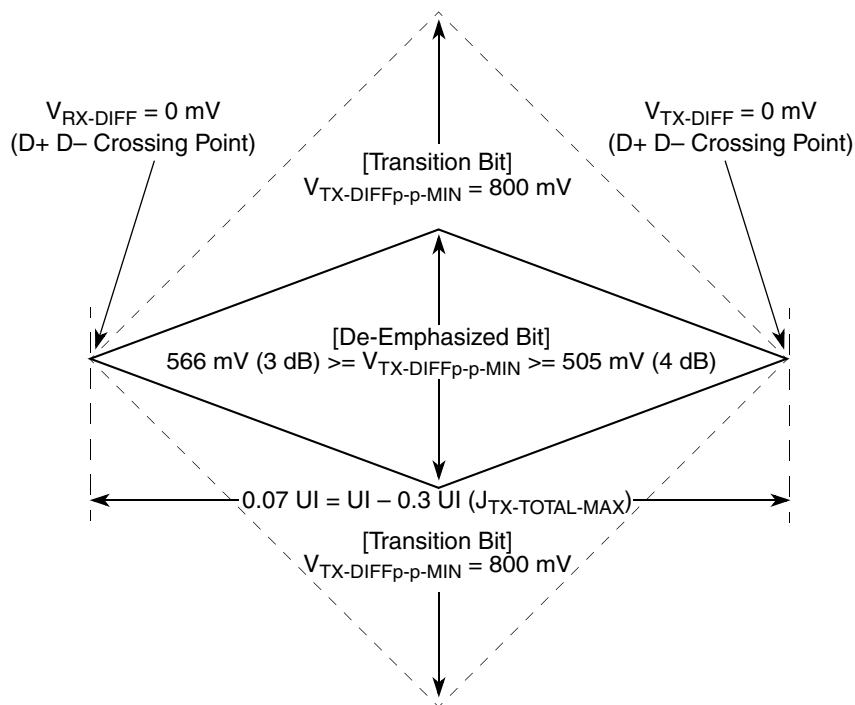


Figure 56. Minimum Transmitter Timing and Voltage Output Compliance Specifications

17.4.3 Differential Receiver (RX) Input Specifications

Table 60 defines the specifications for the differential input at all receivers. The parameters are specified at the component pins.

Table 60. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps \pm 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ See Note 2.
T_{RX-EYE}	Minimum receiver eye width	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.

Table 60. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7.
$V_{RX-CM-ACp}$	AC peak common mode input voltage	—	—	150	mV	$V_{RX-CM-ACp} = V_{RXD+} - V_{RXD-} \div 2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)} \text{ of } V_{RX-D+} - V_{RX-D-} /2$ See Note 2.
$RL_{RX-DIFF}$	Differential return loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 and –300 mV, respectively. See Note 4.
RL_{RX-CM}	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4.
$Z_{RX-DIFF-DC}$	DC differential input impedance	80	100	120	Ω	RX DC differential mode impedance. See Note 5.
Z_{RX-DC}	DC input impedance	40	50	60	Ω	Required RX D+ as well as D– DC impedance ($50 \pm 20\%$ tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered down DC input impedance	200 k	—	—	Ω	Required RX D+ as well as D– DC impedance when the receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ Measured at the package pins of the receiver.
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	—	—	10	ms	An unexpected electrical idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

18 Package Description

This section details package parameters, pin assignments, and dimensions.

18.1 Package Parameters for the MPC8544E FC-PBGA

The package parameters for flip chip plastic ball grid array (FC-PBGA) are provided in [Table 61](#).

Table 61. Package Parameters

Parameter	PBGA ¹
Package outline	29 mm × 29 mm
Interconnects	783
Ball pitch	1 mm
Ball diameter (typical)	0.6 mm
Solder ball (Pb-free)	96.5% Sn 3.5% Ag

Note:

1. (FC-PBGA) without a lid.

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Ethernet Management Interface				
EC_MDC	AC7	O	OV _{DD}	4, 8, 14
EC_MDIO	Y9	I/O	OV _{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	T2	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	U10, U9, T10, T9, U8, T8, T7, T6	I	LV _{DD}	—
TSEC1_TXD[7:0]	T5, U5, V5, V3, V2, V1, U2, U1	O	LV _{DD}	4, 8, 14
TSEC1_COL	R5	I	LV _{DD}	—
TSEC1_CRS	T4	I/O	LV _{DD}	16
TSEC1_GTX_CLK	T1	O	LV _{DD}	—
TSEC1_RX_CLK	V7	I	LV _{DD}	—
TSEC1_RX_DV	U7	I	LV _{DD}	—
TSEC1_RX_ER	R9	I	LV _{DD}	4, 8
TSEC1_TX_CLK	V6	I	LV _{DD}	—
TSEC1_TX_EN	U4	O	LV _{DD}	22
TSEC1_TX_ER	T3	O	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_RXD[7:0]	P11, N11, M11, L11, R8, N10, N9, P10	I	LV _{DD}	—
TSEC3_TXD[7:0]	M7, N7, P7, M8, L7, R6, P6, M6	O	LV _{DD}	4, 8, 14
TSEC3_COL	M9	I	LV _{DD}	—
TSEC3_CRS	L9	I/O	LV _{DD}	16
TSEC3_GTX_CLK	R7	O	LV _{DD}	—
TSEC3_RX_CLK	P9	I	LV _{DD}	—
TSEC3_RX_DV	P8	I	LV _{DD}	—
TSEC3_RX_ER	R11	I	LV _{DD}	—
TSEC3_TX_CLK	L10	I	LV _{DD}	—
TSEC3_TX_EN	N6	O	LV _{DD}	22
TSEC3_TX_ER	L8	O	LV _{DD}	4, 8
DUART				
UART_CTS[0:1]	AH8, AF6	I	OV _{DD}	—
UART_RTS[0:1]	AG8, AG9	O	OV _{DD}	—

20.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC8544E implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see [Section 20.3.4, “Temperature Diode,”](#) for more information.

The recommended attachment method to the heat sink is illustrated in [Figure 61](#). The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

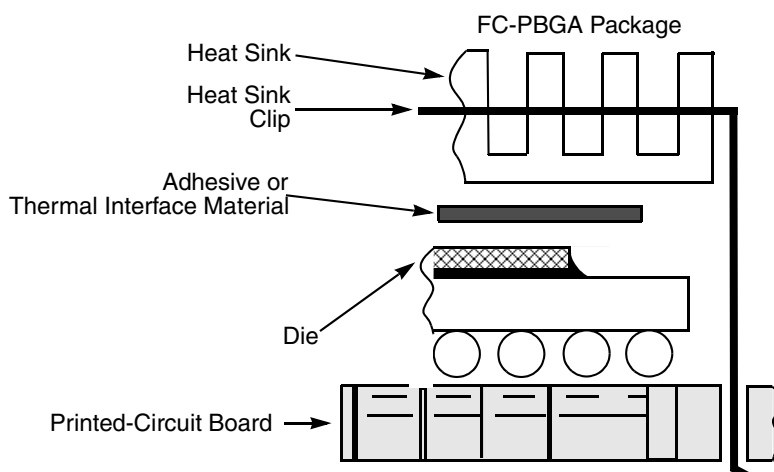


Figure 61. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 603-224-9988

80 Commercial St.

Concord, NH 03301

Internet: www.aavidthermalloy.com

Advanced Thermal Solutions 781-769-2800

89 Access Road #27.

Norwood, MA 02062

Internet: www.qats.com

Alpha Novatech 408-567-8082

473 Sapena Ct. #12

Santa Clara, CA 95054

Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
 413 North Moss St.
 Burbank, CA 91502
 Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
 Loroco Sites
 671 East Brokaw Road
 San Jose, CA 95112
 Internet: www.mei-thermal.com

Tyco Electronics 800-522-6752
 Chip Coolers™
 P.O. Box 3668
 Harrisburg, PA 17105-3668
 Internet: www.chipcoolers.com

Wakefield Engineering 603-635-2800
 33 Bridge St.
 Pelham, NH 03076
 Internet: www.wakefield.com

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Advanced Thermal Solutions, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8544E to function in various environments.

20.3.1 Internal Package Conduction Resistance

For the packaging technology, shown in [Table 70](#), the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 61). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

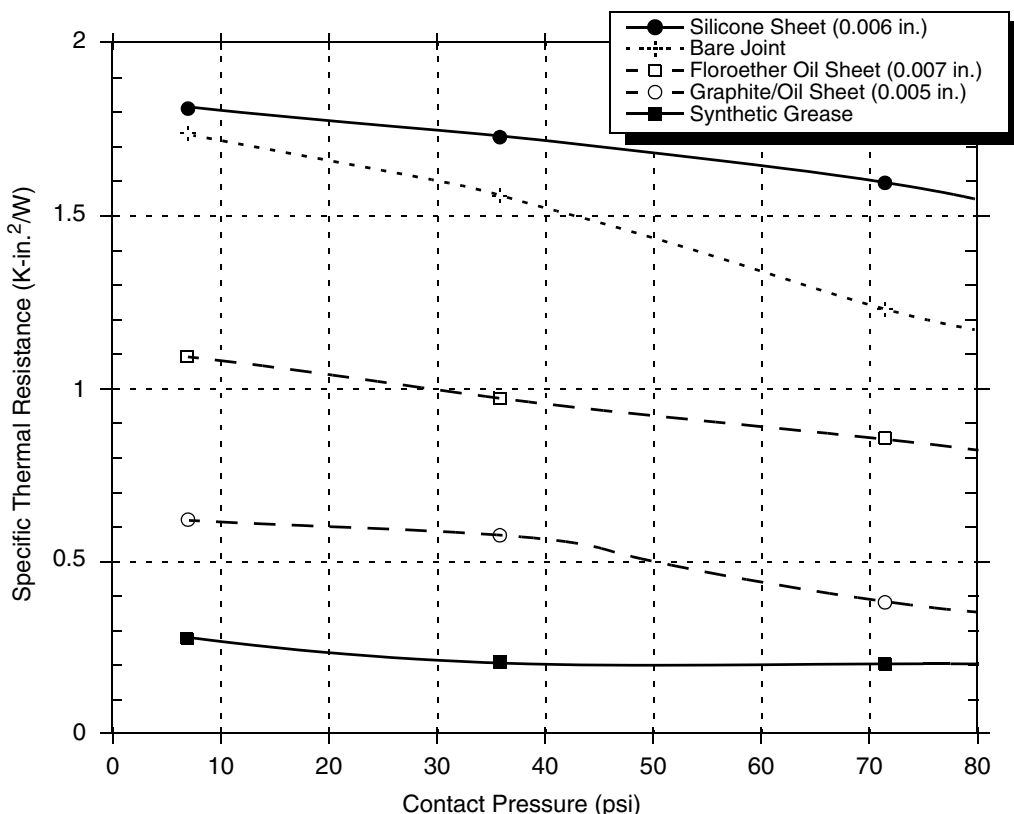


Figure 63. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation 800-248-2481
Corporate Center
P.O. Box 999
Midland, MI 48686-0997
Internet: www.dow.com

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

The Bergquist Company 800-347-4572
18930 West 78th St.

Note the following:

- AV_{DD_SRDS} should be a filtered version of SV_{DD} .
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8544E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} ; and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types and quantity of bulk capacitors.

21.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least $10 \times 10\text{-nF}$ SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1- μF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10- μF , low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100- μF , low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

Option 2

- If PCI arbiter is disabled during POR,
- All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-k Ω resistor(s).
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-k Ω resistor.

21.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following list shows the termination recommendation:

- For LDP[0:3]: tie them to ground or the power supply rail via a 4.7-k Ω resistor.
- For LPBSE: tie it to the power supply rail via a 4.7-k Ω resistor (pull-up resistor).

22 Device Nomenclature

Ordering information for the parts fully covered by this hardware specifications document is provided in [Section 22.3, “Part Marking.”](#) Contact your local Freescale sales office or regional marketing team for order information.

22.1 Industrial and Commercial Tier Qualification

The MPC8544E device has been tested to meet the industrial tier qualification. [Table 74](#) provides a description for commercial and industrial qualifications.

Table 74. Commercial and Industrial Description

Tier ¹	Typical Application Use Time	Power-On Hours	Example of Typical Applications
Commercial	5 years	Part-time/ Full-Time	PC's, consumer electronics, office automation, SOHO networking, portable telecom products, PDAs, etc.
Industrial	10 years	Typically Full-Time	Installed telecom equipment, work stations, servers, warehouse equipment, etc.

Note:

1. Refer to [Table 2](#) for operating temperature ranges. Temperature is independent of tier and varies per product.