



Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8544evtaqga

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



MPC8544E Overview

- Two key (K1, K2, K1) or three key (K1, K2, K3)
- ECB and CBC modes for both DES and 3DES
- AESU—Advanced Encryption Standard unit
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, CTR, and CCM modes
 - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- MDEU—message digest execution unit
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- KEU-Kasumi execution unit
 - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
 - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I^2C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data bus operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
 - Two protocol engines available on a per chip select basis:



MPC8544E Overview

- Broadcast address (accept/reject)
- Hash table match on up to 512 multicast addresses
- Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache
- OCeaN switch fabric
 - Full crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
 - Four-channel controller
 - All channels accessible by both the local and remote masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Support for scatter and gather transfers
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no snoop)
 - Ability to start and flow control each DMA channel from external 3-pin interface
 - Ability to launch DMA from single write transaction
- PCI controller
 - PCI 2.2 compatible
 - One 32-bit PCI port with support for speeds from 16 to 66 MHz
 - Host and agent mode support
 - 64-bit dual address cycle (DAC) support
 - Supports PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses
 - Supports posting of processor-to-PCI and PCI-to-memory writes
 - PCI 3.3-V compatible
 - Selectable hardware-enforced coherency



Figure 1 shows the MPC8544E block diagram.



Figure 1. MPC8544E Block Diagram

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8544E. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 **Overall DC Electrical Characteristics**

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

able 1. Absolute	Maximum	Ratings ¹
------------------	---------	----------------------

Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage	V _{DD}	-0.3 to 1.1	V	—
PLL supply voltage	AV _{DD}	–0.3 to 1.1	V	_
Core power supply for SerDes transceivers	SV _{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers	XV _{DD}	-0.3 to 1.1	V	_

Power Characteristics



3 Power Characteristics

The estimated typical core power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in Table 4.

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V _{DD} (V)	Junction Temperature (°C)	Power (W)	Notes
Typical	667	333	1.0	65	2.6	1, 2
Thermal				105	4.5	1, 3
Maximum					7.15	1, 4
Typical	800	400	1.0	65	2.9	1, 2
Thermal				105	4.8	1, 3
Maximum					7.35	1, 4
Typical	1000	400	1.0	65	3.6	1, 2
Thermal				105	5.3	1, 3
Maximum					7.5	1, 4
Typical	1067	533	1.0	65	3.9	1, 2
Thermal				105	6.0	1, 3
Maximum				105	7.7	1, 4

Table 4. MPC8544ECore Power Dissipation

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.

- Typical power is an average value measured at the nominal recommended core voltage (V_{DD}) and 65°C junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark.
- Thermal power is the average power measured at nominal core voltage (V_{DD}) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark.
- 4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}) and maximum operating junction temperature (see Table 2) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.

4 Input Clocks

This section contains the following subsections:

- Section 4.1, "System Clock Timing"
- Section 4.2, "Real-Time Clock Timing"
- Section 4.3, "eTSEC Gigabit Reference Clock Timing"
- Section 4.4, "Platform to FIFO Restrictions"
- Section 4.5, "Other Input Clocks"



Input Clocks

4.1 System Clock Timing

Table 5 provides the system clock (SYSCLK) AC timing specifications for the MPC8544E.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with $OV_{DD} = 3.3 V \pm 165 mV$.

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
SYSCLK frequency	f _{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t _{SYSCLK}	7.5	—	30.3	ns	_
SYSCLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	2.1	ns	2
SYSCLK duty cycle	t _{KHK} ∕t _{SYSCLK}	40	—	60	%	_
SYSCLK jitter	_	—	—	±150	ps	3, 4

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.

2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.

3. This represents the total input jitter-short- and long-term.

4. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 5 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC8544E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8544E is compatible with spread spectrum sources if the recommendations listed in Table 6 are observed.

Table 6. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Мах	Unit	Notes
Frequency modulation	20	60	kHz	—
Frequency spread	0	1.0	%	1

Note:

1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 5.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.





Table 18. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MDQS postamble	t _{DDKHME}	0.4 x tMCK	0.6 x tMCK	ns	6

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/ \overline{MCK} referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.
- 4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the MPC8544E PowerQUICC III Integrated Communications Processor Reference Manual, for a description and understanding of the timing modifications enabled by use of these bits.
- 5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
- 7. Maximum DDR1 frequency is 400 MHz.

NOTE

For the ADDR/CMD setup and hold specifications in Table 18, it is assumed that the clock control register is set to adjust the memory clocks by $\frac{1}{2}$ applied cycle.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).







Figure 7 shows an example of a 4-wire AC-coupled SGMII serial link connection.



Figure 8 shows an SGMII transmitter DC measurement circuit.



Figure 8. SGMII Transmitter DC Measurement Circuit

Table 25 shows the DC receiver electrical characteristics.

Table 25. DC Receiver Electrical Characteristics

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Supply Voltage	V _{DD_SRDS2}	0.9	1.0	1.05	V	_
DC input voltage range	—			_	—	1



Enhanced Three-Speed Ethernet (eTSEC), MII Management

Table 28. FIFO Mode Transmit AC Timing Specification (continued)

(continued)At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
Fall time TX_CLK (80%–20%)	t _{FITF}	_	—	0.75	ns	—
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t _{FITDX}	0.5	—	3.0	ns	1

Note:

1. Data valid $t_{\ensuremath{\mathsf{FITDV}}}$ to GTX_CLK Min setup time is a function of clock period and max hold time.

(Min setup = Cycle time - Max hold).

Table 29. FIFO Mode Receive AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
RX_CLK clock period	t _{FIR}	—	8.0	—	ns	—
RX_CLK duty cycle	t _{FIRH} /t _{FIRH}	45	50	55	%	—
RX_CLK peak-to-peak jitter	t _{FIRJ}	—	—	250	ps	—
Rise time RX_CLK (20%–80%)	t _{FIRR}	—	—	0.75	ns	—
Fall time RX_CLK (80%-20%)	t _{FIRF}	—	—	0.75	ns	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{FIRDV}	1.5	—	—	ns	—
RX_CLK to RXD[7:0], RX_DV, RX_ER hold time	t _{FIRDX}	0.5	—	—	ns	—

Timing diagrams for FIFO appear in Figure 11 and Figure 12.



Figure 12. FIFO Receive AC Timing Diagram



Table 33. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V \pm 5%.or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns	—
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns	—
RX_CLK clock rise (20%–80%)	t _{MRXR}	1.0	—	4.0	ns	—
RX_CLK clock fall time (80%–20%)	t _{MRXF}	1.0	—	4.0	ns	

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

Figure 17 provides the AC test load for eTSEC.



Figure 17. eTSEC AC Test Load

Figure 18 shows the MII receive AC timing diagram.



Figure 18. MII Receive AC Timing Diagram

8.7 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.



Table 41. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC fall time	t _{MDHF}	_	_	10	ns	

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

- 2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
- 3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns).
- 4. t_{plb clk} is the platform (CCB) clock.

Figure 26 shows the MII management AC timing diagram.



Figure 26. MII Management Interface Timing Diagram



Local Bus



Figure 30. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)



Local Bus



Figure 32. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)



PCI

15.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. Table 56 provides the PCI AC timing specifications at 66 MHz.

Parameter	Symbol ¹	Min	Max	Unit	Notes
SYSCLK to output valid	t _{PCKHOV}	_	7.4	ns	2, 3
Output hold from SYSCLK	t _{PCKHOX}	2.0	_	ns	2
SYSCLK to output high impedance	t _{PCKHOZ}	_	14	ns	2, 4
Input setup to SYSCLK	t _{PCIVKH}	3.7	_	ns	2, 5
Input hold from SYSCLK	t _{PCIXKH}	0.5	_	ns	2, 5
REQ64 to HRESET ⁹ setup time	t _{PCRVRH}	$10 \times t_{SYS}$	_	clocks	6, 7
HRESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	7
HRESET high to first FRAME assertion	t _{PCRHFV}	10	_	clocks	8
Rise time (20%–80%)	t _{PCICLK}	0.6	2.1	ns	
Fall time (20%–80%)	t _{PCICLK}	0.6	2.1	ns	

Table 56. PCI AC Timin	g Specifications at 66 MHz
------------------------	----------------------------

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub></sub>

- 2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
- 4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Input timings are measured at the pin.
- The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 19, "Clocking."
- 7. The setup and hold time is with respect to the rising edge of HRESET.
- 8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the PCI 2.2 Local Bus Specifications.
- 9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 $\mu\text{s}.$

Figure 41 provides the AC test load for PCI.



Figure 41. PCI AC Test Load



- For external DC-coupled connection, as described in Section 16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV.
 Figure 46 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
- For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDSn. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDSn). Figure 47 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- Single-ended Mode
 - The reference clock can also be single-ended. The SDn_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-peak (from Vmin to Vmax) with SDn_REF_CLK either left unconnected or tied to ground.
 - The SDn_REF_CLK input average voltage must be between 200 and 400 mV. Figure 48 shows the SerDes reference clock input requirement for single-ended signaling mode.
 - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase (SDn_REF_CLK) through the same source impedance as the clock input (SDn_REF_CLK) in use.







18.3 Pinout Listings

Table 62 provides the pinout listing for the MPC8544E 783 FC-PBGA package.

NOTE

The naming convention of TSEC1 and TSEC3 is used to allow the splitting voltage rails for the eTSEC blocks and to ease the port of existing PowerQUICC III software.

NOTE

The DMA_DACK[0:1] and TEST_SEL pins must be set to a proper state during POR configuration. Please refer to Table 62 for more details.

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	PCI			
PCI1_AD[31:0]	AE8, AD8, AF8, AH12, AG12, AB9, AC9, AE9, AD10, AE10, AC11, AB11, AB12, AC12, AF12, AE11, Y14, AE15, AC15, AB15, AA15, AD16, Y15, AB16, AF18, AE18, AC17, AE19, AD19, AB17, AB18, AA16	I/O	OV _{DD}	
PCI1_C_BE[3:0]	AC10, AE12, AA14, AD17	I/O	OV _{DD}	—
PCI1_GNT[4:1]	AE7, AG11,AH11, AC8	0	OV _{DD}	4, 8, 24
PCI1_GNT0	AE6	I/O	OV _{DD}	—
PCI1_IRDY	AF13	I/O	OV _{DD}	2
PCI1_PAR	AB14	I/O	OV _{DD}	—
PCI1_PERR	AE14	I/O	OV _{DD}	2
PCI1_SERR	AC14	I/O	OV _{DD}	2
PCI1_STOP	AA13	I/O	OV _{DD}	2
PCI1_TRDY	AD13	I/O	OV _{DD}	2
PCI1_REQ[4:1]	AF9, AG10, AH10, AD6	I	OV _{DD}	—
PCI1_REQ0	AB8	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	—
PCI1_DEVSEL	AC13	I/O	OV _{DD}	2
PCI1_FRAME	AD12	I/O	OV _{DD}	2
PCI1_IDSEL	AG6	l	OV _{DD}	—

Table 62. MPC8544E Pinout Listing



Signal	Package Pin Number	Pin Type	Power Supply	Notes	
AVDD_SRDS	W28	Power for SRDSPLL (1.0 V)	_	19	
AVDD_SRDS2	AG1	Power for SRDSPLL (1.0 V)	_	19	
SENSEVDD	W11	0	V _{DD}	12	
SENSEVSS	W10	—	_	12	
	Analog Signals				
MVREF	A28	Reference voltage signal for DDR	MVREF	_	
SD1_IMP_CAL_RX	M26	—	200 Ω to GND		
SD1_IMP_CAL_TX	AE28	—	100 Ω to GND	_	
SD1_PLL_TPA	V26		AVDD_SRDS ANALOG	17	
SD2_IMP_CAL_RX	АНЗ	I	200 Ω to GND		
SD2_IMP_CAL_TX	Y1	I	100 Ω to GND		
SD2_PLL_TPA	AH1	0	AVDD_SRDS2 ANALOG	17	
No Connect Pins					
NC	C19, D7, D10, K13, L6, K9, B6, F12, J7, M19, M25, N19, N24, P19, R19, AB19, T12, W3, M12, W5, P12, T19, W1, W7, L13, U19, W4, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V19, W2, W6, W8, T11, U11, W12, W13, W14, W15, W16, W17, W18, W19, W27, V25, Y17, Y18, Y19, AA18, AA19, AB20, AB21, AB22, AB23, J9	_	_	_	

Notes:

1.All multiplexed signals are listed only once and do not re-occur. For example, LCS5/DMA_REQ2 is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as DMA_REQ2.

2. Recommend a weak pull-up resistor (2–10 K Ω) be placed on this pin to OV_{DD}.

3. This pin must always be pulled high.

4. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull-up or active driver is needed. TSEC3_TXD[3] (cfg_srds_sgmii_refclk) is an exception, because the default value of this configuration signal is low (0). Thus, no external pull-down resistor is needed for selecting the default configuration value.

5. Treat these pins as no connects (NC) unless using debug address functionality.



Note the following:

- AV_{DD} SRDS should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8544E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} ; and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μ F (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types and quantity of bulk capacitors.

21.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a $1-\mu F$ ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a $10-\mu$ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a $100-\mu$ F, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.



System Design Information

Figure 69 shows the JTAG interface connection.



Notes:

- 1. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown here.
- 2. Populate this with a 10- Ω resistor for short-circuit/current-limiting protection.
- 3. The KEY location (pin 14) is not physically present on the COP header.
- 4. Although pin 12 is defined as a No Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
- This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed to position B.
- 6. Asserting SRESET causes a machine check interrupt to the e500 core.

Figure 69. JTAG Interface Connection



Device Nomenclature

Option 2

- If PCI arbiter is disabled during POR,
- All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-k Ω resistor(s).
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-k Ω resistor.

21.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following list shows the termination recommendation:

- For LDP[0:3]: tie them to ground or the power supply rail via a 4.7-k Ω resistor.
- For LPBSE: tie it to the power supply rail via a 4.7-k Ω resistor (pull-up resistor).

22 Device Nomenclature

Ordering information for the parts fully covered by this hardware specifications document is provided in Section 22.3, "Part Marking." Contact your local Freescale sales office or regional marketing team for order information.

22.1 Industrial and Commercial Tier Qualification

The MPC8544E device has been tested to meet the industrial tier qualification. Table 74 provides a description for commercial and industrial qualifications.

Tier ¹	Typical Application Use Time	Power-On Hours	Example of Typical Applications
Commercial	5 years	Part-time/ Full-Time	PC's, consumer electronics, office automation, SOHO networking, portable telecom products, PDAs, etc.
Industrial	10 years	Typically Full-Time	Installed telecom equipment, work stations, servers, warehouse equipment, etc.

Table 74. Commercial and Industrial Description

Note:

1. Refer to Table 2 for operating temperature ranges. Temperature is independent of tier and varies per product.



Document Revision History

23 Document Revision History

This table provides a revision history for the MPC8544E hardware specification.

Revision Date Substantive Change(s) 8 09/2015 • In Table 10 and Table 12, removed the output leakage current rows and removed table note 4. 7 06/2014 • In Table 75, "Device Nomenclature," added full Pb-free part code. • In Table 75, "Device Nomenclature," added footnotes 3 and 4. 05/2011 6 Updated the value of t_{JTKLDX} to 2.5 ns from 4ns in Table 50. 5 01/2011 • Updated Table 75. 4 09/2010 • Modified local bus information in Section 1.1, "Key Features," to show max local bus frequency as 133 MHz. Added footnote 28 to Table 62. • Updated solder-ball parameter in Table 61. 11/2009 • Update Section 20.3.4, "Temperature Diode," 3 • Update Table 61 Package Parameters from 95.5%sn to 96.5%sn 2 01/2009 • Update power number table to include 1067 MHz/533 MHz power numbers. Remove Part number tables from Hardware spec. The part numbers are available on Freescale web site product page. Removed I/O power numbers from the Hardware spec. and added the table to bring-up guide application note. • Update t_{DDKHMP}, t_{DDKHME} in Table 18. • Updated RX_CLK duty cycle min, and max value to meet the industry standard GMII duty cycle.

• Update paragraph Section 21.3, "Decoupling Recommendations."

• Update Section 22, "Device Nomenclature," with regards to Commercial Tier.

Update in Table 48 Local Bus General Timing Parameters—PLL Bypassed

Update in Table 18 DDR SDRAM Output AC Timing Specifications tMCK Max value

• In Table 40, removed note 1 and renumbered remaining note.

Improvement to Section 16, "High-Speed Serial Interfaces (HSSI)

• Update Figure 5 DDR Output Timing Diagram.

Update Figure 59 Mechanical Dimensions

Table 76. MPC8544E Document Revision History

1

0

06/2008

04/2008

Initial release.