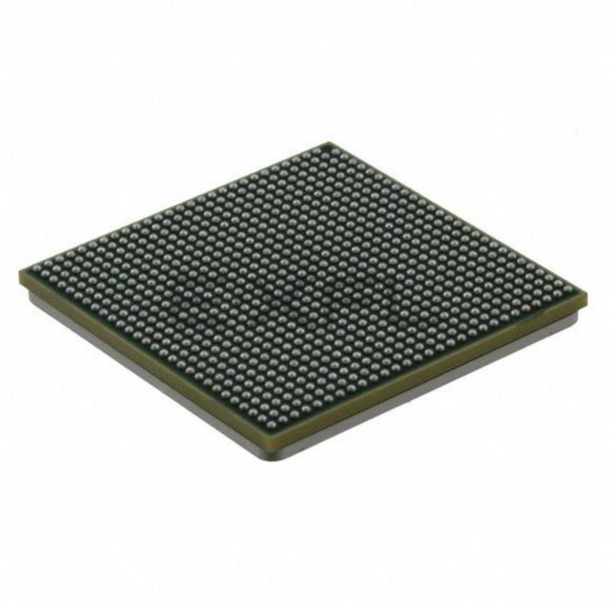
NXP USA Inc. - MPC8544VJAQGA Datasheet



Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544vjaqga

  - Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
  - 36-bit real addressing
  - Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
  - Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte–4-Gbyte page sizes.
  - Enhanced hardware and software debug support
  - Performance monitor facility that is similar to, but separate from, the device performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 256-Kbyte L2 cache/SRAM
  - Flexible configuration
  - Full ECC support on 64-bit boundary in both cache and SRAM modes
  - Cache mode supports instruction caching, data caching, or both.
  - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
    - 1, 2, or 4 ways can be configured for stashing only.
  - Eight-way set-associative cache organization (32-byte cache lines)
  - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
  - Global locking and flash clearing done through writes to L2 configuration registers
  - Instruction and data locks can be flash cleared separately.
  - SRAM features include the following:
    - I/O devices access SRAM regions by marking transactions as snoopable (global).
    - Regions can reside at any aligned location in the memory map.
    - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 36-bit address space.
  - Inbound and outbound ATMUs map to larger external address spaces.
    - Three inbound windows plus a configuration window on PCI and PCI Express
    - Four outbound windows plus default translation for PCI and PCI Express
- DDR/DDR2 memory controller
  - Programmable timing supporting DDR and DDR2 SDRAM
  - 64-bit data interface

  - Two key (K1, K2, K1) or three key (K1, K2, K3)
  - ECB and CBC modes for both DES and 3DES
- AESU—Advanced Encryption Standard unit
  - Implements the Rijndael symmetric key cipher
  - ECB, CBC, CTR, and CCM modes
  - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
  - Implements a stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- MDEU—message digest execution unit
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- KEU—Kasumi execution unit
  - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
  - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications

• Dual I^2C controllers
- Two-wire interface
- Multiple master support
- Master or slave I^2C mode support
- On-chip digital filtering rejects spikes on the bus

• Boot sequencer
- Optionally loads configuration data from serial ROM at reset via the I^2C interface
- Can be used to initialize configuration registers and/or memory
- Supports extended I^2C addressing mode
- Data integrity checked with preamble signature and CRC

• DUART
- Two 4-wire interfaces (SIN, SOUT, $\overline{RTS}$, $\overline{CTS}$)
- Programming model compatible with the original 16450 UART and the PC16550D

• Local bus controller (LBC)
- Multiplexed 32-bit address and data bus operating at up to 133 MHz
- Eight chip selects support eight external slaves
- Up to eight-beat burst transfers
- The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
- Two protocol engines available on a per chip select basis:

Table 1. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Notes
DDR and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage		LV_{DD} (eTSEC1)	–0.3 to 3.63 –0.3 to 2.75	V	—
		TV_{DD} (eTSEC3)	–0.3 to 3.63 –0.3 to 2.75	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR/DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2
	DDR/DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	2
	Local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	V	—
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	2
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	2
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause.
2. (M,L,O)V_{IN}, and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for this device. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.0 ± 50 mV	V	—
PLL supply voltage	AV_{DD}	1.0 ± 50 mV	V	1
Core power supply for SerDes transceivers	SV_{DD}	1.0 ± 50 mV	V	—
Pad power supply for SerDes transceivers	XV_{DD}	1.0 ± 50 mV	V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	2

4.1 System Clock Timing

Table 5 provides the system clock (SYSCLK) AC timing specifications for the MPC8544E.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.1	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	—
SYSCLK jitter	—	—	—	±150	ps	3, 4

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, “CCB/SYSCLK PLL Ratio,” and Section 19.3, “e500 Core PLL Ratio,” for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
3. This represents the total input jitter—short- and long-term.
4. The SYSCLK driver’s closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 5 considers short-term (cycle-to-cycle) jitter only and the clock generator’s cycle-to-cycle output jitter should meet the MPC8544E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8544E is compatible with spread spectrum sources if the recommendations listed in Table 6 are observed.

Table 6. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Max	Unit	Notes
Frequency modulation	20	60	kHz	—
Frequency spread	0	1.0	%	1

Note:
1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 5.

It is imperative to note that the processor’s minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

4.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8544E. Table 8 provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 8. RESET Initialization Timing Specifications[1]

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HREST}}$	100	—	µs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Note:
1. SYSCLK is the primary clock input for the MPC8544E.

Table 9 provides the PLL lock times.

Table 9. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
Core and platform PLL lock times	—	100	µs	—
Local bus PLL	—	50	µs	—
PCI bus lock time	—	50	µs	—

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8544E. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

Table 18. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQS postamble	t_{DDKHME}	0.4 x tMCK	0.6 x tMCK	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8544E PowerQUICC III Integrated Communications Processor Reference Manual,* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz.

NOTE

For the ADDR/CMD setup and hold specifications in Table 18, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

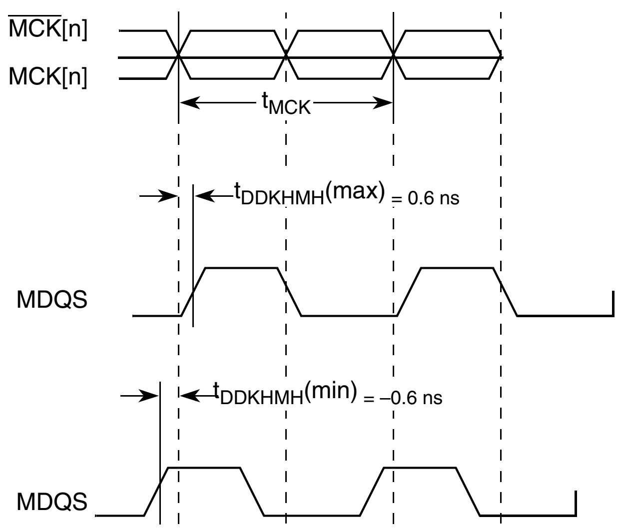


Figure 4. Timing Diagram for t_{DDKHMH}

Table 28. FIFO Mode Transmit AC Timing Specification (continued)

(continued)At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
Fall time TX_CLK (80%–20%)	t_{FITF}	—	—	0.75	ns	—
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5	—	3.0	ns	1

Note:

1. Data valid t_{FITDV} to GTX_CLK Min setup time is a function of clock period and max hold time. (Min setup = Cycle time – Max hold).

Table 29. FIFO Mode Receive AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
RX_CLK clock period	t_{FIR}	—	8.0	—	ns	—
RX_CLK duty cycle	t_{FIRH}/t_{FIRH}	45	50	55	%	—
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps	—
Rise time RX_CLK (20%–80%)	t_{FIRR}	—	—	0.75	ns	—
Fall time RX_CLK (80%–20%)	t_{FIRF}	—	—	0.75	ns	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	—	—	ns	—
RX_CLK to RXD[7:0], RX_DV, RX_ER hold time	t_{FIRDX}	0.5	—	—	ns	—

Timing diagrams for FIFO appear in Figure 11 and Figure 12.

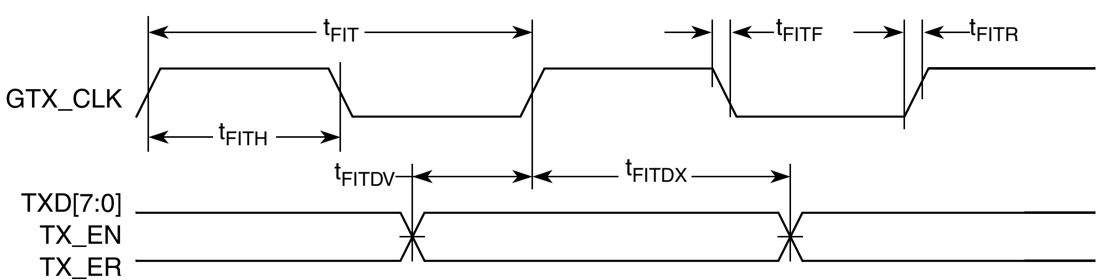


Figure 11. FIFO Transmit AC Timing Diagram

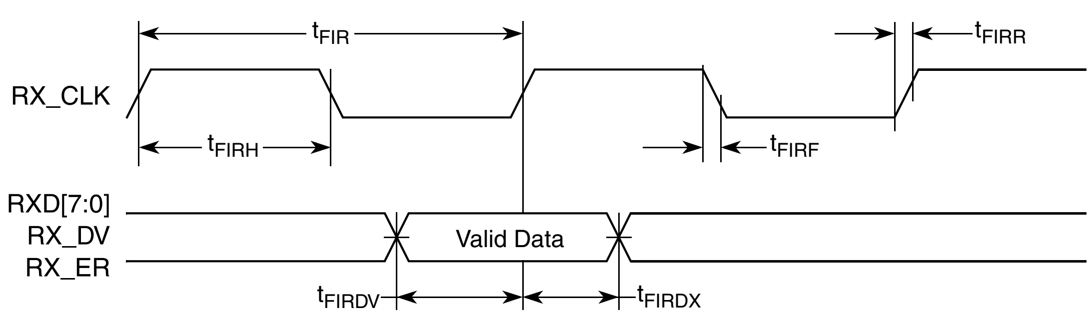


Figure 12. FIFO Receive AC Timing Diagram

8.7.1 TBI Transmit AC Timing Specifications

Table 34 provides the TBI transmit AC timing specifications.

Table 34. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
GTX_CLK to TCG[9:0] delay time	t_{TTKHDX}	0.2	—	5.0	ns	2
GTX_CLK rise (20%–80%)	t_{TTXR}	—	—	1.0	ns	—
GTX_CLK fall time (80%–20%)	t_{TTXF}	—	—	1.0	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state\ )(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Data valid t_{TTKHDV} to GTX_CLK Min setup time is a function of clock period and max hold time (Min setup = cycle time – Max delay).

Figure 19 shows the TBI transmit AC timing diagram.

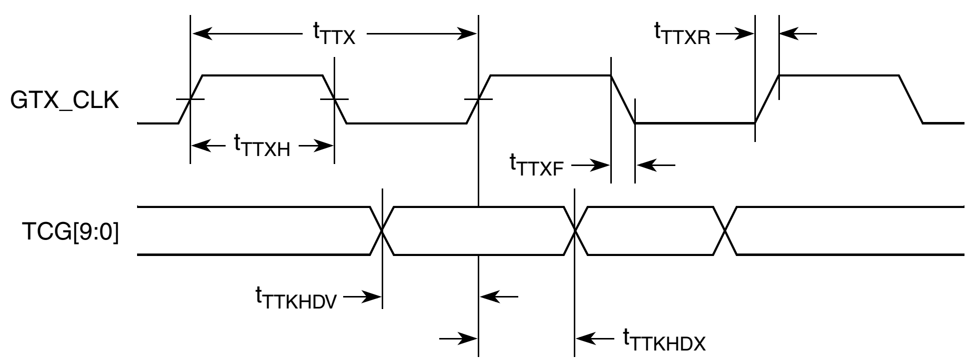


Figure 19. TBI Transmit AC Timing Diagram

8.7.2 TBI Receive AC Timing Specifications

Table 35 provides the TBI receive AC timing specifications.

Table 35. TBI Receive AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
PMA_RX_CLK[0:1] clock period	t_{TRX}	—	16.0	—	ns	—
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns	—

Table 37. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by design.

Figure 22 shows the RGMII and RTBI AC timing and multiplexing diagrams.

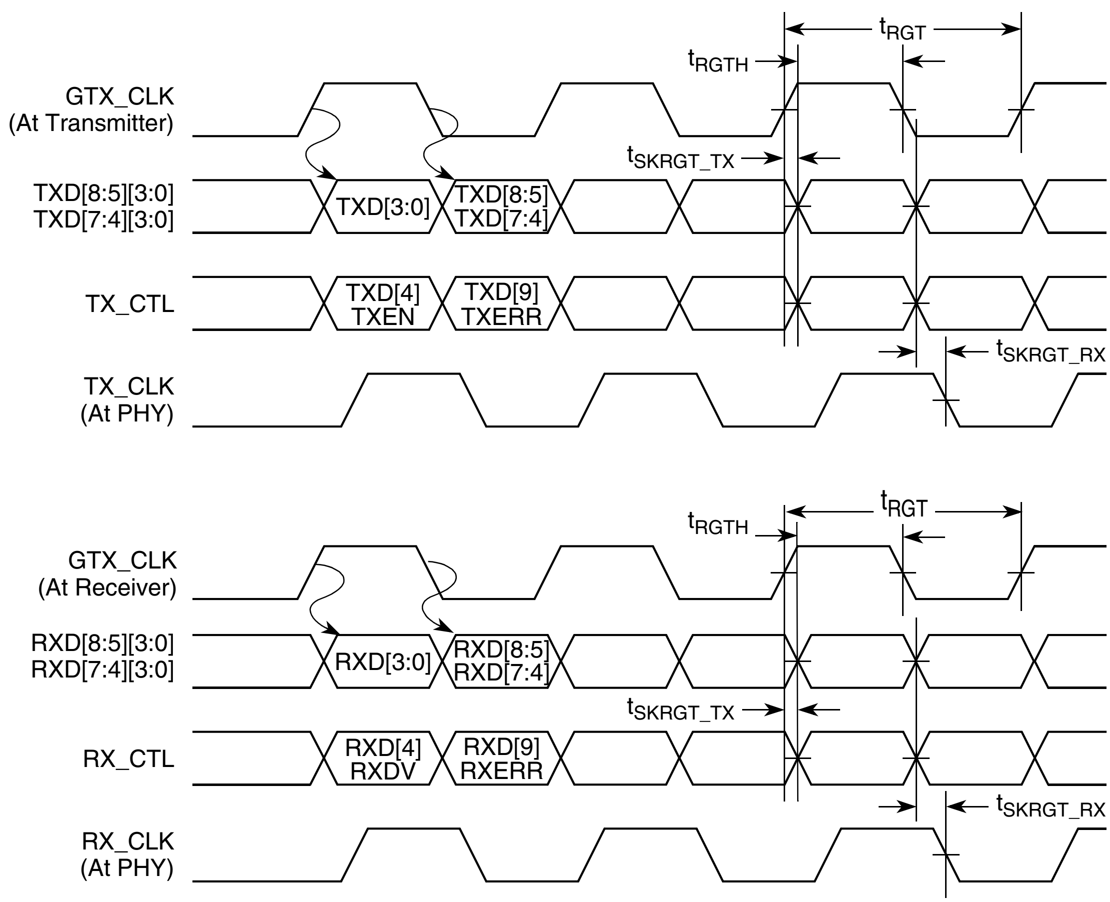


Figure 22. RGMII and RTBI AC Timing and Multiplexing Diagrams

Table 41. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns).
4. t_{plb_clk} is the platform (CCB) clock.

Figure 26 shows the MII management AC timing diagram.

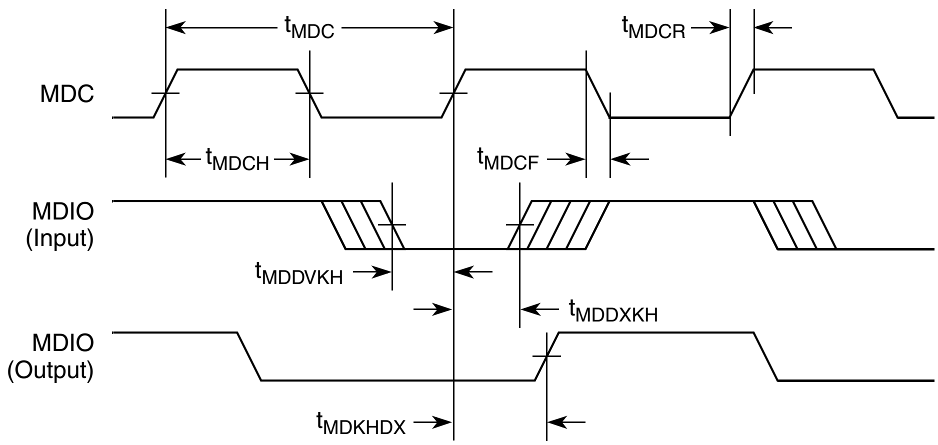


Figure 26. MII Management Interface Timing Diagram

Figure 37 provides the boundary-scan timing diagram.

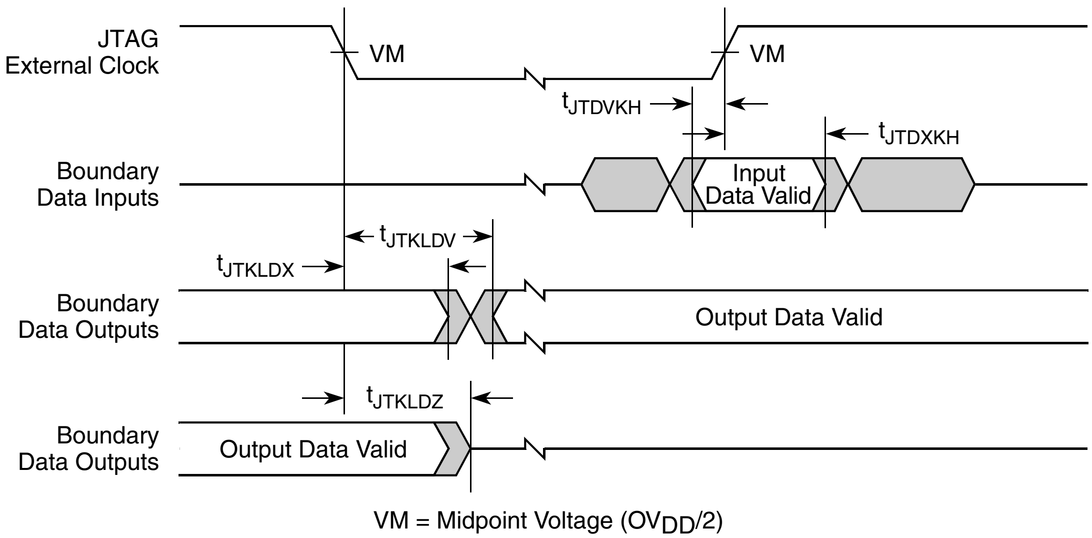


Figure 37. Boundary-Scan Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8544E.

13.1 I²C DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the I²C interfaces.

Table 51. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	0.7 × OV_{DD}	OV_{DD} + 0.3	V	—
Input low voltage level	V_{IL}	–0.3	0.3 × OV_{DD}	V	—
Low level output voltage	V_{OL}	0	0.2 × OV_{DD}	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD}(max)	I_I	–10	10	μA	3
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8544EPowerQUICC III Integrated Communications Host Processor Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

Figure 38 provides the AC test load for the I^2C.

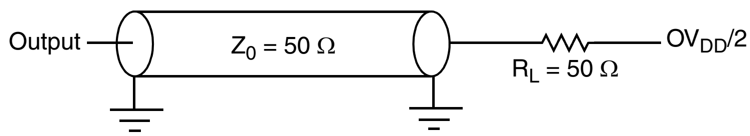


Figure 38. I^2C AC Test Load

Figure 39 shows the AC timing diagram for the I^2C bus.

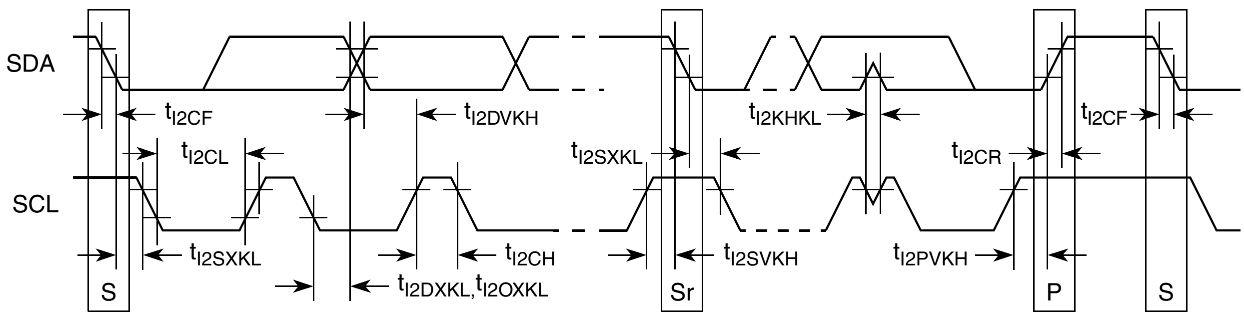


Figure 39. I^2C Bus AC Timing Diagram

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8544E.

14.1 GPIO DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the GPIO interface.

Table 53. GPIO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA	1
High-level output voltage (OV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

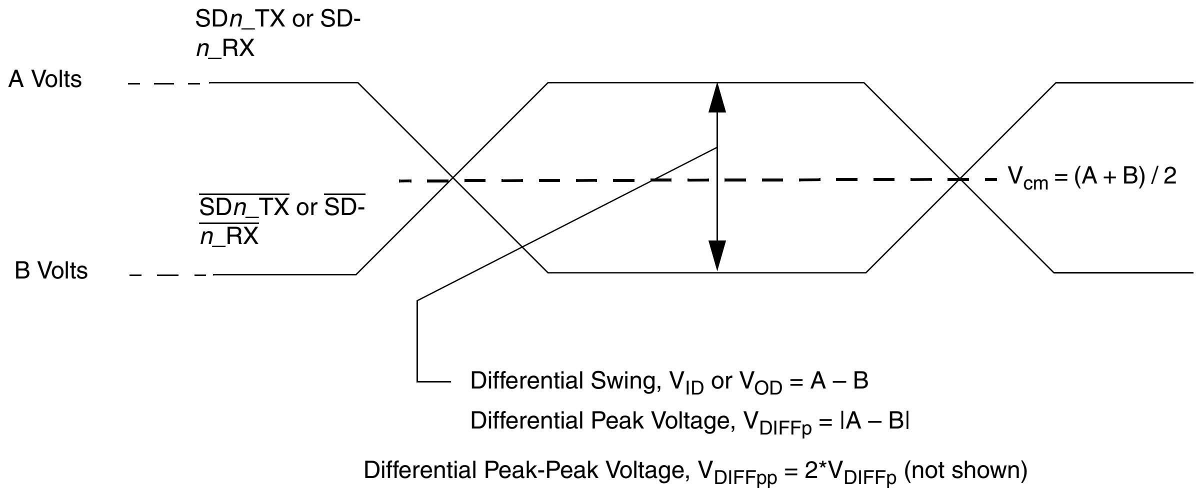


Figure 44. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp\text{-}p}$) is 1000 mV p-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$ for PCI Express1, PCI Express2. SD2_REF_CLK, and $\overline{\text{SD2\_REF\_CLK}}$ for the PCI Express3 or SGMII interface, respectively. The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 45 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XV_{DD_SRDS2} are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure
  - The SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 45. Each differential clock input (SD*n*_REF_CLK or $\overline{\text{SD}n\text{\_REF\_CLK}}$) has a 50-Ω termination to SGND_SRDS*n* (xcorevss) followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.

— The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range:
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  — If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  — This requirement is described in detail in the following sections.

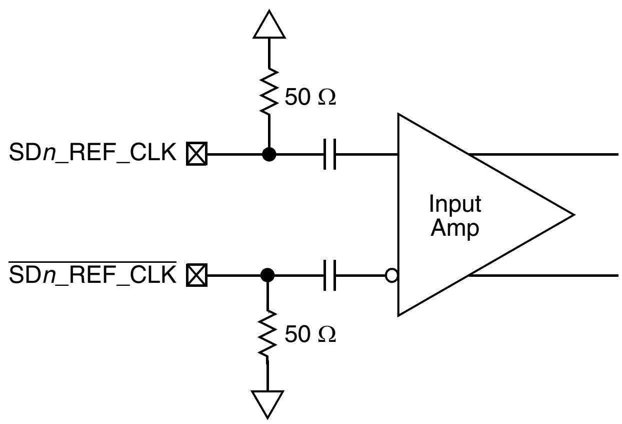


Figure 45. Receiver of SerDes Reference Clocks

16.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8544E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  — The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8544E SerDes reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

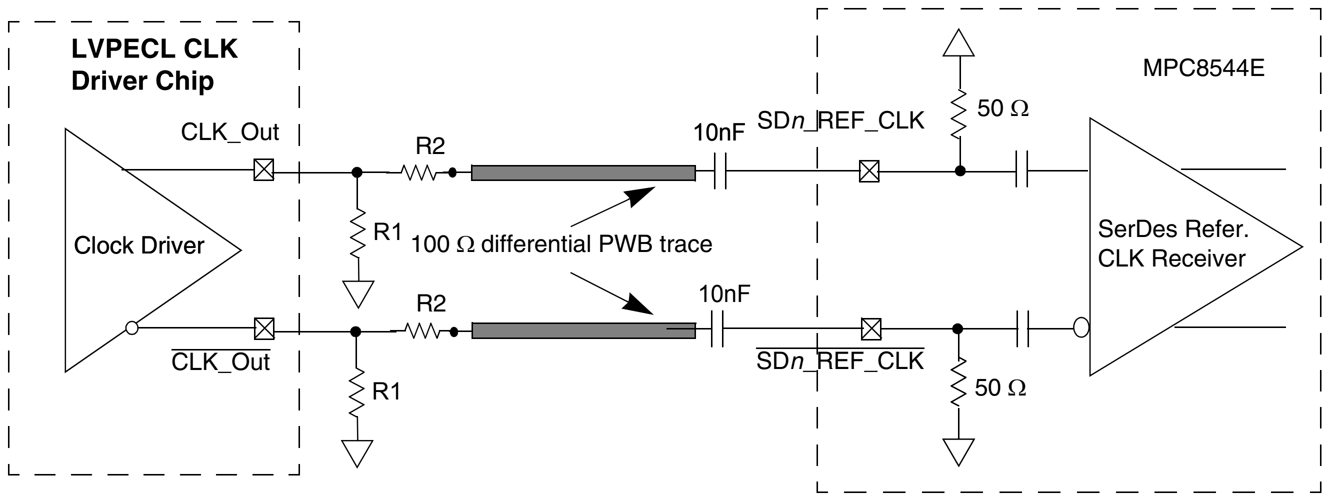


Figure 51. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 52 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8544E SerDes reference clock input's DC requirement.

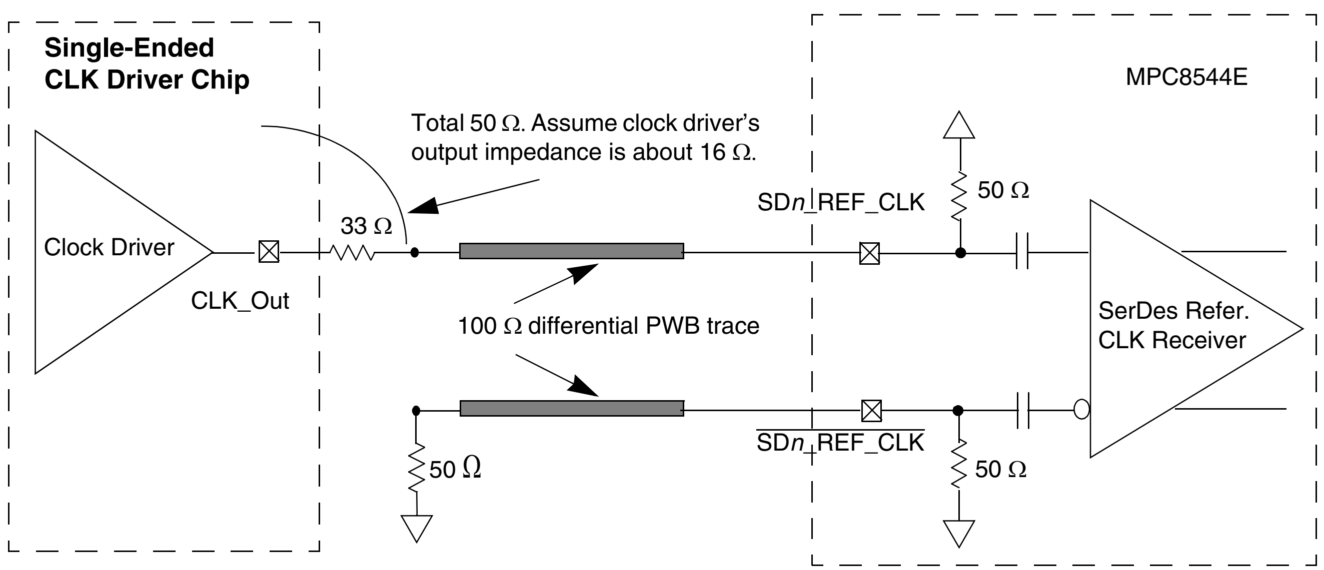


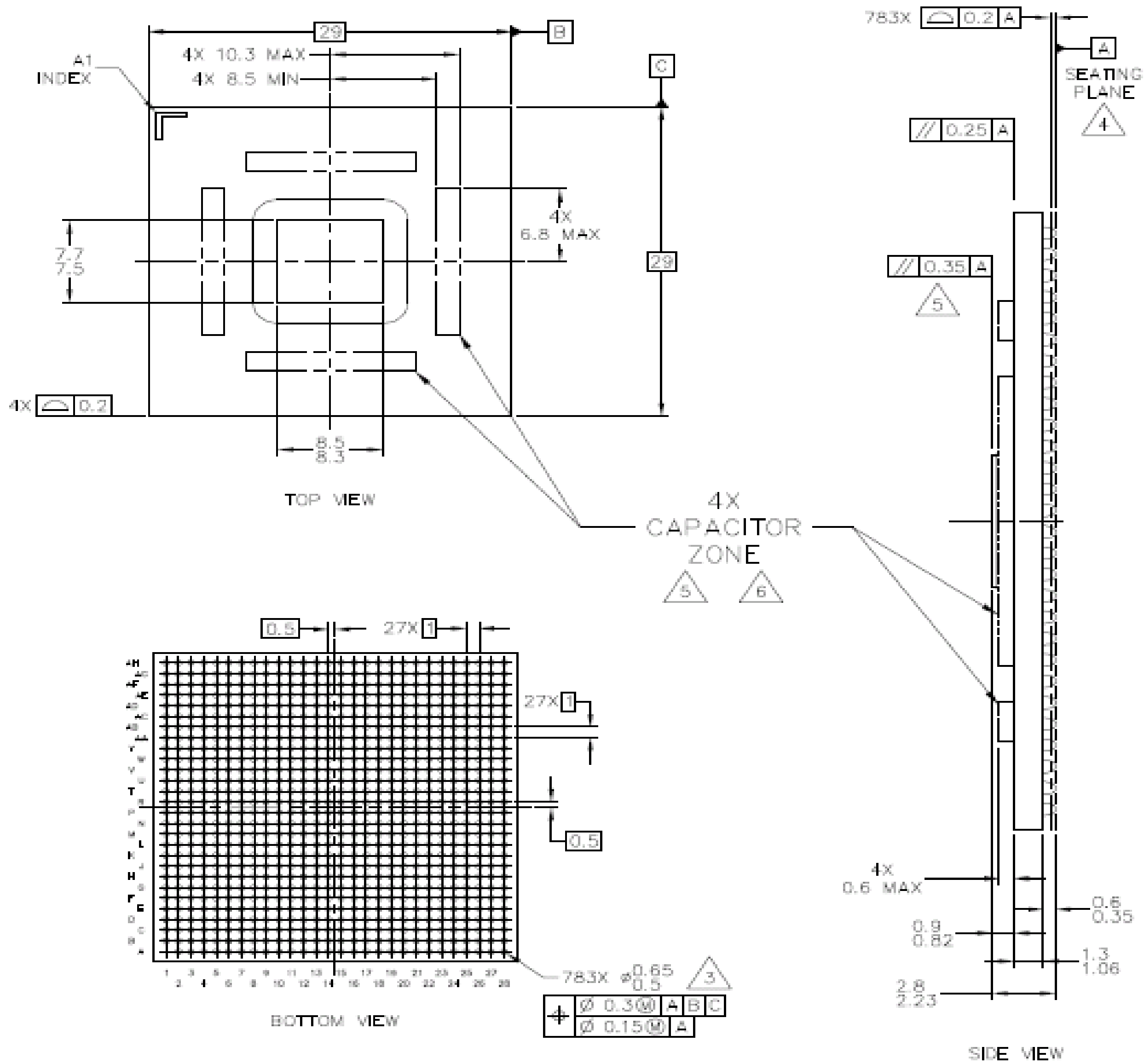
Figure 52. Single-Ended Connection (Reference Only)

Table 60. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7.
$V_{RX\text{-}CM\text{-}ACp}$	AC peak common mode input voltage	—	—	150	mV	$V_{RX\text{-}CM\text{-}ACp} = \lvert V_{RXD+} - V_{RXD-} \rvert \div 2 - V_{RX\text{-}CM\text{-}DC}$ $V_{RX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert /2$ See Note 2.
$RL_{RX\text{-}DIFF}$	Differential return loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 and –300 mV, respectively. See Note 4.
$RL_{RX\text{-}CM}$	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4.
$Z_{RX\text{-}DIFF\text{-}DC}$	DC differential input impedance	80	100	120	Ω	RX DC differential mode impedance. See Note 5.
$Z_{RX\text{-}DC}$	DC input impedance	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	Powered down DC input impedance	200 k	—	—	Ω	Required RX D+ as well as D– DC impedance when the receiver terminations do not have power. See Note 6.
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	Electrical idle detect threshold	65	—	175	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$ Measured at the package pins of the receiver.
$T_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	—	—	10	ms	An unexpected electrical idle ($V_{RX\text{-}DIFFp\text{-}p} < V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$) must be recognized no longer than $T_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}ENTERING}$ to signal an unexpected idle condition.

18.2 Mechanical Dimensions of the MPC8544E FC-PBGA

Figure 59 shows the mechanical dimensions and bottom surface nomenclature of the MPC8544E, 783 FC-PBGA package without a lid.



Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. Capacitors may not be present on all parts. Care must be taken not to short exposed metal capacitor pads.
7. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

Figure 59. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8544E FC-PBGA without a Lid

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Ethernet Management Interface				
EC_MDC	AC7	O	OV_{DD}	4, 8, 14
EC_MDIO	Y9	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	T2	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	U10, U9, T10, T9, U8, T8, T7, T6	I	LV_{DD}	—
TSEC1_TXD[7:0]	T5, U5, V5, V3, V2, V1, U2, U1	O	LV_{DD}	4, 8, 14
TSEC1_COL	R5	I	LV_{DD}	—
TSEC1_CRS	T4	I/O	LV_{DD}	16
TSEC1_GTX_CLK	T1	O	LV_{DD}	—
TSEC1_RX_CLK	V7	I	LV_{DD}	—
TSEC1_RX_DV	U7	I	LV_{DD}	—
TSEC1_RX_ER	R9	I	LV_{DD}	4, 8
TSEC1_TX_CLK	V6	I	LV_{DD}	—
TSEC1_TX_EN	U4	O	LV_{DD}	22
TSEC1_TX_ER	T3	O	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_RXD[7:0]	P11, N11, M11, L11, R8, N10, N9, P10	I	LV_{DD}	—
TSEC3_TXD[7:0]	M7, N7, P7, M8, L7, R6, P6, M6	O	LV_{DD}	4, 8, 14
TSEC3_COL	M9	I	LV_{DD}	—
TSEC3_CRS	L9	I/O	LV_{DD}	16
TSEC3_GTX_CLK	R7	O	LV_{DD}	—
TSEC3_RX_CLK	P9	I	LV_{DD}	—
TSEC3_RX_DV	P8	I	LV_{DD}	—
TSEC3_RX_ER	R11	I	LV_{DD}	—
TSEC3_TX_CLK	L10	I	LV_{DD}	—
TSEC3_TX_EN	N6	O	LV_{DD}	22
TSEC3_TX_ER	L8	O	LV_{DD}	4, 8
DUART				
$\overline{\text{UART\_CTS}}$[0:1]	AH8, AF6	I	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[0:1]	AG8, AG9	O	OV_{DD}	—

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
UART_SIN[0:1]	AG7, AH6	I	OV_{DD}	—
UART_SOUT[0:1]	AH7, AF7	O	OV_{DD}	—
I^2C interface				
IIC1_SCL	AG21	I/O	OV_{DD}	20
IIC1_SDA	AH21	I/O	OV_{DD}	20
IIC2_SCL	AG13	I/O	OV_{DD}	20
IIC2_SDA	AG14	I/O	OV_{DD}	20
SerDes 1				
SD1_RX[0:7]	N28, P26, R28, T26, Y26, AA28, AB26, AC28	I	XV_{DD}	—
$\overline{\text{SD1\_RX}}$[0:7]	N27, P25, R27, T25, Y25, AA27, AB25, AC27	I	XV_{DD}	—
SD1_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	O	XV_{DD}	—
$\overline{\text{SD1\_TX}}$[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	O	XV_{DD}	—
SD1_PLL_TPD	V28	O	XV_{DD}	17
SD1_REF_CLK	U28	I	XV_{DD}	—
$\overline{\text{SD1\_REF\_CLK}}$	U27	I	XV_{DD}	—
SD1_TST_CLK	T22		—	—
$\overline{\text{SD1\_TST\_CLK}}$	T23		—	—
SerDes 2				
SD2_RX[0]	AD25	I	XV_{DD}	—
SD2_RX[2]	AD1	I	XV_{DD}	26
SD2_RX[3]	AB2	I	XV_{DD}	26
$\overline{\text{SD2\_RX}}$[0]	AD26	I	XV_{DD}	—
$\overline{\text{SD2\_RX}}$[2]	AC1	I	XV_{DD}	26
$\overline{\text{SD2\_RX}}$[3]	AA2	I	XV_{DD}	26
SD2_TX[0]	AA21	O	XV_{DD}	—
SD2_TX[2]	AC4	O	XV_{DD}	26
SD2_TX[3]	AA5	O	XV_{DD}	26
$\overline{\text{SD2\_TX}}$[0]	AA20	O	XV_{DD}	—
$\overline{\text{SD2\_TX}}$[2]	AB4	O	XV_{DD}	26
$\overline{\text{SD2\_TX}}$[3]	Y5	O	XV_{DD}	26
SD2_PLL_TPD	AG3	O	XV_{DD}	17
SD2_REF_CLK	AE2	I	XV_{DD}	—

where:

I_{fw} = Forward current
I_s = Saturation current
V_d = Voltage at diode
V_f = Voltage forward biased
V_H = Diode voltage while I_H is flowing
V_L = Diode voltage while I_L is flowing
I_H = Larger diode bias current
I_L = Smaller diode bias current
q = Charge of electron (1.6×10^{-19} C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant (1.38×10^{-23} Joules/K)
T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$\mathbf{V_H - V_L = 1.986 \times 10^{-4} \times nT}$$

Solving for T, the equation becomes:

$$\mathbf{nT} = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8544E.

21.1 System Clocking

This device includes six PLLs:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 19.2, "CCB/SYSCLK PLL Ratio."
- The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 19.3, "e500 Core PLL Ratio."
- The PCI PLL generates the clocking for the PCI bus.
- The local bus PLL generates the clock for the local bus.
- There are two PLLs for the SerDes block.