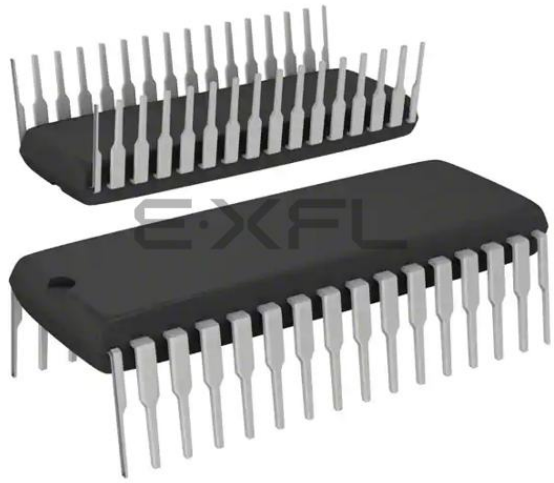

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, Motor Control PWM, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	32-SDIP (0.400", 10.16mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72t141k2b6

1.4 REGISTER & MEMORY MAP

As shown in Figure 6, the MCU is capable of addressing 64K bytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, 256 bytes of RAM and 8Kbytes of user program memory. The RAM space includes up to 64 bytes for the stack from 0140h to 017Fh.

The highest address bytes contain the user reset and interrupt vectors.

Figure 6. Memory Map

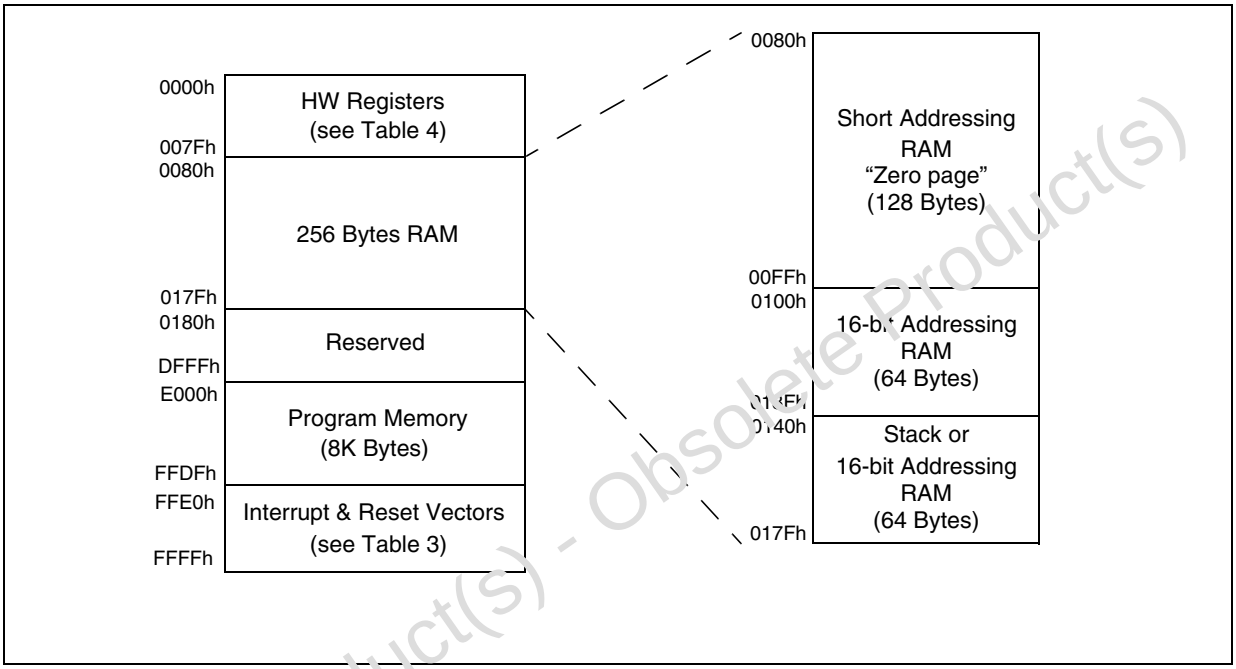


Table 3. Interrupt Vector Map

Vector Address	Description	Remarks
FFE0-FFE1h	Not used	Internal Interrupt
FFE2-FFE3h	Not used	
FFE4-FFE5h	Not used	
FFE6-FFE7h	Not used	
FFE8-FFE9h	Not used	
FFEA-FFEBh	TIMER B interrupt vector	
FFEC-FFEDh	TIMER A interrupt vector	
FFEE-FFEFh	SPI interrupt vector	
FFF0-FFF1h	Motor control interrupt vector (events: E, O)	
FFF2-FFF3h	Motor control interrupt vector (events: C, D)	
FFF4-FFF5h	Motor control interrupt vector (events: R, Z)	
FFF6-FFF7h	External interrupt vector EI1: port B7..0	External Interrupt
FFF8-FFF9h	External interrupt vector EI0: port A7..0	External Interrupt
FFFA-FFFBh	Not used	
FFFC-FFFDh	TRAP (software) interrupt vector	CPU Interrupt
FFFE-FFFFh	RESET vector	

Address	Block	Register Label	Register Name	Reset Status	Remarks
0041h	TIMER B	TBCR2	Timer B Control Register 2	00h	R/W
0042h		TBCR1	Timer B Control Register 1	00h	R/W
0043h		TBSR	Timer B Status Register	xxh	Read Only
0044h		TBIC1HR	Timer B Input Capture 1 High Register	xxh	Read Only
0045h		TBIC1LR	Timer B Input Capture 1 Low Register	xxh	Read Only
0046h		TBOC1HR	Timer B Output Compare 1 High Register	80h	R/W
0047h		TBOC1LR	Timer B Output Compare 1 Low Register	00h	R/W
0048h		TBCHR	Timer B Counter High Register	FFh	Read Only
0049h		TBCLR	Timer B Counter Low Register	FCh	Read Only
004Ah		TBACHR	Timer B Alternate Counter High Register	FFh	Read Only
004Bh		TBACLR	Timer B Alternate Counter Low Register	FCh	Read Only
004Ch		TBIC2HR	Timer B Input Capture 2 High Register	xxh	Read Only
004Dh		TBIC2LR	Timer B Input Capture 2 Low Register	xxh	Read Only
004Eh		TBOC2HR	Timer B Output Compare 2 High Register	80h	R/W
004Fh		TBOC2LR	Timer B Output Compare 2 Low Register	00h	R/W
0050h to 005Fh	Reserved Area (16 Bytes)				
0060h	MOTOR CONTROL	MTIM	Timer Counter Register	00h	R/W
0061h		MZPRV	Zn-1 Capture Register	00h	R/W
0062h		MZREG	Zn Capture Register	00h	R/W
0063h		MCOMP	C_{n+1} Compare Register	00h	R/W
0064h		MDREG	D capture/Compare Register	00h	R/W
0065h		MWGHT	Weight Register	00h	R/W
0066h		MPRSR	Prescaler and Ratio Register	00h	R/W
0067h		MIMR	Interrupt Mask Register	00h	R/W
0068h		MISR	Interrupt Status Register	00h	R/W
0069h		MCRA	Control Register A	00h	R/W
006Ah		MCRB	Control Register B	00h	R/W
006Bh		MPHST	Phase State Register	00h	R/W
006Ch		MPAR	Output Parity Register	00h	R/W
006Dh		MPOL	Output Polarity Register	00h	R/W
006Eh to 006Fh	Reserved Area (2 bytes)				
0070h	ADC	ADCDR	Data Register	00h	Read Only
0071h		ADCCSR	Control/Status Register	00h	R/W
0072h to 007Fh	Reserved Area (14 Bytes)				

CENTRAL PROCESSING UNIT (Cont'd)

Stack Pointer (SP)

Read/Write

Reset Value: 01 7Fh

15							8
0	0	0	0	0	0	0	1

7							0
0	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The Stack Pointer is a 16-bit register which is always pointing to the next free location in the stack. It is then decremented after data has been pushed onto the stack and incremented before data is popped from the stack (see Figure 8).

Since the stack is 128 bytes deep, the 9th most significant bits are forced by hardware. Following an MCU Reset, or after a Reset Stack Pointer instruction (RSP), the Stack Pointer contains its reset value (the SP6 to SP0 bits are set) which is the stack higher address.

The least significant byte of the Stack Pointer (called S) can be directly accessed by a LD instruction.

Note: When the lower limit is exceeded, the Stack Pointer wraps around to the stack upper limit, without indicating the stack overflow. The previously stored information is then overwritten and therefore lost. The stack also wraps in case of an underflow.

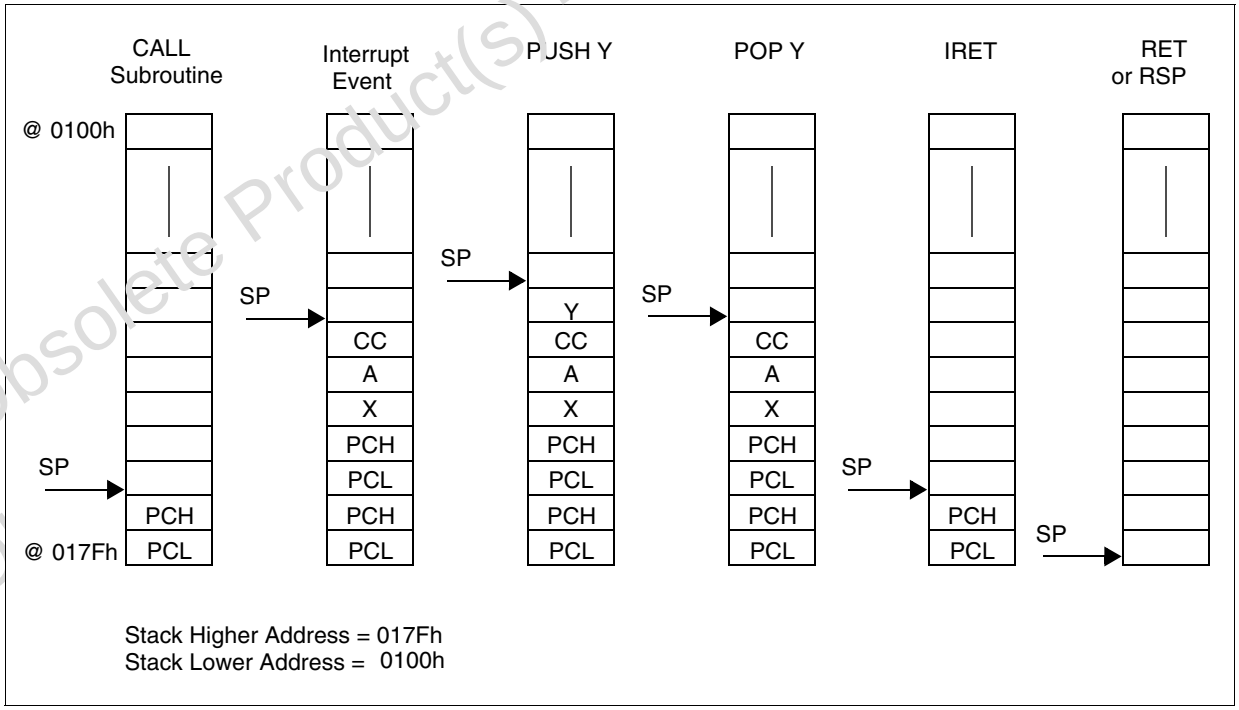
The stack is used to save the return address during a subroutine call and the CPU context during an interrupt. The user may also directly manipulate the stack by means of the PUSH and POP instructions. In the case of an interrupt, the PCL is stored at the first location pointed to by the SP. Then the other registers are stored in the next locations as shown in Figure 8.

– When an interrupt is received, the SP is decremented and the context is pushed on the stack.

– On return from interrupt, the SP is incremented and the context is popped from the stack.

A subroutine call occupies two locations and an interrupt five locations in the stack area.

Figure 8. Stack Manipulation Example



3.1 LOW VOLTAGE DETECTOR (LVD)

To allow the integration of power management features in the application, the Low Voltage Detector function (LVD) generates a static reset when the V_{DD} supply voltage is below a V_{LVDf} reference value. This means that it secures the power-up as well as the power-down keeping the ST7 in reset.

The V_{LVDf} reference value for a voltage drop is lower than the V_{LVDr} reference value for power-on in order to avoid a parasitic reset when the MCU starts running and sinks current on the supply (hysteresis).

The LVD Reset circuitry generates a reset when V_{DD} is below:

– V_{LVDr} when V_{DD} is rising
– V_{LVDf} when V_{DD} is falling

The LVD function is illustrated in Figure 10.

Provided the minimum V_{DD} value (guaranteed for the oscillator frequency) is below V_{LVDf}, the MCU can only be in two modes:

– under full software control
– in static safe reset

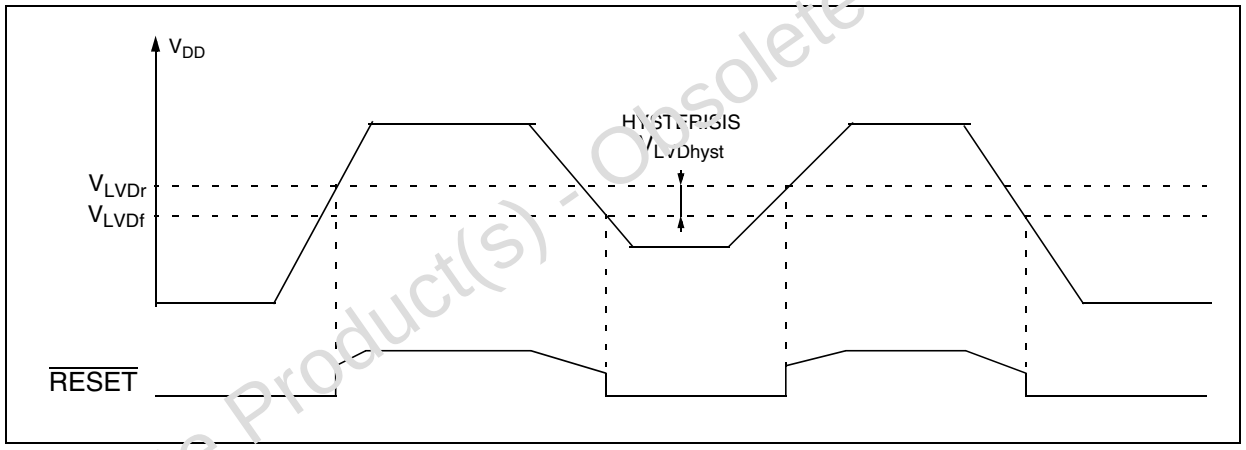
In these conditions, secure operation is always ensured for the application without the need for external reset hardware.

During a Low Voltage Detector Reset, the $\overline{\text{RESET}}$ pin is held low, thus permitting the MCU to reset other devices.

Notes:

The LVD allows the device to be used without any external RESET circuitry.

Figure 10. Low Voltage Detector vs Reset

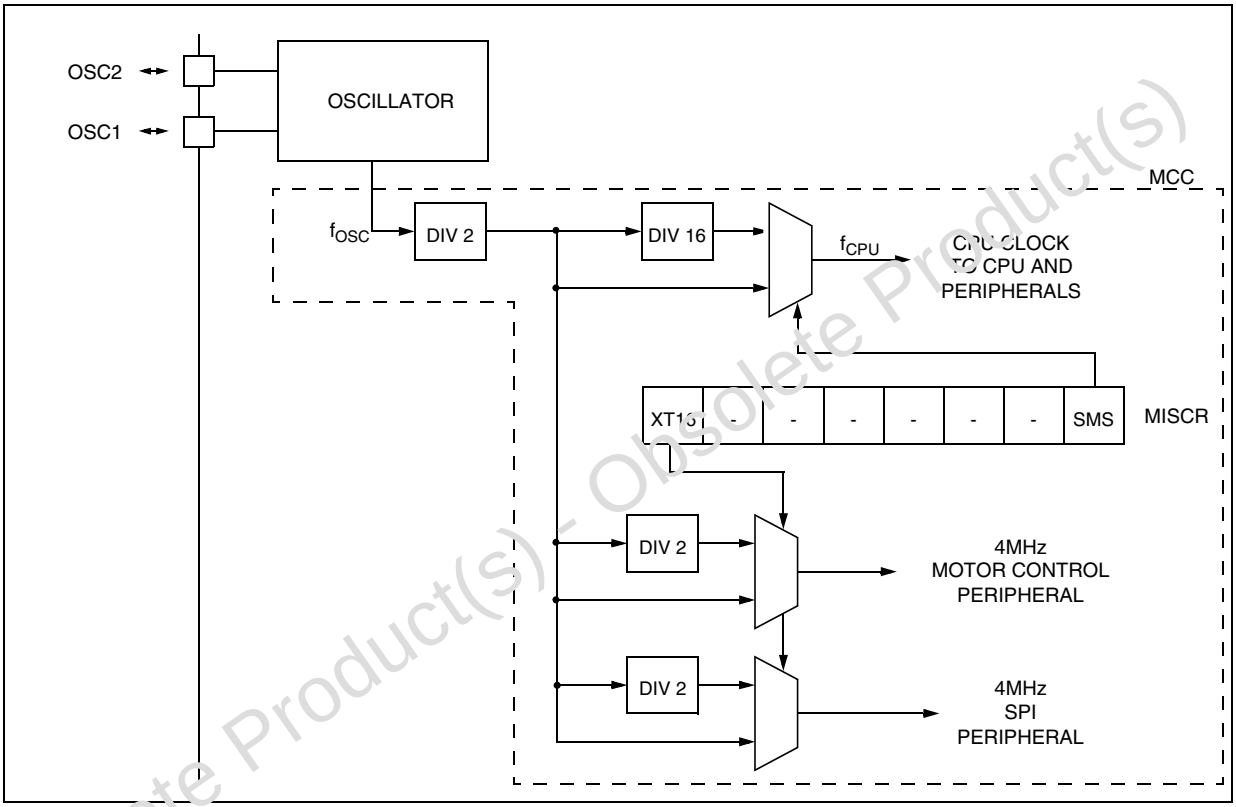


3.4 MAIN CLOCK CONTROLLER (MCC)

The MCC block supplies the clock for the ST7 CPU and its internal peripherals. It allows the SLOW power saving mode and the Motor Contral and SPI peripheral clocks to be managed independently. The MCC functionality is controlled by two bits of the MISCR register: SMS and XT16.

The XT16 bit acts on the clock of the motor control and SPI peripherals while the SMS bit acts on the CPU and the other peripherals.

Figure 17. Main Clock Controller (MCC) Block Diagram



POWER SAVING MODES (Cont'd)

5.3 WAIT Mode

WAIT mode places the MCU in a low power consumption mode by stopping the CPU.
This power saving mode is selected by calling the "WFI" ST7 software instruction.
All peripherals remain active. During WAIT mode, the I bit of the CC register are forced to 0, to enable all interrupts. All other registers and memory remain unchanged. The MCU remains in WAIT mode until an interrupt or Reset occurs, whereupon the Program Counter branches to the starting address of the interrupt or Reset service routine.
The MCU will remain in WAIT mode until a Reset or an Interrupt occurs, causing it to wake up.

Refer to Figure 22.

5.4 SLOW Mode

This mode has two targets:

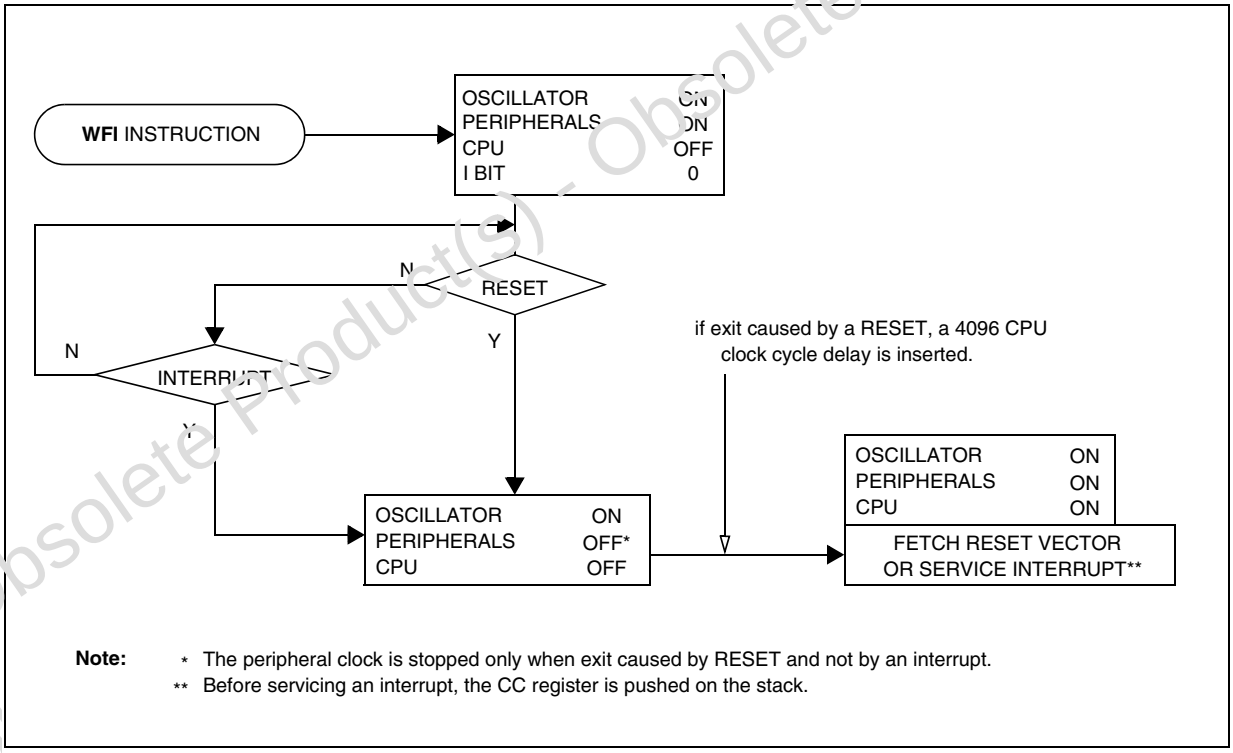
– To reduce power consumption by decreasing the internal clock in the device,

– To adapt the internal clock frequency (f_{CPU}) to the available supply voltage.

SLOW mode is controlled by the SMS bit in the MISCR register. This bit enables or disables Slow mode selecting the internal slow frequency (f_{CPU}).

In this mode, the oscillator frequency can be divided by 32 instead of 2 in normal operating mode. The CPU and peripherals are clocked at this lower frequency except the Motor Control and the SPI peripherals which have their own clock selection bit (XT16) in the MISCR register.

Figure 22. WAIT mode flow-chart



Note: * The peripheral clock is stopped only when exit caused by RESET and not by an interrupt.
** Before servicing an interrupt, the CC register is pushed on the stack.

I/O PORTS (Cont'd)

Figure 23. I/O Port General Block Diagram

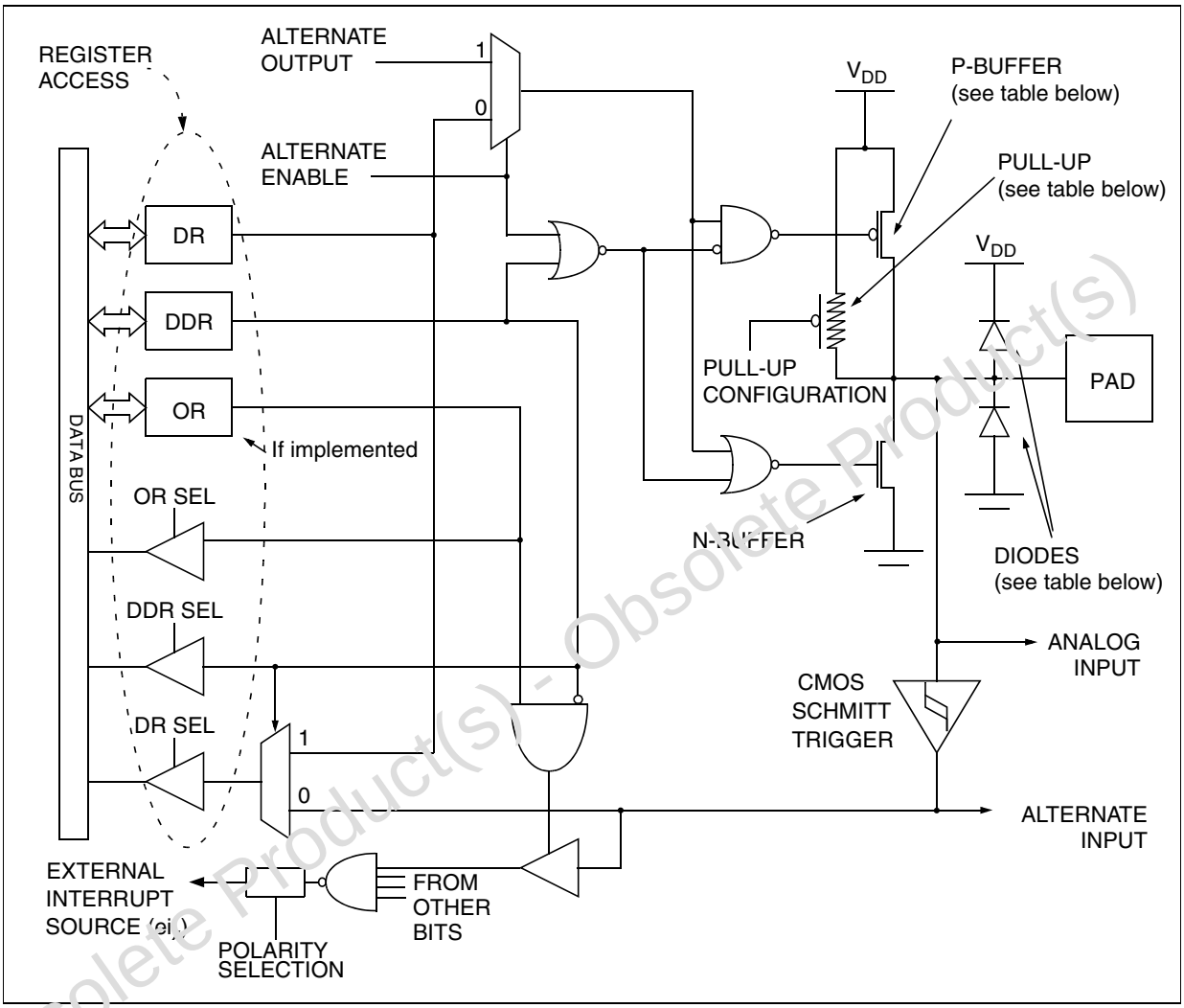


Table 6. I/O Port Mode Options

Configuration Mode		Pull-Up	P-Buffer	Diodes	
				to V_{DD}	to V_{SS}
Input	Floating with/without Interrupt	Off	Off	On	On
	Pull-up with/without Interrupt	On			
Output	Push-pull	Off	On		
	Open Drain (logic level)		Off		
	True Open Drain	NI	NI	NI (see note)	

Legend: NI - not implemented
Off - implemented not activated
On - implemented and activated

Note: The diode to V_{DD} is not implemented in the true open drain pads. A local protection between the pad and V_{SS} is implemented to protect the device against positive stress.

MISCELLANEOUS REGISTER (Cont'd)

7.4 Miscellaneous Register Description

MISCELLANEOUS REGISTER (MISCR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
XT16	SSM	SSI	IS11	IS10	IS01	IS00	SMS

Bit 7 = **XT16** *MTC and SPI clock selection*
This bit is set and cleared by software. The maximum allowed frequency is 4MHz.
0: MTC and SPI clock supplied with $f_{OSC}/2$
1: MTC and SPI clock supplied with $f_{OSC}/4$

Bit 6 = **SSM** *$\overline{SS}$ mode selection*
This bit is set and cleared by software.
0: Normal mode - the level of the SPI $\overline{SS}$ signal is the external $\overline{SS}$ pin.
1: I/O mode, the level of the SPI $\overline{SS}$ signal is read from the SSI bit.

Bit 5 = **SSI** *$\overline{SS}$ internal mode*
This bit replaces the $\overline{SS}$ pin of the SPI when the SSM bit is set to 1. (see SPI description). It is set and cleared by software.

Bits 4:3 = **IS1[1:0]** *EI1 sensitivity*
The interrupt sensitivity defined using the IS1[1:0] bits combination is applied to the EI1 external interrupts. These two bits can be written only when the I bit of the CC register is set to 1 (interrupt masked).

EI1: Port B

IS11	IS10	External Interrupt Sensitivity
0	0	Falling edge & low level
0	1	Rising edge only
1	0	Falling edge only
1	1	Rising and falling edge

Bits 2:1 = **IS0[1:0]** *EI0 sensitivity*
The interrupt sensitivity defined using the IS0[1:0] bits combination is applied to the EI1 external interrupts. These two bits can be written only when the I bit of the CC register is set to 1 (interrupt masked).

EI0: Port A

IS01	IS00	External Interrupt Sensitivity
0	0	Falling edge & low level
0	1	Rising edge only
1	0	Falling edge only
1	1	Rising and falling edge

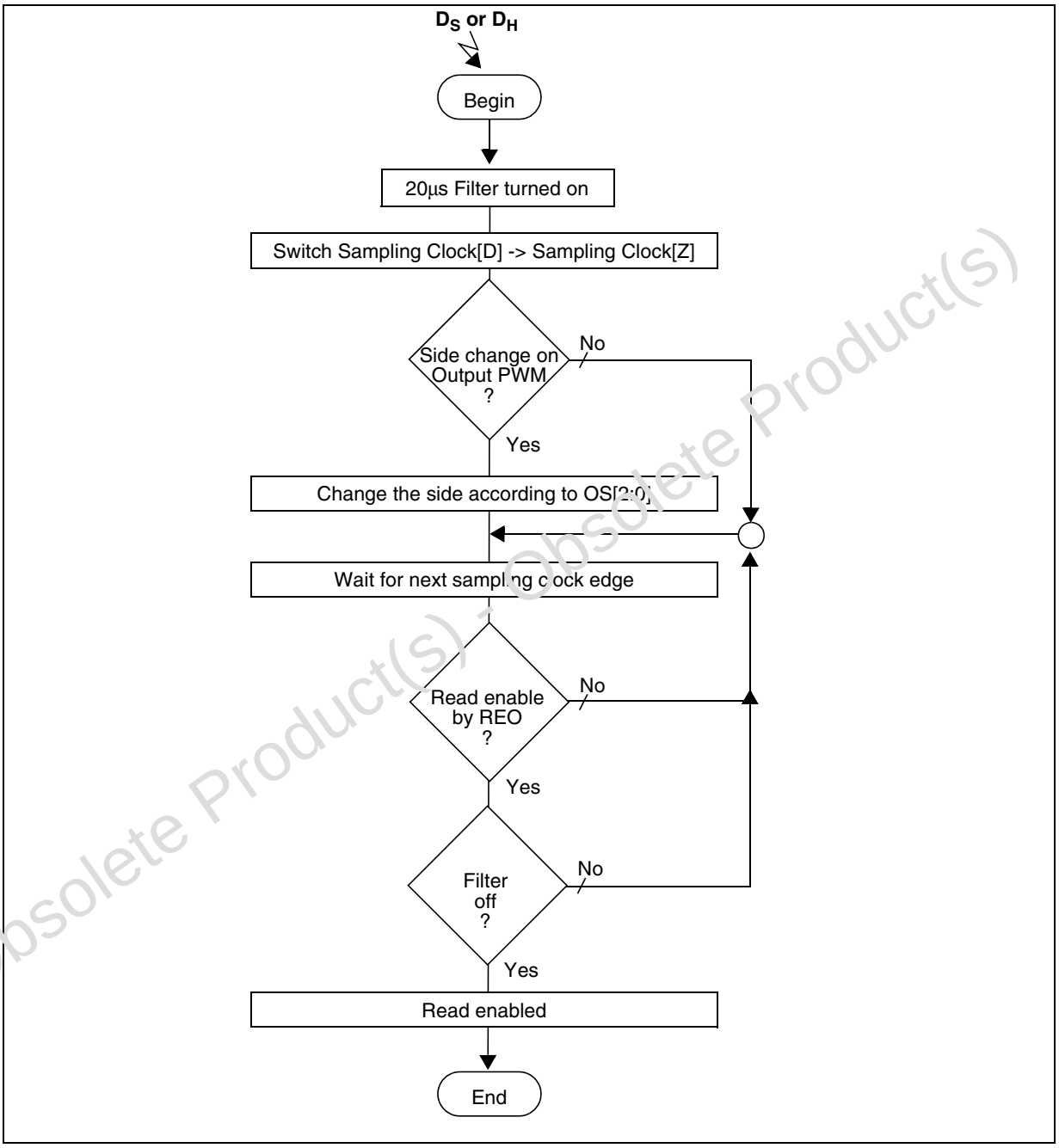
Bit 0 = **SMS** *Slow mode select*
This bit is set and cleared by software.
0: Normal mode. $f_{CPU} = f_{OSC} / 2$
1: Slow mode. $f_{CPU} = f_{OSC} / 32$
See sections on low power consumption mode and MCC for more details.

Table 10. Miscellaneous Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0020h	**MISCR** Reset Value	XT16 0	SSM 0	SSI 0	IS11 0	IS10 0	IS01 0	IS00 0	SMS 0

MOTOR CONTROLLER (Cont'd)

Figure 32. Functional Diagram of Z Detection after D Event



MOTOR CONTROLLER (Cont'd)

Table 20. MTIM Timer-related Registers

Name	Reset Value	Contents
MTIM	00h	Timer Value
MZPRV	00h	Capture Zn-1
MZREG	00h	Capture Zn
MCOMP	00h	Compare Cn+1
MDREG	00h	Demagnetization Dn

Note on using the auto-updated MTIM timer: The auto-updated MTIM timer works accurately within its operating range but some care has to be taken when processing timer-dependent data such as the step duration for regulation or demagnetization.

For example if an overflow occurs when calculating a software end of demagnetization (MCOMP+demagnetisation_time>FFh), the value that stored in MDREG will be:
7Fh+(MCOMP+demagnetization_time-FFh)/2.

Note on commutation interrupts: It is good practice to modify the configuration for the next step as soon as possible, i.e within the commutation interrupt routine.

All registers that need to be changed at each step have a preload register that enables the modifications for a complete new configuration to be performed at the same time (at C event in normal mode or when writing the MPHST register in direct access mode).

These configuration bits are:

CPB, HDM, SDM and OS2 in the MCRB register and IS[1:0], OO[5:0] in the MPHST register.

Note on initializing the MTC: As shown in Table 22 all the MTIM timer registers are in read-write mode until the MTC clock is enabled (with the MOE and DAC bits). This allows the timer, prescaler and compare registers to be properly initialized for start-up.

In sensorless mode, the motor has to be started in switched mode until a BEMF voltage is present on the inputs. This means the prescaler ST[3:0] bits and MCOMP register have to be modified by software. When running the ST[3:0] bits can only be incremented/decremented, so the initial value is very important.

When starting directly in autoswitched mode (in sensor mode for example), write an appropriate value in the MZREG and MZPRV register to perform a step calculation as soon as the clock is enabled.

MOTOR CONTROLLER (Cont'd)

Direct access to the phase register is also possible when the DAC bit in the MCRA register is set.

Table 26. DAC and MOE Bit Meaning

MOE bit	DAC bit	Effect on Output	Effect on MTIM Timer
0	x	High Z	Clock disabled
1	0	Standard running mode	Standard running mode
1	1	MPHST value same as MPOL value	Clock disabled

The polarity register is used to match the polarity of the power drivers keeping the same control logic and software. If one of the OPx bits in the MPOL register is set, this means the switch x is ON when MCOx is V_{DD}.

Each output status depends also on the momentary state of the PWM, its group (odd or even), and the peripheral state.

PWM Features

The outputs can be split in two PWM groups in order to differentiate the high side and the low side switches. This output property can be programmed using the OE[5:0] bits in the MPAR register

Table 27. Meaning of the OE[5:0] Bits

OE[5:0]	Channel group
0	Even channel
1	Odd channel

The multiplexer directs the PWM to the upper channel, the lower channel or both of them alternatively or simultaneously according to the peripheral state.

This means that the PWM can affect any of the upper or lower channels allowing the selection of the most appropriate reference potential when freewheeling the motor in order to:

– Improve system efficiency
– Speed up the demagnetization phase
– Enable Back EMF zero crossing detection.

The OS[2:0] bits in the MCRB register allow the PWM configuration to be configured for each case as shown in Figure 41, Figure 42 and Figure 40. This configuration depends also on the current/voltage mode (V0C1 bit in the MCRA register) because the OS[2:0] have not the same meaning in voltage mode and in current mode.

During demagnetization, the OS2 bit is used to control PWM mode, and it is latched in a preload register so it can be modified when a commutation event occurs.

The OS[1:0] bits are used to control the PWM between the D and C events.

Warning: In Voltage Mode the OS[2:0] bits have a special configuration value: OS[2:0] = 010.

In this mode, there is NO current limitation and NO PWM applied to active outputs. The active outputs are always at 100% whether in demagnetization, or normal mode.

Note about demagnetization speed-up: during demagnetization the voltage on the winding has to be as high as possible in order to reduce the demagnetization time. Software can apply a different PWM configuration on the outputs between the C and D events, to force the free wheeling on the appropriate diodes to maximize the demagnetization voltage.

Emergency Feature

When the NMCES pin goes low

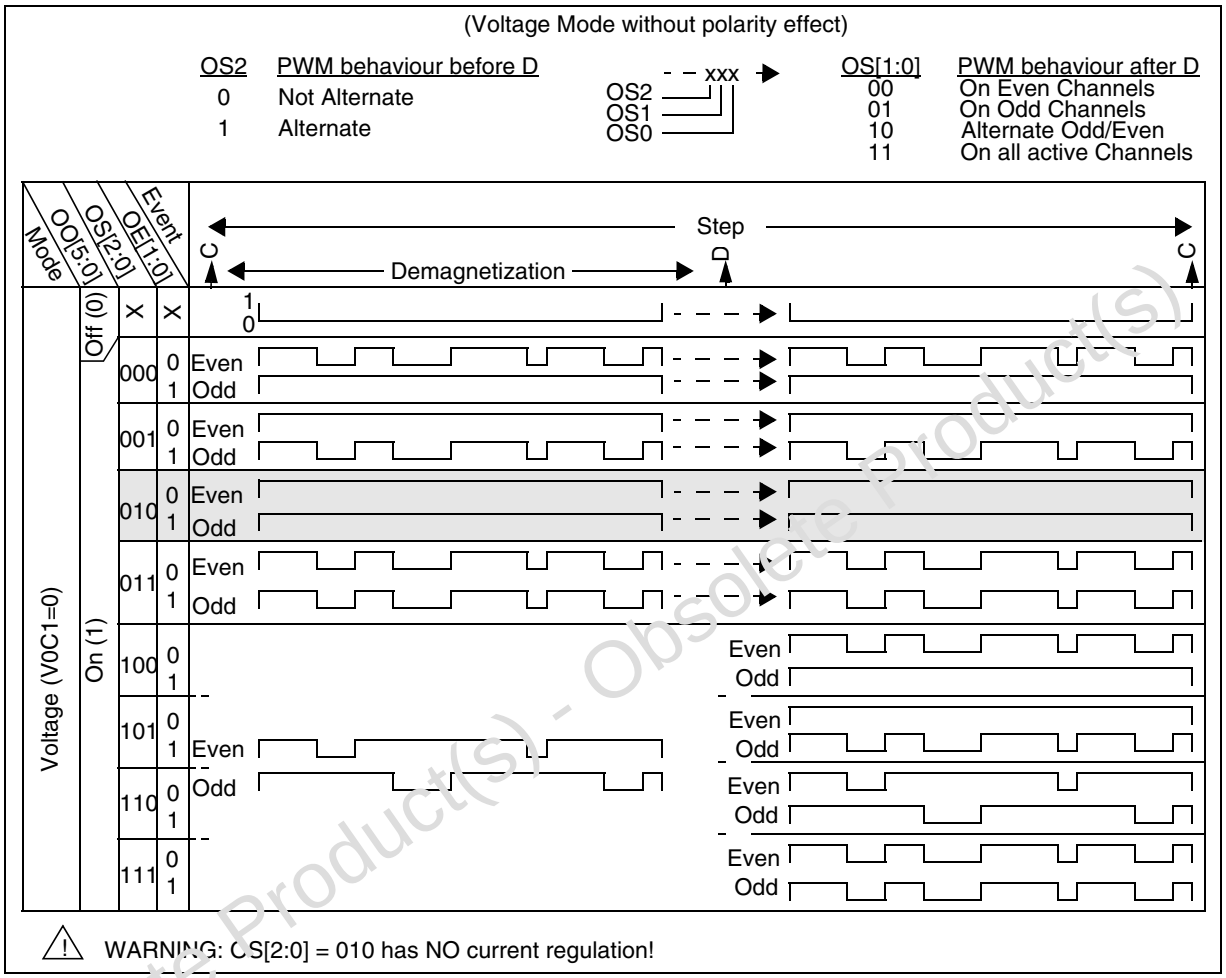
– The tristate output buffer is put in HiZ asynchronously
– The MOE bit in the MCRA register is reset
– An interrupt request is sent to the CPU if the EIM bit in the MIMR register is set

This bit can be connected to an alarm signal from the drivers, thermal sensor or any other security component.

This feature functions even if the MCU oscillator is off.

MOTOR CONTROLLER (Cont'd)

Figure 40. Step Behaviour of one Output Channel MCO[n] in Voltage Mode



WATCHDOG TIMER (Cond't)

Table 40. Watchdog Timer Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0024h	**WDGCR** Reset Value	WDGA 0	T6 1	T5 1	T4 1	T3 1	T2 1	T1 1	T0 1
0025h	**WDGSR** Reset Value	- 0	- 0	- 0	- 0	- 0	- 0	- 0	WDOGF 0

16-BIT TIMER (Cont'd)

Notes:

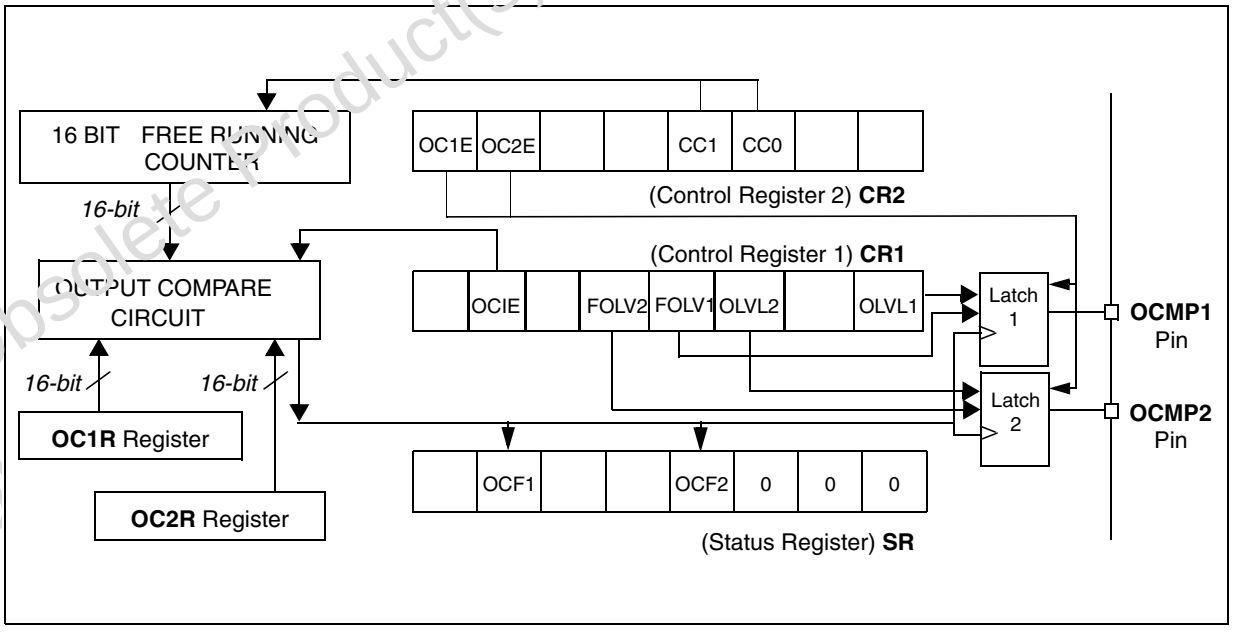
1. After a processor write cycle to the OC*i*HR register, the output compare function is inhibited until the OC*i*LR register is also written.
2. If the OC*i*E bit is not set, the OCMP*i* pin is a general I/O port and the OLVL*i* bit will not appear when a match is found but an interrupt could be generated if the OCIE bit is set.
3. When the timer clock is $f_{CPU}/2$, OCF*i* and OCMP*i* are set while the counter value equals the OC*i*R register value (see Figure 52). This behaviour is the same in OPM or PWM mode. When the timer clock is $f_{CPU}/4$, $f_{CPU}/8$ or in external clock mode, OCF*i* and OCMP*i* are set while the counter value equals the OC*i*R register value plus 1 (see Figure 53).
4. The output compare functions can be used both for generating external events on the OCMP*i* pins even if the input capture mode is also used.
5. The value in the 16-bit OC*i*R register and the OLV*i* bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed timeout.

Forced Compare Output capability

When the FOLV*i* bit is set by software, the OLVL*i* bit is copied to the OCMP*i* pin. The OLV*i* bit has to be toggled in order to toggle the OCMP*i* pin when it is enabled (OC*i*E bit=1). The OCF*i* bit is then not set by hardware, and thus no interrupt request is generated.

FOLVL*i* bits have no effect in either One-Pulse mode or PWM mode.

Figure 51. Output Compare Block Diagram



16-BIT TIMER (Cont'd)

8.3.4 Low Power Modes

Mode	Description
WAIT	No effect on 16-bit Timer. Timer interrupts cause the device to exit from WAIT mode.
HALT	16-bit Timer registers are frozen. In HALT mode, the counter stops counting until Halt mode is exited. Counting resumes from the previous count when the MCU is woken up by an interrupt with "exit from HALT mode" capability or from the counter reset value when the MCU is woken up by a RESET. If an input capture event occurs on the ICAP*i* pin, the input capture detection circuitry is armed. Consequently, when the MCU is woken up by an interrupt with "exit from HALT mode" capability, the ICF*i* bit is set, and the counter value present when exiting from HALT mode is captured into the IC*i*R register.

8.3.5 Interrupts

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
Input Capture 1 event/Counter reset in PWM mode	ICF1	ICIE	Yes	No
Input Capture 2 event	ICF2		Yes	No
Output Compare 1 event (not available in PWM mode)	OCF1	OCIE	Yes	No
Output Compare 2 event (not available in PWM mode)	OCF2		Yes	No
Timer Overflow event	TOF	TOIE	Yes	No

Note: The 16-bit Timer interrupt events are connected to the same interrupt vector (see Interrupts chapter). These events generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

8.3.6 Summary of Timer modes

MODES	AVAILABLE RESOURCES			
	Input Capture 1	Input Capture 2	Output Compare 1	Output Compare 2
Input Capture (1 and/or 2)	Yes	Yes	Yes	Yes
Output Compare (1 and/or 2)	Yes	Yes	Yes	Yes
One Pulse mode	No	Not Recommended[1)]	No	Partially [2)]
PWM Mode	No	Not Recommended[3)]	No	No

1) See note 4 in Section 8.3.3.5 One Pulse Mode

2) See note 5 in Section 8.3.3.5 One Pulse Mode

3) See note 4 in Section 8.3.3.6 Pulse Width Modulation Mode

SERIAL PERIPHERAL INTERFACE (Cont'd)

8.4.4.3 Data Transfer Format

During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The serial clock is used to synchronize the data transfer during a sequence of eight clock pulses.

The $\overline{SS}$ pin allows individual selection of a slave device; the other slave devices that are not selected do not interfere with the SPI transfer.

Clock Phase and Clock Polarity

Four possible timing relationships may be chosen by software, using the CPOL and CPHA bits.

The CPOL (clock polarity) bit controls the steady state value of the clock when no data is being transferred. This bit affects both master and slave modes.

The combination between the CPOL and CPHA (clock phase) bits selects the data capture clock edge.

Figure 59, shows an SPI transfer with the four combinations of the CPHA and CPOL bits. The diagram may be interpreted as a master or slave timing diagram where the SCK pin, the MISO pin, the MOSI pin are directly connected between the master and the slave device.

The $\overline{SS}$ pin is the slave device select input and can be driven by the master device.

The master device applies data to its MOSI pin-clock edge before the capture clock edge.

CPHA bit is set

The second edge on the SCK pin (falling edge if the CPOL bit is reset, rising edge if the CPOL bit is set) is the MSBit capture strobe. Data is latched on the occurrence of the second clock transition.

No write collision should occur even if the $\overline{SS}$ pin stays low during a transfer of several bytes (see Figure 58).

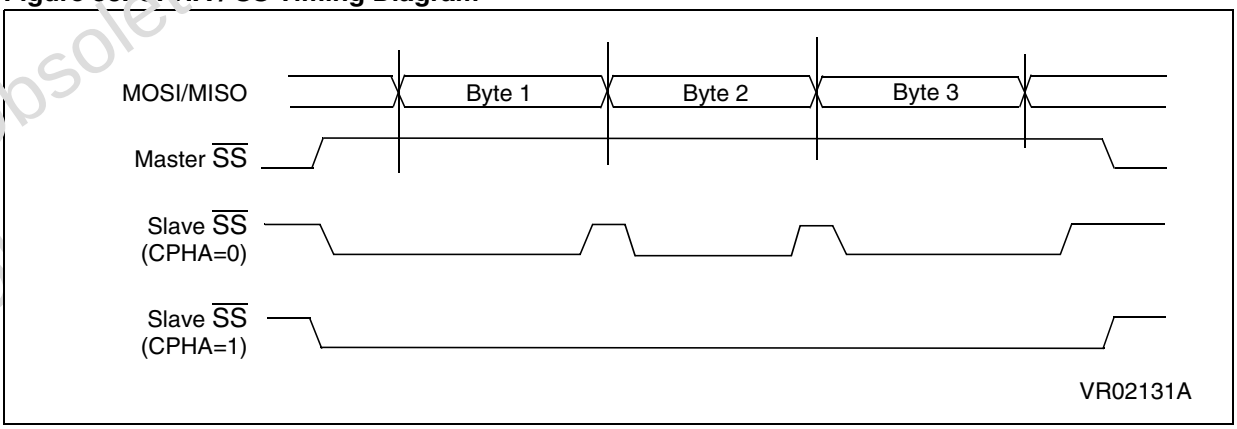
CPHA bit is reset

The first edge on the SCK pin (falling edge if CPOL bit is set, rising edge if CPOL bit is reset) is the MSBit capture strobe. Data is latched on the occurrence of the first clock transition.

The $\overline{SS}$ pin must be toggled high and low between each byte transmitted (see Figure 58).

To protect the transmission from a write collision a low value on the $\overline{SS}$ pin of a slave device freezes the data in its DR register and does not allow it to be altered. Therefore the $\overline{SS}$ pin must be high to write a new data byte in the DR without producing a write collision.

Figure 58. CPHA / $\overline{SS}$ Timing Diagram



ST7 ADDRESSING MODES (Cont'd)

9.1.1 Inherent

All Inherent instructions consist of a single byte. The opcode fully specifies all the required information for the CPU to process the operation.

Inherent Instruction	Function
NOP	No operation
TRAP	S/W Interrupt
WFI	Wait For Interrupt (Low Power Mode)
HALT	Halt Oscillator (Lowest Power Mode)
RET	Sub-routine Return
IRET	Interrupt Sub-routine Return
SIM	Set Interrupt Mask
RIM	Reset Interrupt Mask
SCF	Set Carry Flag
RCF	Reset Carry Flag
RSP	Reset Stack Pointer
LD	Load
CLR	Clear
PUSH/POP	Push/Pop to/from the stack
INC/DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
MUL	Byte Multiplication
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles

9.1.2 Immediate

Immediate instructions have two bytes, the first byte contains the opcode, the second byte contains the operand value.

Immediate Instruction	Function
LD	Load
CP	Compare
BCP	Bit Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Operations

9.1.3 Direct

In Direct instructions, the operands are referenced by their memory address.

The direct addressing mode consists of two sub-modes:

Direct (short)

The address is a byte, thus requires only one byte after the opcode, but only allows 00 - FF addressing space.

Direct (long)

The address is a word, thus allowing 64 Kbyte addressing space, but requires 2 bytes after the opcode.

9.1.4 Indexed (No Offset, Short, Long)

In this mode, the operand is referenced by its memory address, which is defined by the unsigned addition of an index register (X or Y) with an offset.

The indexed addressing mode consists of three sub-modes:

Indexed (No Offset)

There is no offset, (no extra byte after the opcode), and allows 00 - FF addressing space.

Indexed (Short)

The offset is a byte, thus requires only one byte after the opcode and allows 00 - 1FE addressing space.

Indexed (long)

The offset is a word, thus allowing 64 Kbyte addressing space and requires 2 bytes after the opcode.

9.1.5 Indirect (Short, Long)

The required data byte to do the operation is found by its memory address, located in memory (pointer).

The pointer address follows the opcode. The indirect addressing mode consists of two sub-modes:

Indirect (short)

The pointer address is a byte, the pointer size is a byte, thus allowing 00 - FF addressing space, and requires 1 byte after the opcode.

Indirect (long)

The pointer address is a byte, the pointer size is a word, thus allowing 64 Kbyte addressing space, and requires 1 byte after the opcode.

MEMORY AND PERIPHERAL CHARACTERISTICS (Cont'd)

Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH} in the SPI Timing Diagram

Figure 69. SPI Slave Timing Diagram CPHA=0, CPOL=0 1)

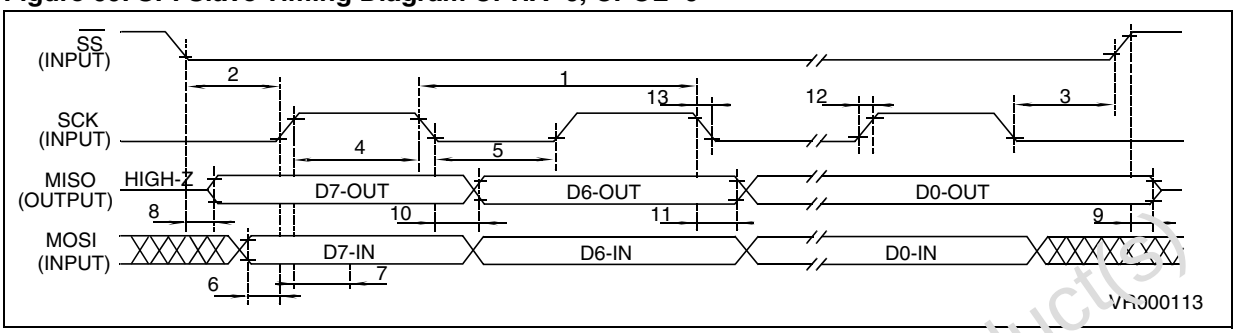


Figure 70. SPI Slave Timing Diagram CPHA=0, CPOL=1 1)

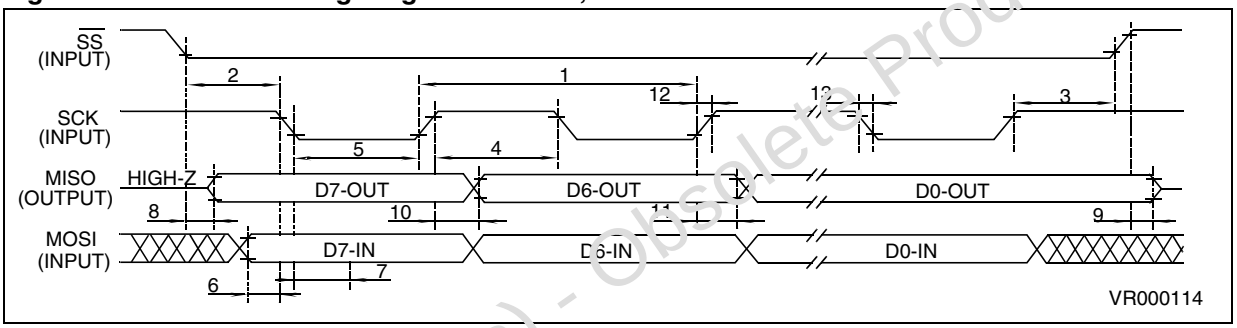


Figure 71. SPI Slave Timing Diagram CPHA=1, CPOL=0 1)

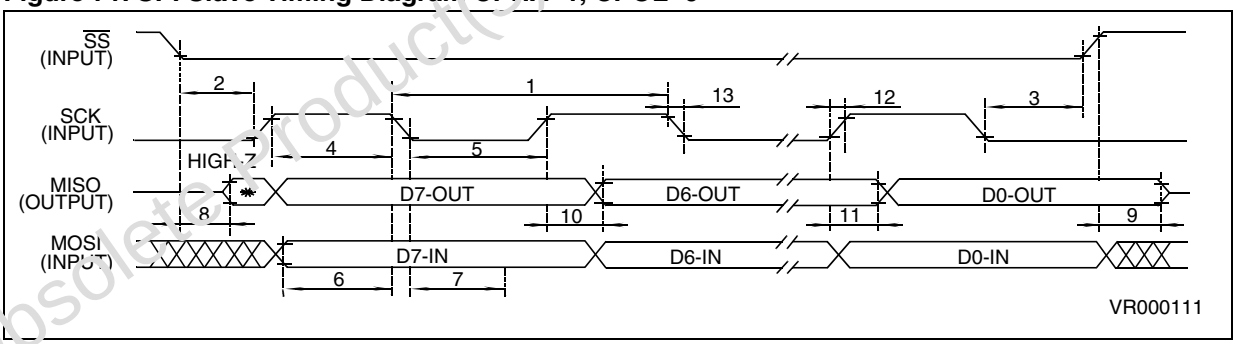
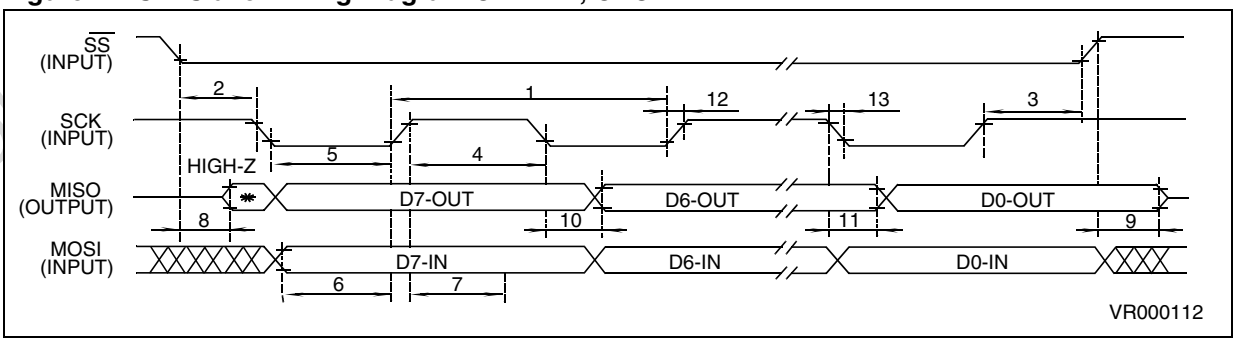


Figure 72. SPI Slave Timing Diagram CPHA=1, CPOL=1 1)



Note:
1) Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH} in the SPI timing diagram

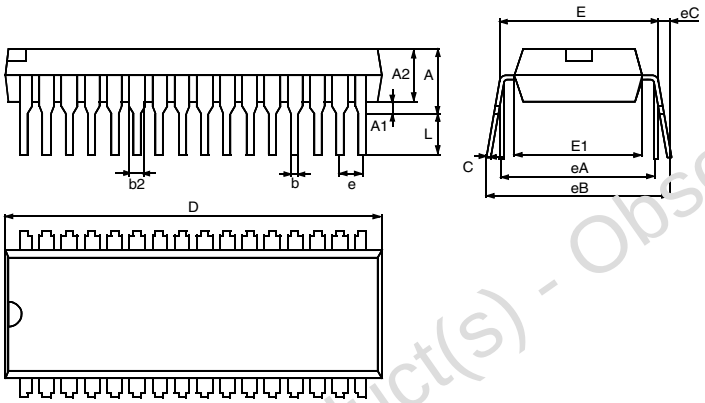
11 PACKAGE CHARACTERISTICS

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK® specifications are available at: www.st.com.

11.1 PACKAGE MECHANICAL DATA

Figure 73. 32-Pin Plastic Dual In-Line Package, Shrink 400-mil Width



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	3.56	3.76	5.08	0.1402	0.1480	0.2000
A1	0.51			0.0201		
A2	3.05	3.56	4.57	0.1201	0.1402	0.1799
b	0.36	0.46	0.58	0.0142	0.0181	0.0228
b2	0.76	1.02	1.40	0.0299	0.0402	0.0551
C	0.20	0.25	0.36	0.0079	0.0098	0.0142
D	27.43		28.45	1.0799		1.1201
E	9.91	10.41	11.05	0.3902	0.4098	0.4350
E1	7.62	8.89	9.40	0.3000	0.3500	0.3701
e		1.78			0.0701	
eA		10.16			0.4000	
eB			12.70			0.5000
eC			1.40			0.0551
L	2.54	3.05	3.81	0.1000	0.1201	0.1500
	Number of Pins					
N	32					

Note 1. Values in inches are converted from mm and rounded to 4 decimal digits.

12 SUMMARY OF CHANGES

Description of the changes between the current release of the specification and the previous one.

Rev.	Main Changes	Date
1.8	Added VtPOR in section 10.6.1 on page 121 Modified VMTChyst and Voffset in section 10.7 on page 122 Modified Option list in Section 11.2	Oct-01
2	Title modified (ST72141K2) Removed references to EPROM devices Document status modified (not for new design) Added “related documentation” section in specific chapters thoughout document Table 13 on page 46 updated with corrections to ZVD and CPB figures for ZVD=1 “RESET Sequence Manager” on page 121: replaced 30 µs with 500 ns to be in line with spec given in “Functional Description” on page 76 In section 8.3.3.3 on page 82: Replaced “see figure 5” with “see Figure 48” in second paragraph In section 9.1.4 on page 113: Replaced “The indirect addressing mode” with “The indexed addressing mode” in second paragraph In “PACKAGE CHARACTERISTICS” on page 128: Added Ecopack information Values in inches rounded to 4 decimal digits (instead of 3 decimal digits) in Figure 73 and Figure 74. Modified Figure 75 and Figure 76 on page 130	04-Nov-08