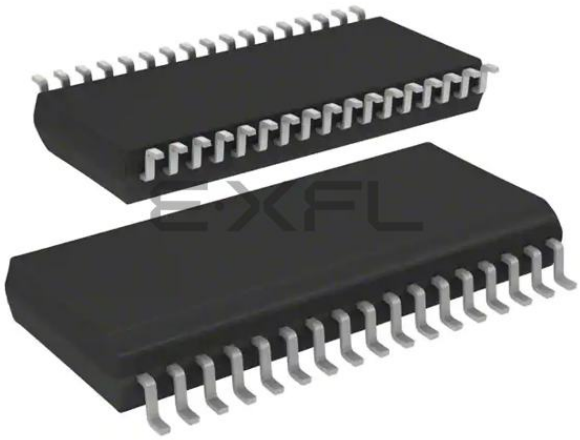

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, Motor Control PWM, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	34-BSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72t141k2m6

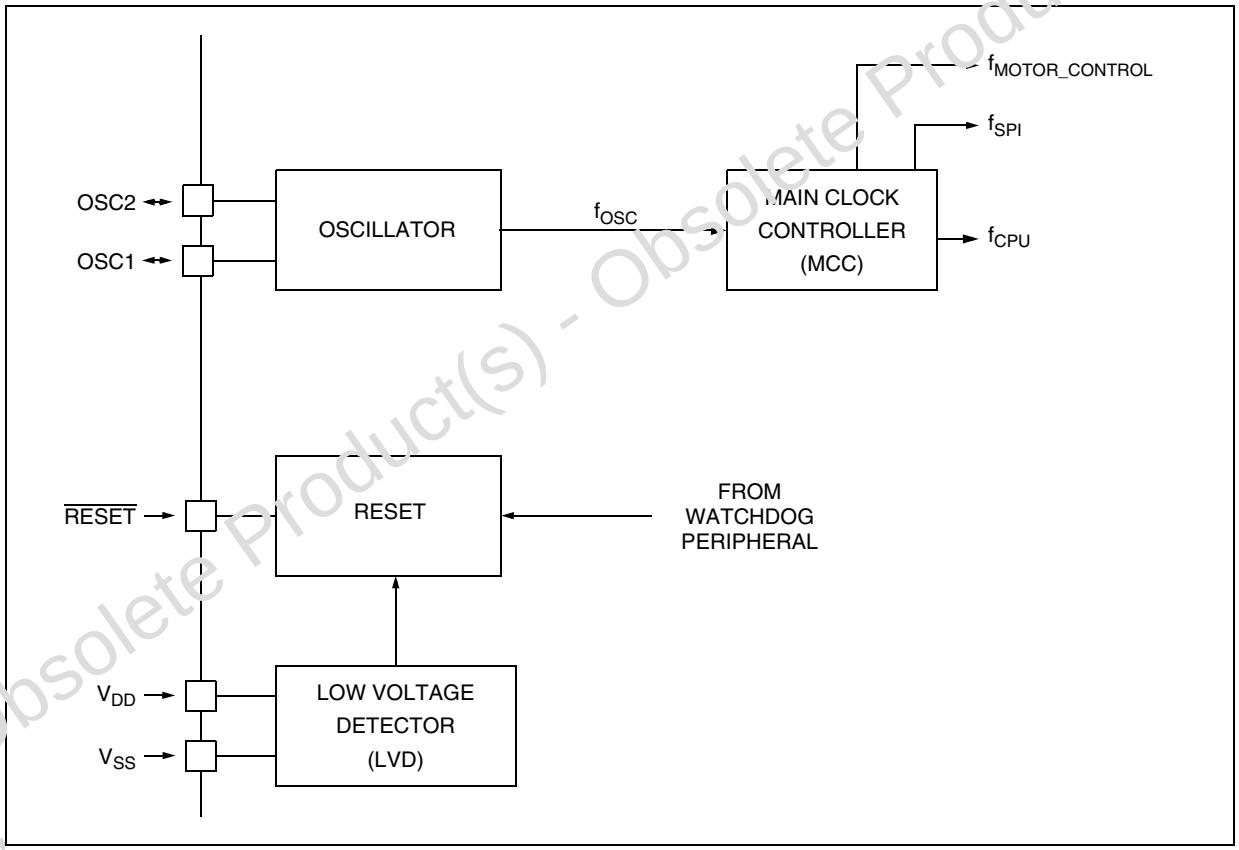
3 SUPPLY, RESET AND CLOCK MANAGEMENT

The ST72141K includes a range of utility features for securing the application in critical situations (for example in case of a power brown-out), and reducing the number of external components. An overview is shown in Figure 9.

Main Features

- Main supply low voltage detection (LVD)
- RESET Manager
- Low consumption resonator oscillator
- Main clock controller (MCC)

Figure 9. Clock, RESET, Option and Supply Management Overview

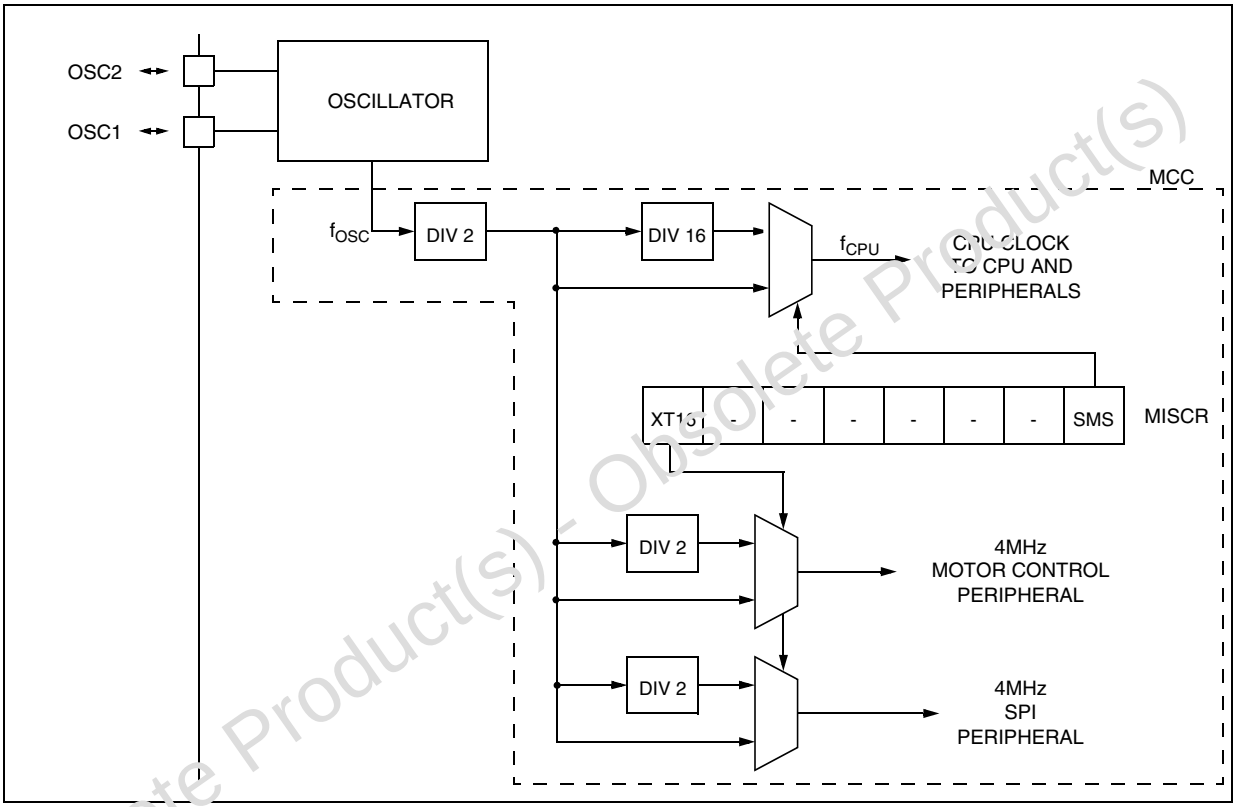


3.4 MAIN CLOCK CONTROLLER (MCC)

The MCC block supplies the clock for the ST7 CPU and its internal peripherals. It allows the SLOW power saving mode and the Motor Contral and SPI peripheral clocks to be managed independently. The MCC functionality is controlled by two bits of the MISCR register: SMS and XT16.

The XT16 bit acts on the clock of the motor control and SPI peripherals while the SMS bit acts on the CPU and the other peripherals.

Figure 17. Main Clock Controller (MCC) Block Diagram



INTERRUPTS (Cont'd)

Table 5. Interrupt Mapping

N°	Source Block	Description	Register Label	Priority Order	Exit from HALT	Address Vector
	RESET	Reset	N/A	Highest Priority	yes	FFFEh-FFFFh
	TRAP	Software Interrupt			no	FFFCh-FFFDh
0		Not used				FFFAh-FFFBh
1	EI0	External Interrupt Port A7..0 (C5..0*)	N/A		yes	FFFAh-FFFBh
2	EI1	External Interrupt Port B7..0 (C5..0*)			yes	FFF8h-FFF9h
3	MTC	Motor Control Interrupt (events: R, Z)	MISR		no	FFF4h-FFF5h
4		Motor Control Interrupt (events: C, D)			no	FFF2h-FFF3h
5		Motor Control Interrupt (events: E, O)			no	FFF0h-FFF1h
6	SPI	SPI Peripheral Interrupts	SPISR		no	FFEEh-FFEFh
7	TIMER A	TIMER A Peripheral Interrupts	TASR		no	FFECh-FFEDh
8	TIMER B	TIMER B Peripheral Interrupts	TBSR		no	FFEAh-FFEBh
9		Not used				FFE8h-FFE9h
10		Not used				FFE6h-FFE7h
11		Not used				FFE4h-FFE5h
12		Not Used		Lowest Priority		FFE2h-FFE3h
13		Not Used				FFE0h-FFE1h

I/O PORTS (Cont'd)

CAUTION: The alternate function must not be activated as long as the pin is configured as input with interrupt, in order to avoid generating spurious interrupts.

Analog alternate function

When the pin is used as an ADC input, the I/O must be configured as floating input. The analog multiplexer (controlled by the ADC registers) switches the analog voltage present on the selected pin to the common analog rail which is connected to the ADC input.

It is recommended not to change the voltage level or loading on any port pin while conversion is in progress. Furthermore it is recommended not to have clocking pins located close to a selected analog pin.

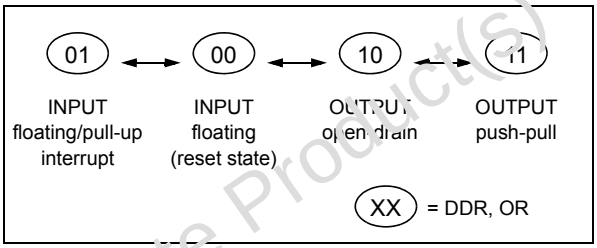
WARNING: The analog input voltage level must be within the limits stated in the absolute maximum ratings.

6.3 I/O PORT IMPLEMENTATION

The hardware implementation on each I/O port depends on the settings in the DDR and OR registers and specific feature of the I/O port such as ADC Input or true open drain.

Switching these I/O ports from one state to another should be done in a sequence that prevents unwanted side effects. Recommended safe transitions are illustrated in Figure 24 Other transitions are potentially risky and should be avoided, since they are likely to present unwanted side-effects such as spurious interrupt generation.

Figure 24. Interrupt I/O Port State Transitions



The I/O port register configurations are summarized as follows.

I/O PORTS (Cont'd)

Interrupt Ports

PA7:0, PB5:3 (with pull-up)

MODE	DDR	OR
floating input	0	0
pull-up interrupt input	0	1
open drain output	1	0
push-pull output	1	1

True Open Drain Interrupt Ports

PB2:0 (without pull-up)

MODE	DDR	OR
floating input	0	0
floating interrupt input	0	1
true open drain (high sink ports)	1	X

Table 8. Port Configuration

Port	Pin name	Input		Output	
		OR = 0	OR = 1	OR = 0	OR = 1
Port A	PA7:0	floating	pull-up interrupt	open drain	push-pull
Port B	PB5:3	floating	pull-up interrupt	open drain	push-pull
	PB2:0	floating	floating interrupt	true open drain	

MOTOR CONTROLLER (Cont'd)

Demagnetization (D) Event

At the end of the demagnetization phase, current no longer goes through the free-wheeling diodes. The voltage on the non-excited winding terminal goes from one of the power rail voltages to the common star connection voltage plus the BEMF voltage. In some cases (if the BEMF voltage is positive and the free-wheeling diodes are at ground for example) this end of demagnetization can be seen as a voltage edge on the selected MCIx input and it is called a hardware demagnetization event D_H. See Table 13.

If enabled by the HDM bit in the MCRB register, the current value of the MTIM timer is captured in register MDREG when this event occurs in order to be able to simulate the demagnetization phase for the next steps.

When enabled by the SDM bit in the MCRB register, demagnetization can also be simulated by comparing the MTIM timer with the MDREG register. This kind of demagnetization is called software demagnetization D_S.

If the HDM and SDM bits are both set, the first event that occurs, triggers a demagnetization event. For this to work correctly, a D_S event must not precede a D_H event because the latter could be detected as a Z event.

Software demagnetization can also be always used if the HDM bit is reset and the SDM bit is set. This mode works as a programmable masking time between the C and Z events. To drive the motor securely, the masking time must be always greater than the real demagnetization time in order to avoid a spurious Z event.

When an event occurs, (either D_H or D_S) the DI bit in the MISR register is set and an interrupt request is generated if the DIM bit of register MIMR is set.

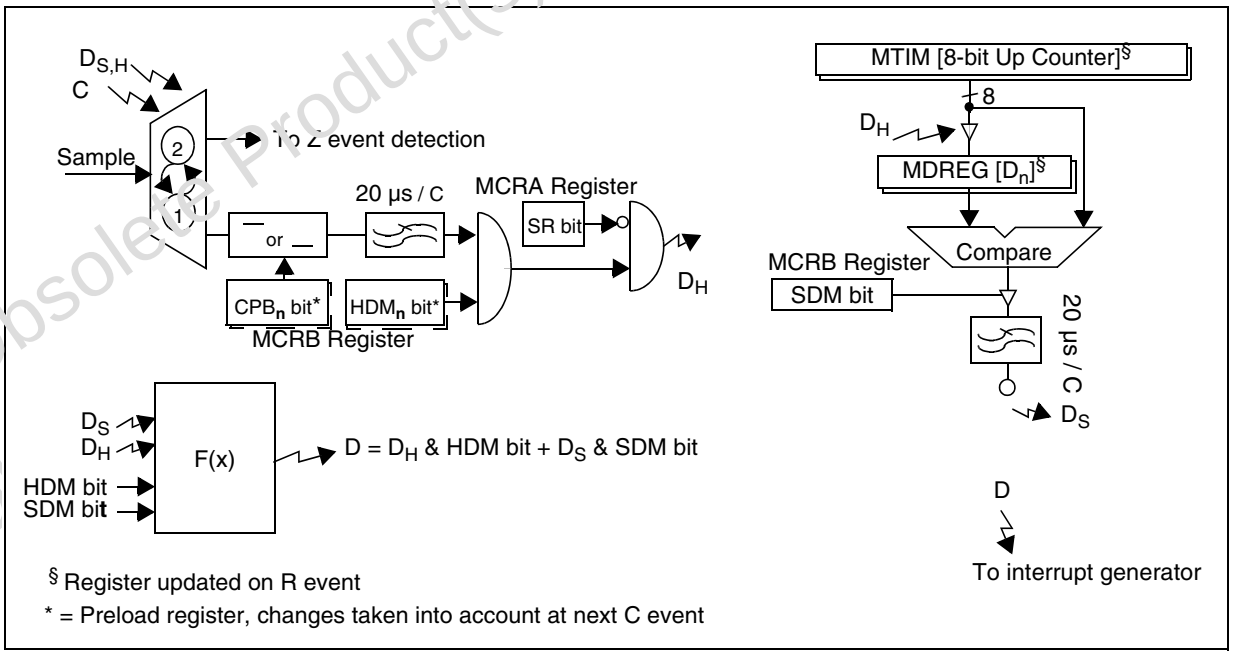
Warning 1: Due to the alternate automatic capture and compare of the MTIM timer with MDREG register by D_H and D_S events, the MDREG register should be manipulated with special care.

Warning 2: To avoid a system stop, the value written to the MDREG register in Soft Demagnetization Mode (SDM = 1) should always be:

– Greater than the MCOMP value of the commutation before the related demagnetization

– Greater than the value in the MTIM counter at that moment (when writing to the MDREG register).

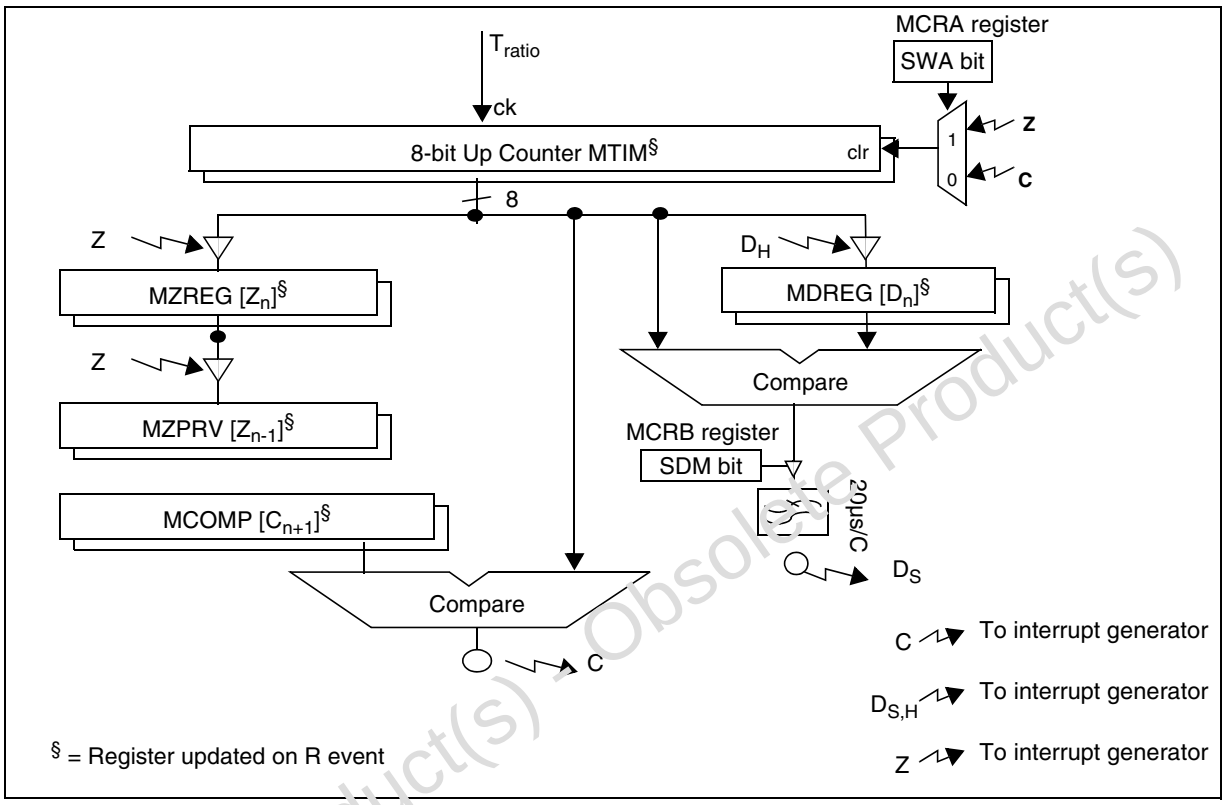
Figure 30. D Event Generation Mechanism



MOTOR CONTROLLER (Cont'd)

8.1.4.2 Delay Manager

Figure 33. Overview of MTIM Timer



This part of the MTC contains all the time-related functions, its architecture is based on an 8-bit shift left/shift right timer shown in Figure 33. The MTIM timer includes:

– An auto-updated prescaler

– A capture/compare register for software demagnetization simulation (MDREG)

– Two cascaded capture register (MZREG and MZPRV) for storing the times between two consecutive BEMF zero crossings (Z events)

– An 8x8 bit multiplier for auto computing the next commutation time

– One compare register for phase commutation generation (MCOMP)

The MTIM timer module can work in two main modes. In switched mode the user must process the step duration and commutation time by software, in autoswitched mode the commutation action is performed automatically depending on the rotor position information and register contents.

Table 17. Switched and Autoswitched Modes

SWA bit	Commutation Type	MCOMP User access
0	Switched mode	Read/Write
1	Autoswitched mode	Read only

Switched Mode

This feature allows the motor to be run step-by-step. This is useful when the rotor speed is still too low to generate a BEMF. It can also run other kinds of motor without BEMF generation such as induction motors or switch reluctance motors. This mode can also be used for autoswitching with all computation for the next commutation time done by software (hardware multiplier not used) and using the powerful interrupt set of the peripheral.

In this mode, the step time is directly written by software in the commutation compare register MCOMP. When the MTIM timer reaches this value a commutation occurs (C event) and the MTIM timer is reset.

MOTOR CONTROLLER (Cont'd)

Table 21. Step Frequency/Period Range

Step Ratio Bits ST[3:0]	Maximum Step Frequency	Minimum Step Frequency	Minimum Step Period	Maximum Step Period
0000	23.5 kHz	7.85 kHz	42.5 µs	127.5 µs
0001	11.7 kHz	3.93 kHz	85 µs	255 µs
0010	5.88 kHz	1.96 kHz	170 µs	510 µs
0011	2.94 kHz	980 Hz	340 µs	1.02 ms
0100	1.47 kHz	490 Hz	680 µs	2.04 ms
0101	735 Hz	245 Hz	1.36 ms	4.08 ms
0110	367 Hz	123 Hz	2.72 ms	8.16 ms
0111	183 Hz	61.3 Hz	5.44 ms	16.32 ms
1000	91.9 Hz	30.7 Hz	10.9 ms	32.6 ms
1001	45.9 Hz	15.4 Hz	21.8 ms	65.2 ms
1010	22.9 Hz	7.66 Hz	43.6 ms	130 ms
1011	11.4 Hz	3.83 Hz	87 ms	261 ms
1100	5.74 Hz	1.92 Hz	174 ms	522 ms
1101	2.87 Hz	0.958 Hz	349 ms	1.04 s
1110	1.43 Hz	0.479 Hz	697 ms	2.08 s
1111	0.718 Hz	0.240 Hz	1.40 s	4.17 s

Table 22. Modes of Accessing MTIM Timer-Related Registers

State of MCRA Register Bits				Access to MTIM Timer Related Registers	
RST bit	SWA bit	MOE bit	Mode	Read Only Access	Read / Write Access
0	0	0	Configuration Mode		MTIM, MZPRV, MZREG, MCOMP, MDREG, ST[3:0]
0	0	1	Switched Mode	MTIM, MZPRV, MZREG, ST[3:0]	MCOMP, MDREG, RMI bit of MISR: 0: No action 1: Decrement ST[3:0] RPI bit of MISR: 0: No action 1: Increment ST[3:0]
0	1	0	Emergency Stop		MTIM, MZPRV, MZREG, MCOMP, MDREG, ST[3:0]
0	1	1	Autoswitched Mode	MTIM, MZPRV, MZREG, MCOMP, ST[3:0]	MDREG,RMI, RPI bit of MISR: Set by hardware, (increment ST[3:0]) Cleared by software

MOTOR CONTROLLER (Cont'd)

Table 32. Multiplier Result

DCB bit	Commutation Delay
0	MCOMP = MWGHT x MZPRV / 32
1	MCOMP = MWGHT x MZREG / 32

CONTROL REGISTER B (MCRB)
Read/Write
Reset Value: 0000 0000 (00h)

7							0
VR1	VR0	CPB*	HDM*	SDM*	OS2*	OS1	OS0

Bits 7:6 = **VR[1:0]**: *BEMF/demagnetization Reference threshold*

These bits select the V_{REF} value as shown in the following table.

VR1	VR0	V_{REF} Voltage threshold
0	0	0.2V
0	1	0.6V
1	0	1.2V
1	1	2.5V

Bit 5 = **CPB***: *Compare Bit for Zero-crossing detection.*
0: Zero crossing detection on falling edge
1: Zero crossing detection on rising edge

Bit 4 = **HDM***: *Hardware Demagnetization event Mask bit*
0: Hardware Demagnetization disabled
1: Hardware Demagnetization enabled

Bit 3 = **SDM***: *Software Demagnetization event Mask bit*
0: Software Demagnetization disabled
1: Software Demagnetization enabled

Bits 2:0 = **OS2*,OS[1:0]**: *Operating output mode Selection bits*

Refer to the Step behaviour diagrams (Figure 40, Figure 41, Figure 42) and Table 33.

These bits are used to configure the various PWM output configurations.

Note: The OS2 bit is the only one with a preload register.

Table 33. Step Behaviour Summary

Mode		OS2 bit	PWM after C and before D	OS [1:0] bits	PWM after D and before C
Voltage mode(V0C1=0)	Sensorless (SR=0)	0	Same as after D and before C	00	On even channels
				01	On odd channels
				10	Continuous
				11	All active channels
		1	Alternate	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels
	Sensor (SR=1)	x	Unused	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels
Current mode (V0C1=1)	Sensorless (SR=0)	0	On even Channels	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels
		1	On odd channels	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels
	Sensor (SR=1)	x	Unused	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels

Note: For more details, see Step behaviour diagrams (Figure 40, Figure 41, and Figure 42).

* Preload bits, new value taken into account at next C event.

MOTOR CONTROLLER (Cont'd)

Note: The CPB, HDM, SDM, OS2 bits in the MCRB and the bits OE[5:0] are marked with *. It means that these bits are taken into account at the following commutation event (in normal mode) or when a value is written in the MPHST register when in direct access mode. For more details, refer to the description of the DAC bit in the MCRA register. The use of a Preload register allows all the registers to be updated at the same time.

Warning: Access to Preload registers

Special care has to be taken with Preload registers, especially when using the ST7 BSET and BRES instructions on MTC registers.

For instance, while writing to the MPHST register, you will write the value in the preload register. However, while reading at the same address, you will get the current value in the register and not the value of the preload register.

All preload registers are loaded in the real registers at the same time. In normal mode this is done automatically when a C event occurs, however in direct access mode (DAC bit=1) the preload registers are loaded as soon as a value is written in the MPHST register.

MOTOR CONTROLLER (Cont'd)

Table 38. MTC Register Map and Reset Values

Address (Hex.)	Register Name	7	6	5	4	3	2	1	0
0060h	**MTIM** Reset Value	T7 0	T6 0	T5 0	T4 0	T3 0	T2 0	T1 0	T0 0
0061h	**MZPRV** Reset Value	ZP7 0	ZP6 0	ZP5 0	ZP4 0	ZP3 0	ZP2 0	ZP1 0	ZP0 0
0062h	**MZREG** Reset Value	ZC7 0	ZC6 0	ZC5 0	ZC4 0	ZC3 0	ZC2 0	ZC1 0	ZC0 0
0063h	**MCOMP** Reset Value	DC7 0	DC6 0	DC5 0	DC4 0	DC3 0	DC2 0	DC1 0	DC0 0
0064h	**MDREG** Reset Value	DN7 0	DN6 0	DN5 0	DN4 0	DN3 0	DN2 0	DN1 0	DN0 0
0065h	**MWGHT** Reset Value	AN7 0	AN6 0	AN5 0	AN4 0	AN3 0	AN2 0	AN1 0	AN0 0
0066h	**MPRSR** Reset Value	SA3 0	SA2 0	SA1 0	SA0 0	ST3 0	ST2 0	ST1 0	ST0 0
0067h	**MIMR** Reset Value	HST 0	CL 0	RIM 0	OIM 0	EIM 0	ZIM 0	DIM 0	CIM 0
0068h	**MISR** Reset Value	0	RPI 0	RMI 0	OI 0	EI 0	ZI 0	DI 0	CI 0
0069h	**MCRA** Reset Value	MOE 0	RST 0	SR 0	DAC 0	V0C1 0	SWA 0	CFF 0	DCB 0
006Ah	**MCRB** Reset Value	VR1 0	VR0 0	CPB 0	HDM 0	SDM 0	OS2 0	OS1 0	OS0 0
006Bh	**MPHST** Reset Value	IS1 0	IS0 0	OO5 0	OO4 0	OO3 0	OO2 0	OO1 0	OO0
006Ch	**MZAR** Reset Value	ZVD 0	REO 0	OE5 0	OE4 0	OE3 0	OE2 0	OE1 0	OE0 0
006Dh	**MPOL** Reset Value	OT1 0	OT0 0	OP5 0	OP4 0	OP3 0	OP2 0	OP1 0	OP0 0

Related Documentation

AN1082: Description of the ST72141 Motor Control Peripherals

AN1083: ST72141 BLDC Motor Control Software and Flowchart Example

AN1129: PWM Management for BLDC Motor Drives Using the ST72141

AN1130: An Introduction to Sensorless Brushless DC Motor Drive Applications with the ST72141

AN1276: BLDC Motor Start Routine for the ST72141 Microcontroller

AN1321: Using the ST72141 Motor Control MCU in Sensor Mode

WATCHDOG TIMER (Cont'd)

8.2.3 Functional Description

The counter value stored in the CR register (bits T6:T0), is decremented every 12288 machine cycles, and the length of the timeout period can be programmed by the user in 64 increments.

If the watchdog is activated (the WDGA bit is set) and when the 7-bit timer (bits T6:T0) rolls over from 40h to 3Fh (T6 become cleared), it initiates a reset cycle pulling low the reset pin for typically 500ns.

The application program must write in the CR register at regular intervals during normal operation to prevent an MCU reset. The value to be stored in the CR register must be between FFh and C0h (see Table 39 . Watchdog Timing (fCPU = 8 MHz)):

– The WDGA bit is set (watchdog enabled)

– The T6 bit is set to prevent generating an immediate reset

– The T5:T0 bits contain the number of increments which represents the time delay before the watchdog produces a reset.

Table 39. Watchdog Timing (f_{CPU} = 8 MHz)

	CR Register initial value	WDG timeout period (ms)
Max	FFh	98.304
Min	C0h	1.536

Notes: Following a reset, the watchdog is disabled. Once activated it cannot be disabled, except by a reset.

The T6 bit can be used to generate a software reset (the WDGA bit is set and the T6 bit is cleared).

If the watchdog is activated, the HALT instruction will generate a Reset.

8.2.4 Low Power Modes

Mode	Description
WAIT	No effect on Watchdog.
HALT	Immediate reset generation as soon as the HALT instruction is executed if the Watchdog is activated (WDGA bit is set).

8.2.5 Interrupts

None.

8.2.6 Register Description

CONTROL REGISTER (CR)

Read/Write

Reset Value: 0111 1111 (7Fh)

7							0
WDGA	T6	T5	T4	T3	T2	T1	T0

Bit 7= **WDGA** *Activation bit.*
This bit is set by software and only cleared by hardware after a reset. When WDGA = 1, the watchdog can generate a reset.
0: Watchdog disabled
1: Watchdog enabled

Bit 6:0 = **T[6:0]** *7 bit timer (MSB to LSB).*
These bits contain the decremented value. A reset is produced when it rolls over from 40h to 3Fh (T6 becomes cleared) if WDGA=1.

STATUS REGISTER (SR)

Read/Write

Reset Value*: xxxx xxxx0

7							0
-	-	-	-	-	-	-	WDOGF

Bit 0 = **WDOGF** *Watchdog flag.*
This bit is set by a watchdog reset and cleared by software or a power on/off reset. This bit is useful for distinguishing power/on off or external reset and watchdog reset.
0: No Watchdog reset occurred
1: Watchdog reset occurred

* Only by software and power on/off reset

16-BIT TIMER (Cont'd)

Figure 49. Input Capture Block Diagram

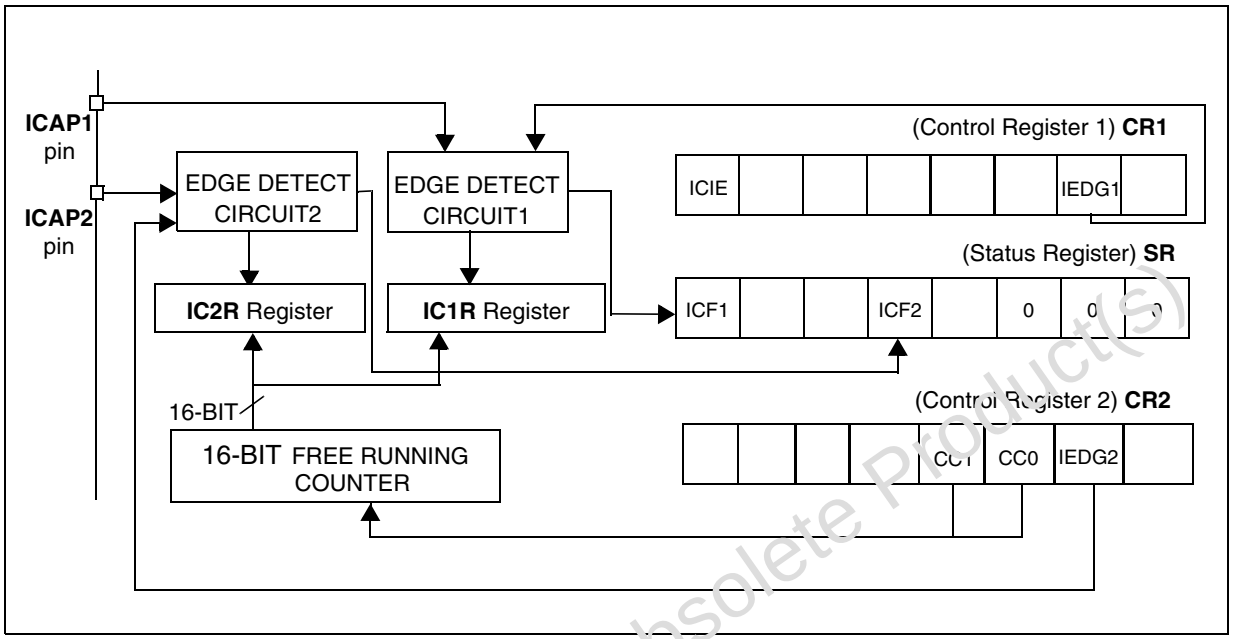
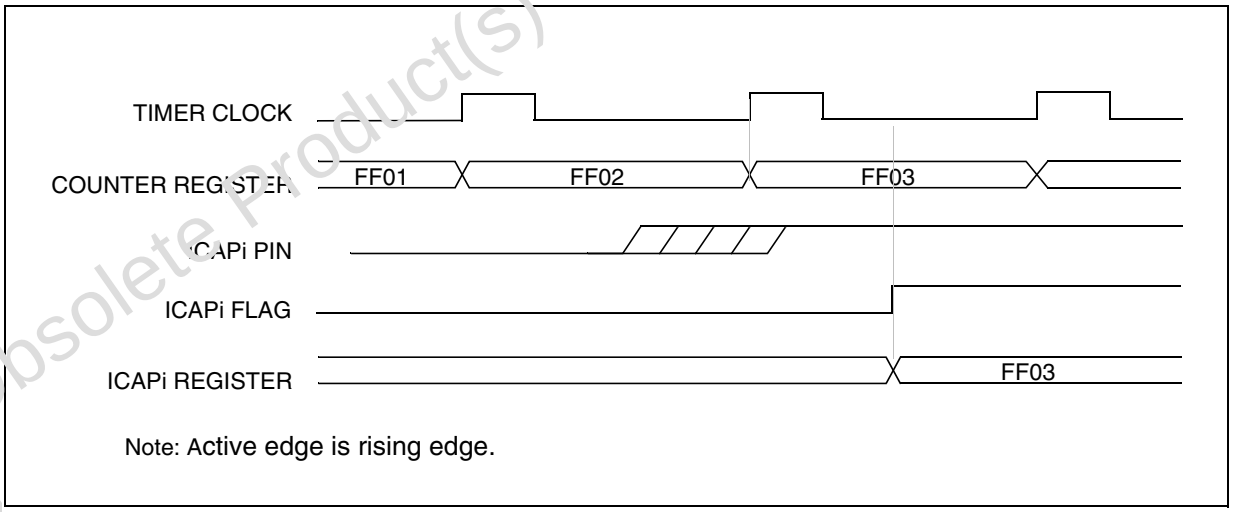


Figure 50. Input Capture Timing Diagram



Note: Active edge is rising edge.

16-BIT TIMER (Cont'd)

Notes:

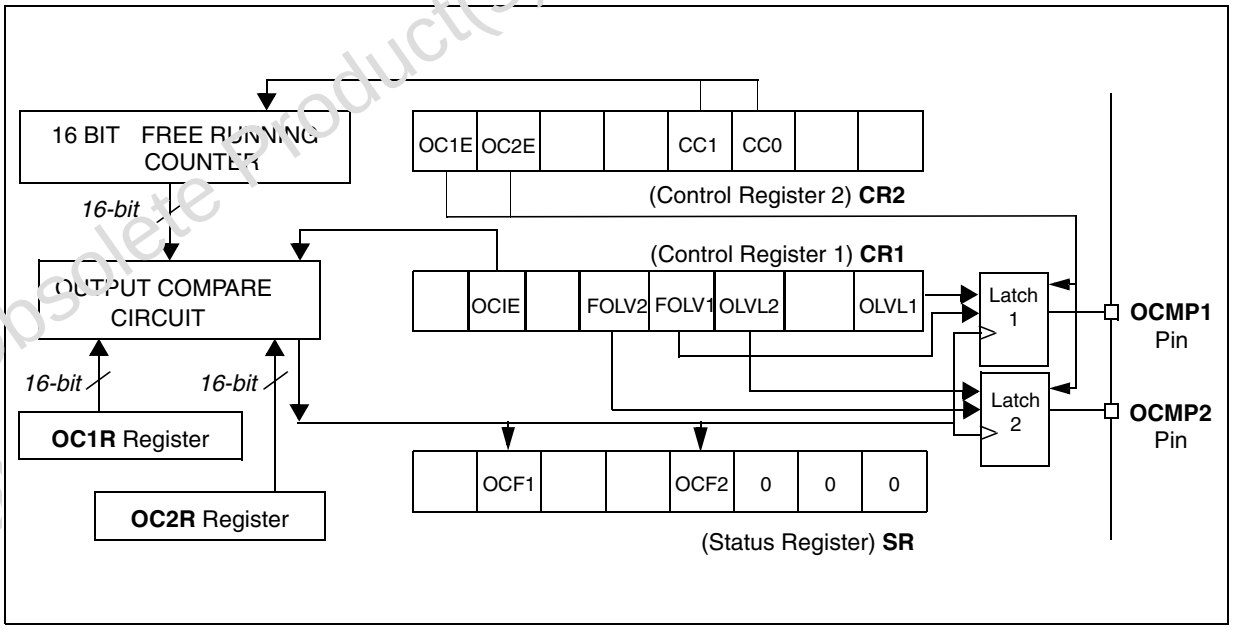
1. After a processor write cycle to the OC*i*HR register, the output compare function is inhibited until the OC*i*LR register is also written.
2. If the OC*i*E bit is not set, the OCMP*i* pin is a general I/O port and the OLVL*i* bit will not appear when a match is found but an interrupt could be generated if the OCIE bit is set.
3. When the timer clock is $f_{CPU}/2$, OCF*i* and OCMP*i* are set while the counter value equals the OC*i*R register value (see Figure 52). This behaviour is the same in OPM or PWM mode. When the timer clock is $f_{CPU}/4$, $f_{CPU}/8$ or in external clock mode, OCF*i* and OCMP*i* are set while the counter value equals the OC*i*R register value plus 1 (see Figure 53).
4. The output compare functions can be used both for generating external events on the OCMP*i* pins even if the input capture mode is also used.
5. The value in the 16-bit OC*i*R register and the OLV*i* bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed timeout.

Forced Compare Output capability

When the FOLV*i* bit is set by software, the OLVL*i* bit is copied to the OCMP*i* pin. The OLV*i* bit has to be toggled in order to toggle the OCMP*i* pin when it is enabled (OC*i*E bit=1). The OCF*i* bit is then not set by hardware, and thus no interrupt request is generated.

FOLVL*i* bits have no effect in either One-Pulse mode or PWM mode.

Figure 51. Output Compare Block Diagram



16-BIT TIMER (Cont'd)

8.3.4 Low Power Modes

Mode	Description
WAIT	No effect on 16-bit Timer. Timer interrupts cause the device to exit from WAIT mode.
HALT	16-bit Timer registers are frozen. In HALT mode, the counter stops counting until Halt mode is exited. Counting resumes from the previous count when the MCU is woken up by an interrupt with "exit from HALT mode" capability or from the counter reset value when the MCU is woken up by a RESET. If an input capture event occurs on the ICAP*i* pin, the input capture detection circuitry is armed. Consequently, when the MCU is woken up by an interrupt with "exit from HALT mode" capability, the ICF*i* bit is set, and the counter value present when exiting from HALT mode is captured into the IC*i*R register.

8.3.5 Interrupts

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
Input Capture 1 event/Counter reset in PWM mode	ICF1	ICIE	Yes	No
Input Capture 2 event	ICF2		Yes	No
Output Compare 1 event (not available in PWM mode)	OCF1	OCIE	Yes	No
Output Compare 2 event (not available in PWM mode)	OCF2		Yes	No
Timer Overflow event	TOF	TOIE	Yes	No

Note: The 16-bit Timer interrupt events are connected to the same interrupt vector (see Interrupts chapter). These events generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

8.3.6 Summary of Timer modes

MODES	AVAILABLE RESOURCES			
	Input Capture 1	Input Capture 2	Output Compare 1	Output Compare 2
Input Capture (1 and/or 2)	Yes	Yes	Yes	Yes
Output Compare (1 and/or 2)	Yes	Yes	Yes	Yes
One Pulse mode	No	Not Recommended[1)]	No	Partially [2)]
PWM Mode	No	Not Recommended[3)]	No	No

1) See note 4 in Section 8.3.3.5 One Pulse Mode

2) See note 5 in Section 8.3.3.5 One Pulse Mode

3) See note 4 in Section 8.3.3.6 Pulse Width Modulation Mode

16-BIT TIMER (Cont'd)

Table 42. 16-Bit Timer Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
Timer A: 32 Timer B: 42	**CR1** Reset Value	ICIE 0	OCIE 0	TOIE 0	FOLV2 0	FOLV1 0	OLVL2 0	IEDG1 0	OLVL1 0
Timer A: 31 Timer B: 41	**CR2** Reset Value	OC1E 0	OC2E 0	OPM 0	PWM 0	CC1 0	CC0 0	IEDG2 0	EXEDG 0
Timer A: 33 Timer B: 43	**SR** Reset Value	ICF1 0	OCF1 0	TOF 0	ICF2 0	OCF2 0	- 0	- 0	- 0
Timer A: 34 Timer B: 44	**ICHR1** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 35 Timer B: 45	**ICLR1** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 36 Timer B: 46	**OCHR1** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 37 Timer B: 47	**OCLR1** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 3E Timer B: 4E	**OCHR2** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 3F Timer B: 4F	**OCLR2** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 38 Timer B: 48	**CHR** Reset Value	MSB 1	1	1	1	1	1	1	LSB 1
Timer A: 39 Timer B: 49	**CLR** Reset Value	MSB 1	1	1	1	1	1	0	LSB 0
Timer A: 3A Timer B: 4A	**ACHR** Reset Value	MSB 1	1	1	1	1	1	1	LSB 1
Timer A: 3B Timer B: 4B	**ACLR** Reset Value	MSB 1	1	1	1	1	1	0	LSB 0
Timer A: 3C Timer B: 4C	**ICHR2** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 3D Timer B: 4D	**ICLR2** Reset Value	MSB -	-	-	-	-	-	-	LSB -

SERIAL PERIPHERAL INTERFACE (Cont'd)

8.4.4.4 Write Collision Error

A write collision occurs when the software tries to write to the DR register while a data transfer is taking place with an external device. When this happens, the transfer continues uninterrupted; and the software write will be unsuccessful.

Write collisions can occur both in master and slave mode.

Note: a "read collision" will never occur since the received data byte is placed in a buffer in which access is always synchronous with the MCU operation.

In Slave mode

When the CPHA bit is set:

The slave device will receive a clock (SCK) edge prior to the latch of the first data transfer. This first clock edge will freeze the data in the slave device DR register and output the MSBit on to the external MISO pin of the slave device.

The $\overline{SS}$ pin low state enables the slave device but the output of the MSBit onto the MISO pin does not take place until the first data transfer clock edge.

When the CPHA bit is reset:

Data is latched on the occurrence of the first clock transition. The slave device does not have any way of knowing when that transition will occur; therefore, the slave device collision occurs when software attempts to write the DR register after its $\overline{SS}$ pin has been pulled low.

For this reason, the $\overline{SS}$ pin must be high, between each data byte transfer, to allow the CPU to write in the DR register without generating a write collision.

In Master mode

Collision in the master device is defined as a write of the DR register while the internal serial clock (SCK) is in the process of transfer.

The $\overline{SS}$ pin signal must be always high on the master device.

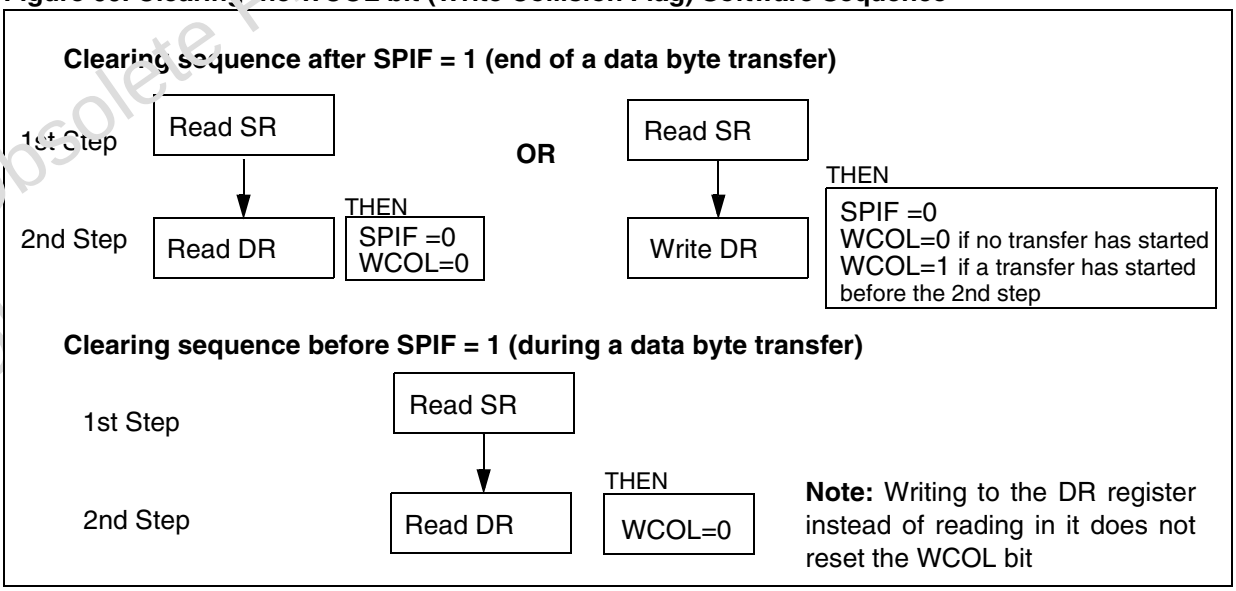
WCOL bit

The WCOL bit in the SR register is set if a write collision occurs.

No SPI interrupt is generated when the WCOL bit is set (the WCOL bit is a status flag only).

Clearing the WCOL bit is done through a software sequence (see Figure 60).

Figure 60. Clearing the WCOL bit (Write Collision Flag) Software Sequence



ST7 ADDRESSING MODES (Cont'd)

9.1.6 Indirect Indexed (Short, Long)

This is a combination of indirect and short indexed addressing modes. The operand is referenced by its memory address, which is defined by the unsigned addition of an index register value (X or Y) with a pointer value located in memory. The pointer address follows the opcode.

The indirect indexed addressing mode consists of two sub-modes:

Indirect Indexed (Short)

The pointer address is a byte, the pointer size is a byte, thus allowing 00 - 1FE addressing space, and requires 1 byte after the opcode.

Indirect Indexed (Long)

The pointer address is a byte, the pointer size is a word, thus allowing 64 Kbyte addressing space, and requires 1 byte after the opcode.

Table 48. Instructions Supporting Direct, Indexed, Indirect and Indirect Indexed Addressing Modes

Long and Short Instructions	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Addition/subtraction operations
BCP	Bit Compare

Short Instructions Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

9.1.7 Relative Mode (Direct, Indirect)

This addressing mode is used to modify the PC register value by adding an 8-bit signed offset to it.

Available Relative Direct/ Indirect Instructions	Function
JRxx	Conditional Jump
CALLR	Call Relative

The relative addressing mode consists of two submodes:

Relative (Direct)

The offset follows the opcode.

Relative (Indirect)

The offset is defined in memory, of which the address follows the opcode.

10.7 PERIPHERAL CHARACTERISTICS

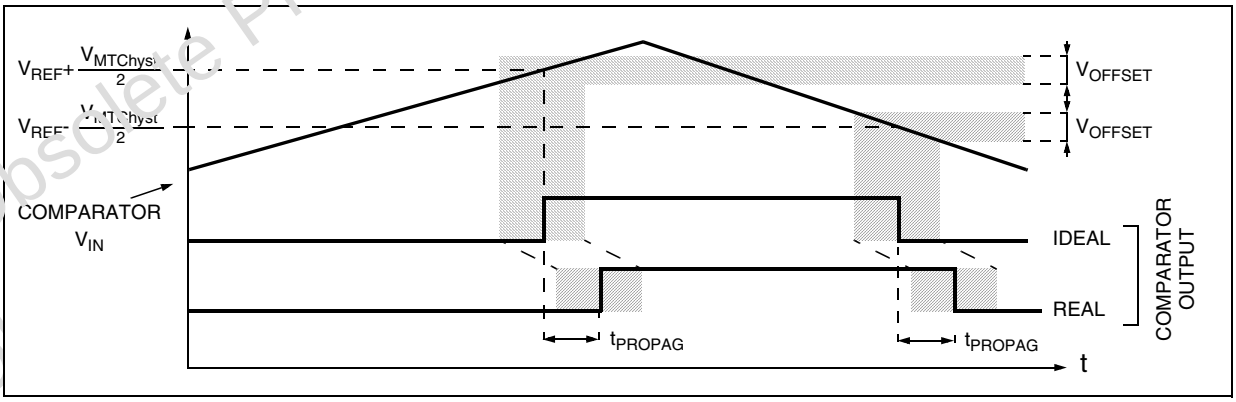
WATCHDOG						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
$t_{w(WDG)}$	Watchdog time-out duration		12,288		786,432	t_{CPU}
		f_{CPU}=8MHz	1.54		98.3	ms
t_{WDGRST}	Watchdog RESET pulse width			500		ns

Recommended operating conditions with T_A=-40 to +125°C and V_{DD}-V_{SS}=5V unless otherwise specified.

MOTOR CONTROL						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ** [1]	**Max**	**Unit**
V_{OFFSET}	Comparator offset error			<10	100	mV
$V_{MTChyst}$	MCIA/B/C comparator hysteresis [2]		35	80	130	mV
t_{PROPAG}	Comparator propagation delay				1	µs
$\frac{\Delta V_{REF}}{V_{REF}}$	Reference voltage tolerance				5	%
R1	V_{CREF} resistance bridge			30		kΩ
R2				70		
$\alpha=\frac{R2}{R1+R2}$				0.7		
$\Delta\alpha/\alpha$	α tolerance				5	%

Note:
1) Unless otherwise specified, typical data is based on T_A = 25° C and V_{DD}-V_{SS} = 5 V. This data is provided only as design guidelines and are not tested.
2) The $V_{MTChyst}$ hysteresis is constant.

Figure 64. Motor Control Comparator Characteristics



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