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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16e5-aur

5. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

5.1 Recommended Reading

- XMEGA E Manual
- XMEGA Application Notes

This device data sheet only contains part specific information with a short description of each peripheral and module. The XMEGA E Manual describes the modules and peripherals in depth. The XMEGA application notes contain example code and show applied use of the modules and peripherals.

All documentations are available from www.atmel.com/avr.

6. Capacitive Touch Sensing

The Atmel QTouch® library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR® microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression™ (AKS™) technology for unambiguous detection of key events. The QTouch library includes support for the QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The Atmel QTouch library is FREE and downloadable from the Atmel website at the following location: http://www.atmel.com/tools/QTOUCHLIBRARY.aspx. For implementation details and other information, refer to the Atmel QTouch library user guide - also available for download from the Atmel website.

the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 71.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 8-1.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 8-1. Device ID Bytes for Atmel AVR XMEGA E5 Devices

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega32E5	4C	95	1E
ATxmega16E5	45	94	1E
ATxmega8E5	41	93	1E

8.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

8.4 Fuses and Lock Bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, startup configuration, etc.

The lock bits are used to set protection levels for the different flash sections (i.e., if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

An un-programmed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are reprogrammable like the flash program memory.

8.10 Device ID and Revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

8.11 I/O Memory Protection

Some features in the device are regarded as critical for safety in some applications. Due to this, it is possible to lock the I/O register related to the clock system, the event system, and the waveform extensions. As long as the lock is enabled, all related I/O registers are locked and they cannot be written from the application software. The lock registers themselves are protected by the configuration change protection mechanism.

8.12 Flash and EEPROM Page Size

The flash program memory and EEPROM data memory are organized in pages. The pages are word accessible for the flash and byte accessible for the EEPROM.

Table 8-2 shows the Flash Program Memory organization and Program Counter (PC) size. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) give the page number and the least significant address bits (FWORD) give the word in the page.

Table 8-2. Number of Words and Pages in the Flash

Devices	PC size	Flash size	Page Size	FWORD	FPAGE	Application		Boot	
	bits	bytes	words			Size	No. of pages	Size	No. of pages
ATxmega32E5	15	32K+4K	64	Z[6:0]	Z[14:7]	32K	256	4K	32
ATxmega16E5	14	16K+4K	64	Z[6:0]	Z[13:7]	16K	128	4K	32
ATxmega8E5	13	8K+2K	64	Z[6:0]	Z[12:7]	8K	64	2K	16

Table 8-3 shows EEPROM memory organization for the Atmel AVR XMEGA E5 devices. EEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM address register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

Table 8-3. Number of Words and Pages in the EEPROM

Devices	EEPROM	Page Size	E2BYTE	E2PAGE	No. of Pages
	Size	bytes			
ATxmega32E5	1K	32	ADDR[4:0]	ADDR[10:5]	32
ATxmega16E5	512Bytes	32	ADDR[4:0]	ADDR[10:5]	16
ATxmega8E5	512Bytes	32	ADDR[4:0]	ADDR[10:5]	16

10. Event System

10.1 Features

- System for direct peripheral-to-peripheral communication and signaling
- Peripherals can directly send, receive, and react to peripheral events
  - CPU and EDMA controller independent operation
  - 100% predictable signal timing
  - Short and guaranteed response time
  - Synchronous and asynchronous event routing
- Eight event channels for up to eight different and parallel signal routing and configurations
- Events can be sent and/or used by most peripherals, clock system, and software
- Additional functions include
  - Quadrature decoder with rotary filtering
  - Digital filtering of I/O pin state with configurable filter
  - Simultaneous synchronous and asynchronous events provided to peripheral
- Works in all sleep modes

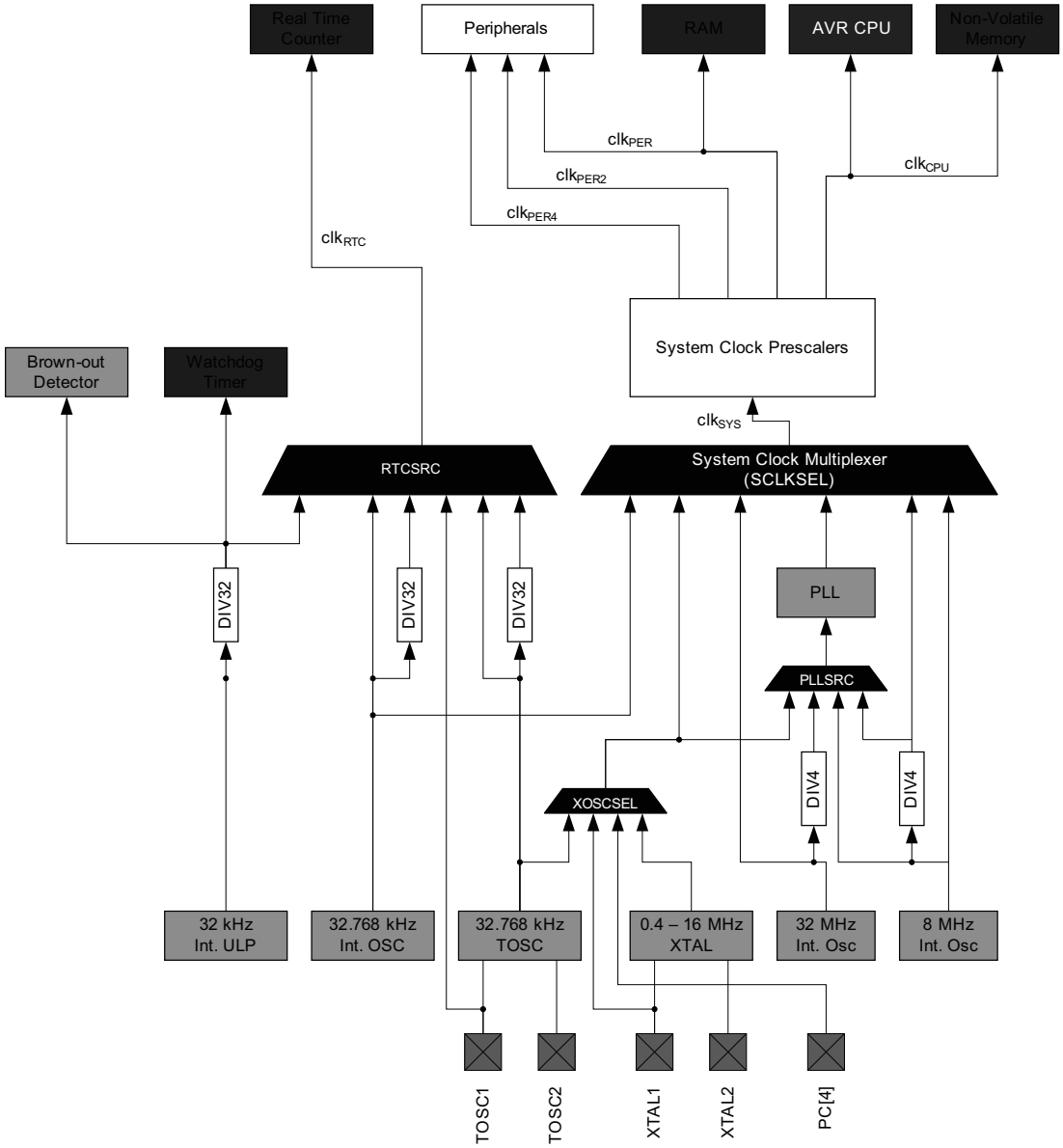
10.2 Overview

The event system enables direct peripheral-to-peripheral communication and signaling. It allows a change in one peripheral's state to automatically trigger actions in other peripherals. It is designed to provide a predictable system for short and predictable response times between peripherals. It allows for autonomous peripheral control and interaction without the use of interrupts, CPU, or EDMA controller resources, and is thus a powerful tool for reducing the complexity, size and execution time of application code. It allows for synchronized timing of actions in several peripheral modules. The event system enables also asynchronous event routing for instant actions in peripherals.

A change in a peripheral's state is referred to as an event, and usually corresponds to the peripheral's interrupt conditions. Events can be directly passed to other peripherals using a dedicated routing network called the event routing network. How events are routed and used by the peripherals is configured in software.

Figure 10-1 shows a basic diagram of all connected peripherals. The event system can directly connect together analog and digital converters, analog comparators, I/O port pins, the real-time counter, timer/counters, IR communication module (IRCOM), and XMEGA Custom Logic (programmable logic) block (XCL). It can also be used to trigger EDMA transactions (EDMA controller). Events can also be generated from software and peripheral clock.

Figure 11-1. The Clock System, Clock Sources, and Clock Distribution



11.3 Clock Sources

The clock sources are divided in two main groups: internal oscillators and external clock sources. Most of the clock sources can be directly enabled and disabled from software, while others are automatically enabled or disabled, depending on peripheral settings. After reset, the device starts up running from the 2MHz output of the 8MHz internal oscillator. The other clock sources, DFLL and PLL, are turned off by default.

The internal oscillators do not require any external components to run. For details on characteristics and accuracy of the internal oscillators, refer to the device datasheet.

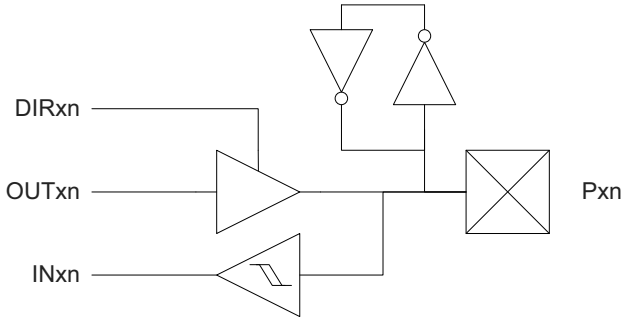
11.3.1 32kHz Ultra Low Power Internal Oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz ultra low power (ULP) internal oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built-in prescaler that provides a 1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device. This oscillator can be selected as the clock source for the RTC.

16.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 16-4. I/O Configuration - Totem-pole with Bus-keeper



16.3.5 Others

Figure 16-5. Output Configuration - Wired-OR with Optional Pull-down

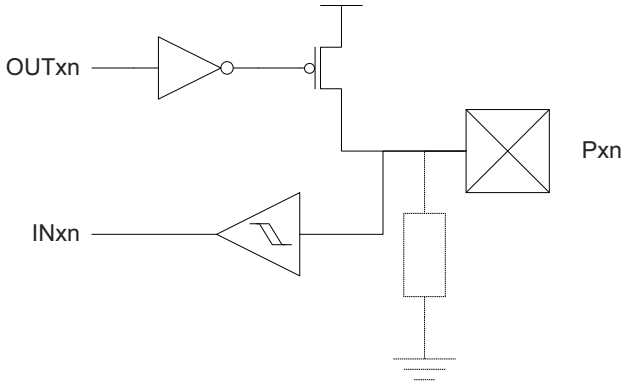
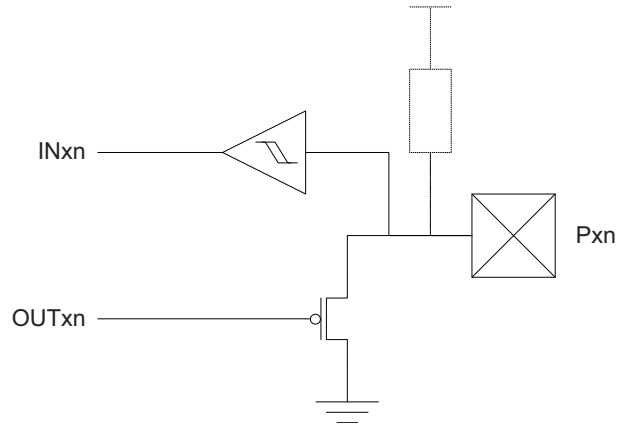


Figure 16-6. I/O Configuration - Wired-AND with Optional Pull-up



18. WeX – Waveform Extension

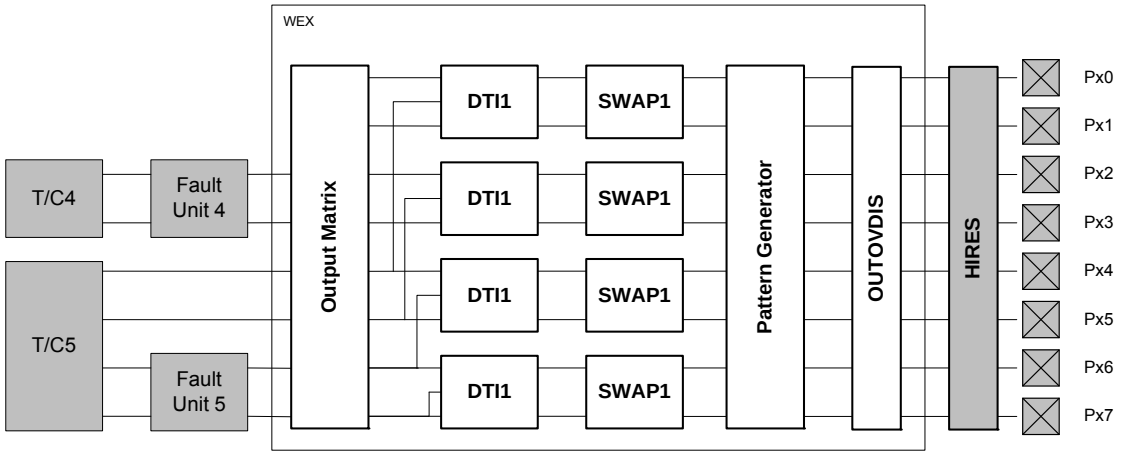
18.1 Features

- Module for more customized and advanced waveform generation
  - Optimized for various type of motor, ballast, and power stage control
- Output matrix for timer/counter waveform output distribution
  - Configurable distribution of compare channel output across port pins
  - Redistribution of dead-time insertion resource between TC4 and TC5
- Four dead-time insertion (DTI) units, each with
  - Complementary high and low side with non overlapping outputs
  - Separate dead-time setting for high and low side
  - 8-bit resolution
- Four swap (SWAP) units
  - Separate port pair or low high side drivers swap
  - Double buffered swap feature
- Pattern generation creating synchronized bit pattern across the port pins
  - Double buffered pattern generation

18.2 Overview

The waveform extension (WEX) provides extra functions to the timer/counter in waveform generation (WG) modes. It is primarily intended for motor control, ballast, LED, H-bridge, power converters, and other types of power control applications. The WEX consist of five independent and successive units, as shown in Figure 18-1.

Figure 18-1. Waveform Extension and Closely Related Peripherals



The output matrix (OTMX) can distribute and route out the waveform outputs from timer/counter 4 and 5 across the port pins in different configurations, each optimized for different application types. The dead time insertion (DTI) unit splits the four lower OTMX outputs into a two non-overlapping signals, the non-inverted low side (LS) and inverted high side (HS) of the waveform output with optional dead-time insertion between LS and HS switching.

The swap (SWAP) unit can swap the LS and HS pin position. This can be used for fast decay motor control. The pattern generation unit generates synchronized output waveform with constant logic level. This can be used for easy stepper motor and full bridge control.

26. XCL – XMEGA Custom Logic Module

26.1 Features

- Two independent 8-bit timer/counter with:
  - Period and compare channel for each timer/counter
  - Input Capture for each timer
  - Serial peripheral data length control for each timer
  - Timeout support for each timer
  - Timer underflow interrupt/event
  - Compare match or input capture interrupt/event for each timer
- One 16-bit timer/counter by cascading two 8-bit timer/counters with:
  - Period and compare channel
  - Input capture
  - Timeout support
  - Timer underflow interrupt/event
  - Compare match or input capture interrupt/event
- Programmable lookup table supporting multiple configurations:
  - Two 2-input units
  - One 3-input unit
  - RS configuration
  - Duplicate input with selectable delay on one input or output
  - Connection to external I/O pins, event system or one selectable USART
- Combinatorial Logic Functions using programmable truth table:
  - AND, NAND, OR, NOR, XOR, XNOR, NOT, MUX
- Sequential Logic Functions:
  - D-Flip-Flop, D Latch, RS Latch
- Input sources:
  - From external pins or the event system
  - One input source includes selectable delay or synchronizing option
  - Can be shared with selectable USART pin locations
- Outputs:
  - Available on external pins or event system
  - Includes selectable delay or synchronizing option
  - Can override selectable USART pin locations
- Operates in active mode and all sleep modes

26.2 Overview

The XMEGA Custom Logic module (XCL) consists of two sub-units, each including 8-bit timer/counter with flexible settings, peripheral counter working with one software selectable USART module, delay elements, glue logic with programmable truth table and a global logic interconnect array.

The timer/counter configuration allows for two 8-bits timer/counters. Each timer/counter supports normal, compare and input capture operation, with common flexible clock selections and event channels for each timer. By cascading the two 8-bit timer/counters, the XCL can be used as a 16-bit timer/counter.

The peripheral counter (PEC) configuration, the XCL is connected to one software selectable USART. This USART controls the counter operation, and the PEC can optionally control the data length within the USART frame.

The glue logic configuration, the XCL implements two programmable lookup tables (LUTs). Each defines the truth table corresponding to the logical condition between two inputs. Any combinatorial function logic is possible. The LUT inputs can be connected to I/O pins or event system channels. If the LUT is connected to the USART0 pin locations, the data lines (TXD/RXD) data encoding/decoding will be possible. Connecting together the LUT units, RS Latch, or any combinatorial logic between two operands or three inputs can be enabled.

30. AC – Analog Comparator

30.1 Features

- Two Analog Comparators
- Selectable propagation delay
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog Comparator output available on pin
- Flexible Input Selection
  - All pins on the port
  - Output from the DAC
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal AVCC voltage
- Interrupt and event generation on
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection
- Source of asynchronous event

30.2 Overview

The Analog Comparator (AC) compares the voltage level on two inputs and gives a digital output based on this comparison. The Analog Comparator may be configured to give interrupt requests and/or synchronous/asynchronous events upon several different combinations of input change.

One important property of the Analog Comparator when it comes to the dynamic behavior, is the hysteresis. This parameter may be adjusted in order to find the optimal operation for each application.

The input section includes analog port pins, several internal signals and a 64-level programmable voltage scaler. The analog comparator output state can also be directly available on a pin for use by external devices. Using as pair they can also be set in Window mode to monitor a signal compared to a voltage window instead of a voltage level.

A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

PORTA has one AC pair. Notation is ACA.

32. Pinout and Pin Functions

The device pinout is shown in “Pinout and Block Diagram” on page 4. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

32.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

32.1.1 Operation/Power Supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
GND	Ground

32.1.2 Port Interrupt Functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

32.1.3 Analog Functions

ACn	Analog Comparator input pin n
ACnOUT	Analog Comparator n Output
ADCn	Analog to Digital Converter input pin n
DACn	Digital to Analog Converter output pin n
A_{REF}	Analog Reference input pin

32.1.4 Timer/Counter and WEX Functions

OCnx	Output Compare Channel x for timer/counter n
OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

32.1.5 Communication Functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
SCLIN	Serial Clock In for TWI when external driver interface is enabled
SCLOUT	Serial Clock Out for TWI when external driver interface is enabled
SDAIN	Serial Data In for TWI when external driver interface is enabled
SDAOUT	Serial Data Out for TWI when external driver interface is enabled

Base Address	Name	Description
0x07E0	PORTR	Port R
0x0800	TCC4	Timer/Counter 4 on port C
0x0840	TCC5	Timer/Counter 5 on port C
0x0880	FAULTC4	Fault Extension on TCC4
0x0890	FAULTC5	Fault Extensionon TCC5
0x08A0	WEXC	Waveform Extension on port C
0x08B0	HIRESC	High Resolution Extension on port C
0x08C0	USARTC0	USART 0 on port C
0x08E0	SPIC	Serial Peripheral Interface on port C
0x08F8	IRCOM	Infrared Communication Module
0x0940	TCD5	Timer/Counter 5 on port D
0x09C0	USARTD0	USART 0 on port D

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two's Complement Overflow	V ← 1	V	1
CLV		Clear Two's Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU control instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

Notes: 1. Cycle times for data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.
2. One extra cycle must be added when accessing internal SRAM.

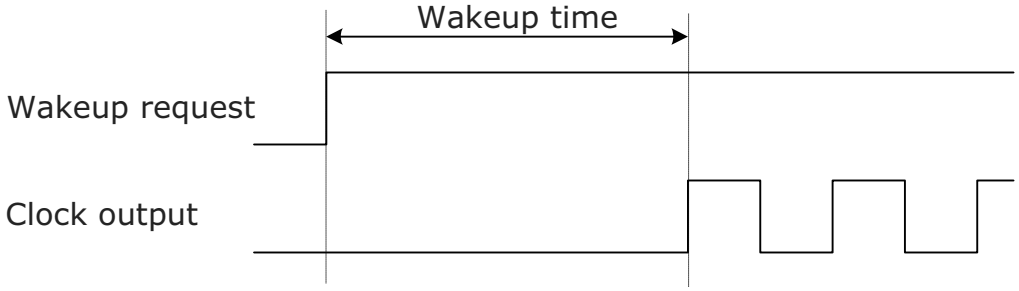
36.4 Wake-up Time from Sleep Modes

Table 36-5. Device Wake-up Time from Sleep Modes with Various System Clock Sources

Symbol	Parameter	Condition		Min.	Typ.(1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock			0.2		µs
		32kHz internal oscillator			120		
		8MHz internal oscillator			0.5		
		32MHz internal oscillator			0.2		
	Wake-up time from power save mode	External 2MHz clock			4.5		
		32kHz internal oscillator			320		
		8MHz internal oscillator	Normal mode		4.5		
			Low power mode		0.5		
		32MHz internal oscillator			5.0		
	Wake-up time from power down mode	External 2MHz clock			4.5		
		32kHz internal oscillator			320		
		8MHz internal oscillator			4.5		
		32MHz internal oscillator			5.0		

Notes: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 36-2. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 36-2. Wake-up Time Definition



36.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low-level input and output voltage limits reflect or exceed this specification.

Table 36-6. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage, except XTAL1 and RESET pin	V_{CC} = 2.4 - 3.6V		0.7*V_{CC}		V_{CC}+0.5	V
		V_{CC} = 1.6 - 2.4V		0.8*V_{CC}		V_{CC}+0.5	
V_{IL}	Low level input voltage, except XTAL1 and RESET pin	V_{CC} = 2.4 - 3.6V		-0.5		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2*V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	3.1		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.7		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.7		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.20	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.15	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.10	0.46	
I_{IN}	Input leakage current	T = 25°C			<0.01	1.0	µA
R_P	Pull/buss keeper resistor				27		kΩ

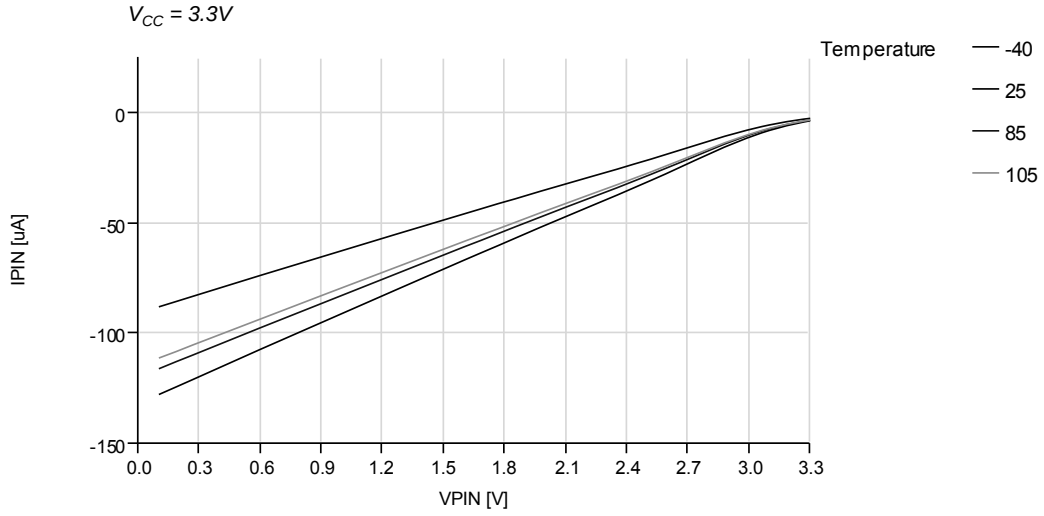
Notes:
1. The sum of all I_{OH} for PA[7:5] on PORTA must not exceed 100mA.
   The sum of all I_{OH} for PA[4:0] on PORTA must not exceed 200mA.
   The sum of all I_{OH} for PORTD and PORTR must not exceed 100mA.
   The sum of all I_{OH} for PORTC and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PA[7:5] on PORTA must not exceed 100mA.
   The sum of all I_{OL} for PA[4:0] on PORTA must not exceed 100mA.
   The sum of all I_{OL} for PORTD and PORTR must not exceed 100mA.
   The sum of all I_{OL} for PORTC PDI must not exceed 100mA.

36.6 ADC Characteristics

Table 36-7. Power Supply, Reference, and Input Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1		AV_{CC}- 0.6	
R_{in}	Input resistance	Switched			4.5	kΩ
C_{in}	Input capacitance	Switched			5	pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF

Figure 37-25.I/O Pin Pull-up Resistor Current vs. Input Voltage



37.2.2 Output Voltage vs. Sink/Source Current

Figure 37-26.I/O Pin Output Voltage vs. Source Current

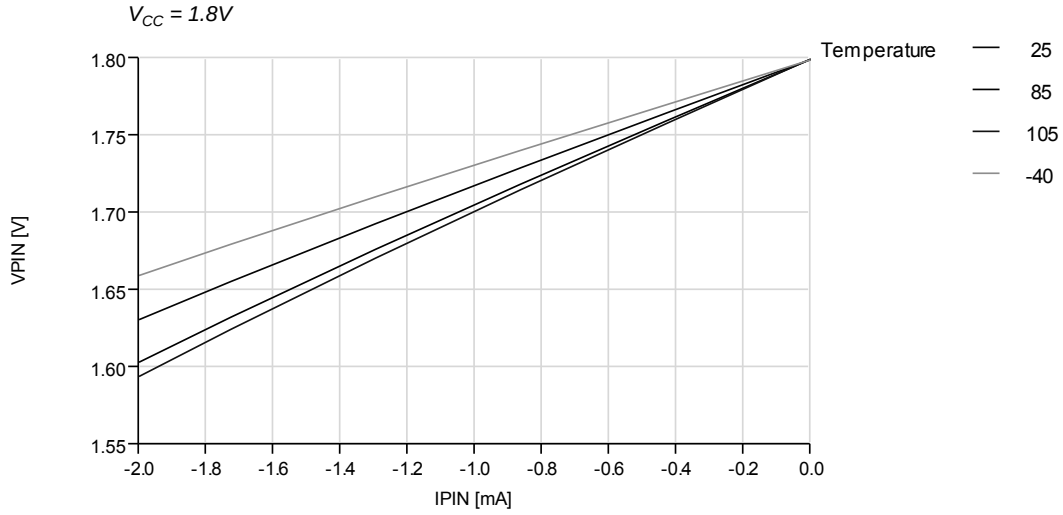


Figure 37-29.I/O Pin Output Voltage vs. Source Current

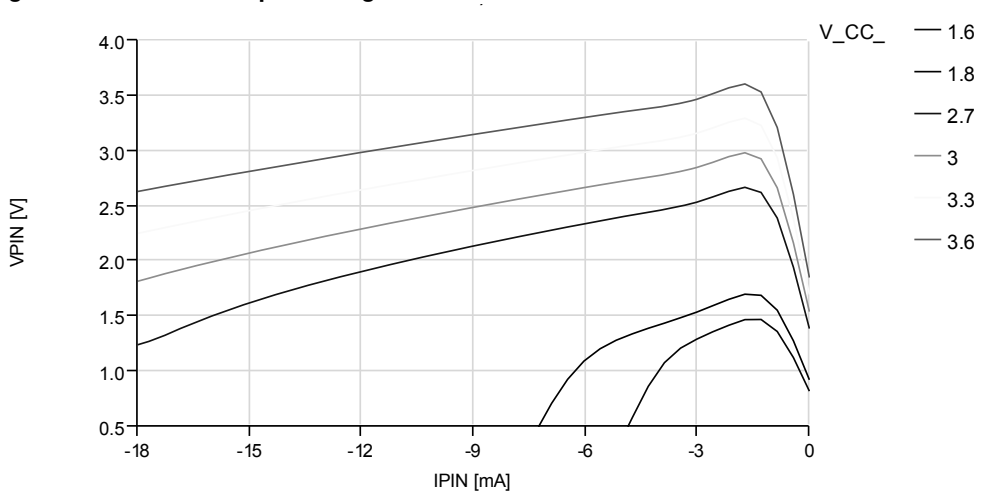


Figure 37-30.I/O Pin Output Voltage vs. Sink Current

V_{CC} = *1.8V*

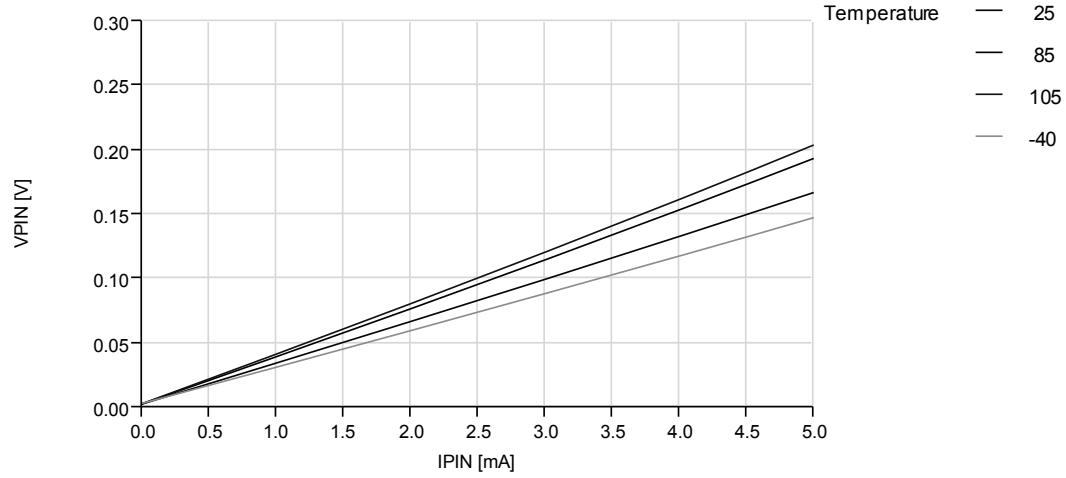


Figure 37-35.I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IH} I/O pin read as "1"

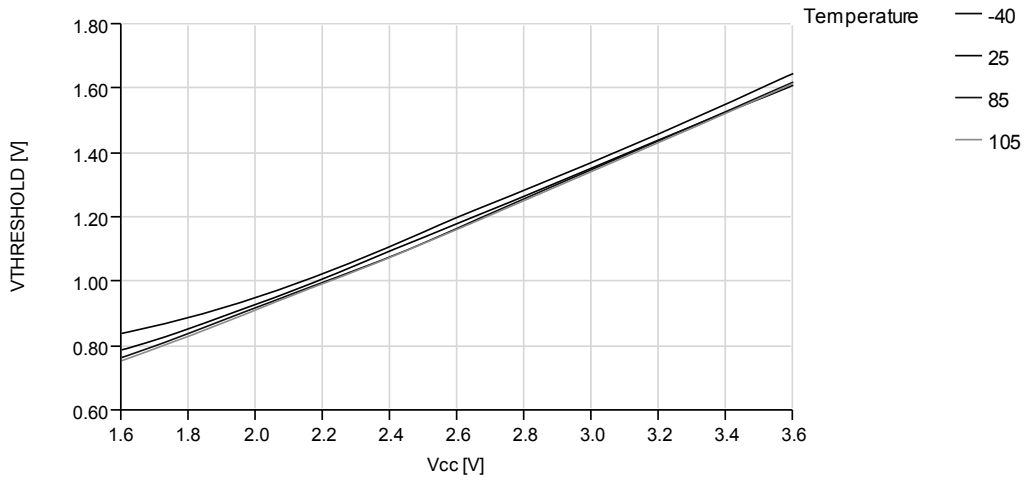
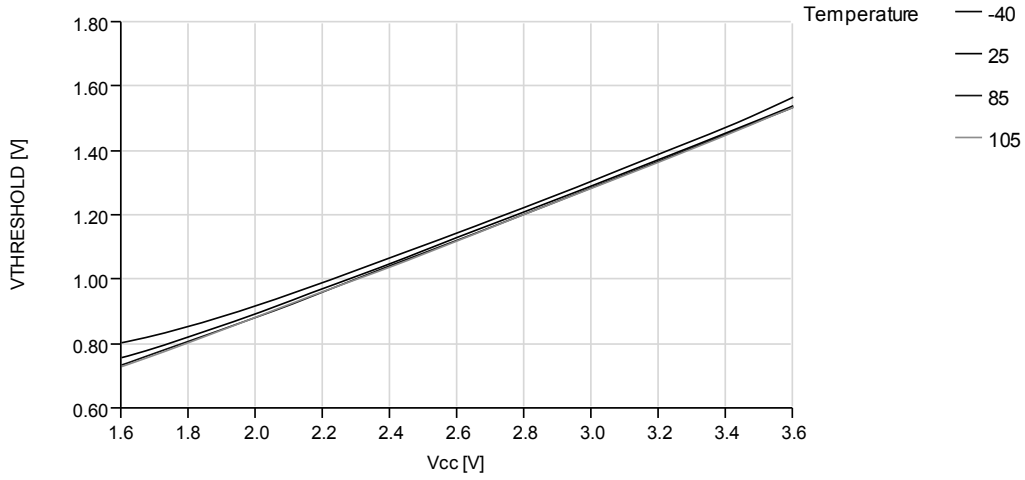


Figure 37-36.I/O Pin Input Threshold Voltage vs. V_{CC}

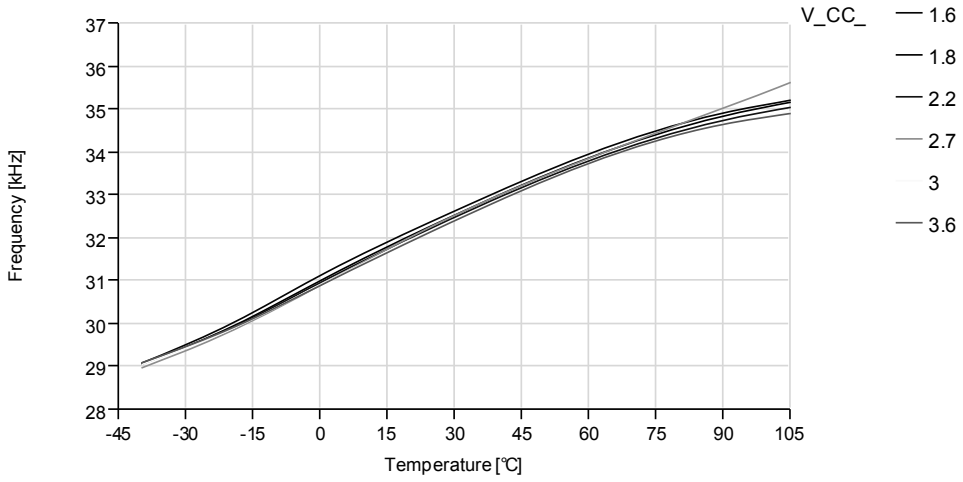
V_{IL} I/O pin read as "0"



37.10 Oscillator Characteristics

37.10.1 Ultra Low-Power Internal Oscillator

Figure 37-70. Ultra Low-Power Internal Oscillator Frequency vs. Temperature



37.10.2 32.768KHz Internal Oscillator

Figure 37-71. 32.768kHz Internal Oscillator Frequency vs. Temperature

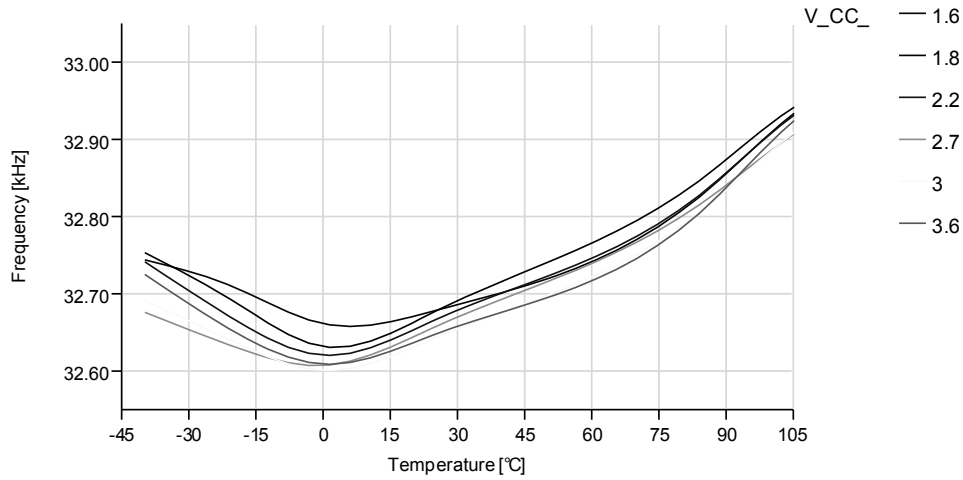


Figure 37-76. 8MHz Internal Oscillator CAL Calibration Step Size

V_{CC} = 3.0V

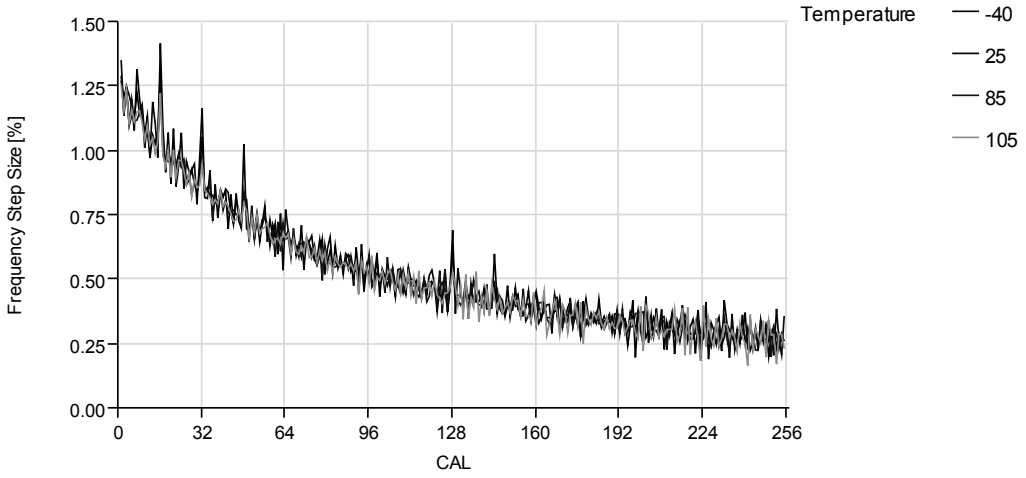
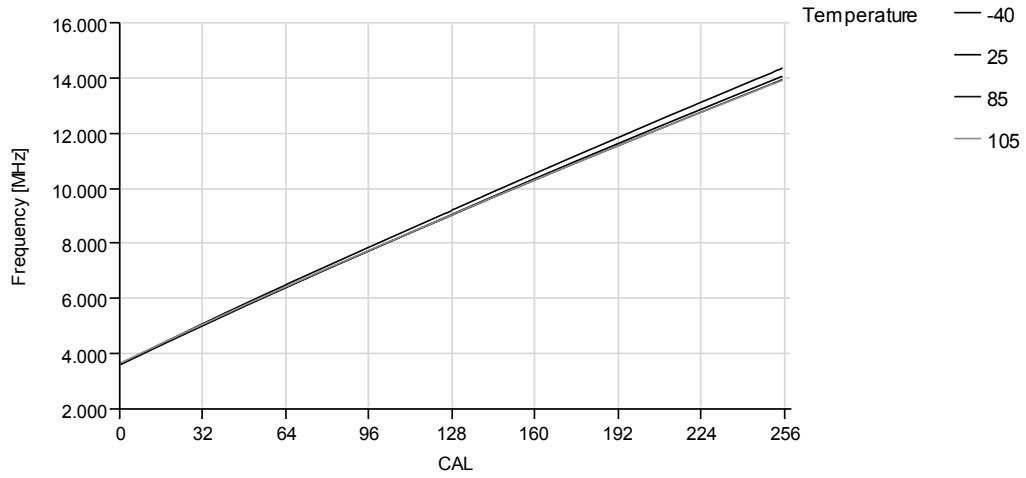


Figure 37-77. 8MHz Internal Oscillator Frequency vs. Calibration

V_{CC} = 3.0V, normal mode



Issue: AC: Flag can not be cleared if the module is not enabled

It is not possible to clear the AC interrupt flags without enabling either of the analog comparators.

Workaround:

Clear the interrupt flags before disabling the module.

Issue: USART: Receiver not functional when variable data length and start frame detector are enabled

When using USART in variable frame length with XCL PEC01 configuration and start frame detection activated, the USART receiver is not functional.

Workaround:

Use XCL BTC0PCE2 configuration instead of PEC01.

Issue: T/C: Counter does not start when CLKSEL is written

When STOP bit is cleared (CTRLGCLR.STOP) before the timer/counter is enabled (CTRLA.CLKSEL != OFF), the T/C doesn't start operation.

Workaround:

Do not write CTRLGCLR.STOP bit before writing CTRLA.CLKSEL bits.

Issue: EEPROM write and Flash write operations fails under 2.0V

EEPROM write and Flash write operations are limited from 2.0V to 3.6V. Other functionalities operates from 1.6V to 3.6V.

Workaround:

None.

Issue: TWI master or slave remembering data

If a write is made to Data register, prior to Address register, the TWI design sends the data as soon as the write to Address register is made. But the send data will be always 0x00.

Workaround:

None.

Issue: Temperature sensor not calibrated

Temperature sensor factory calibration is not implemented.

Workaround:

None.