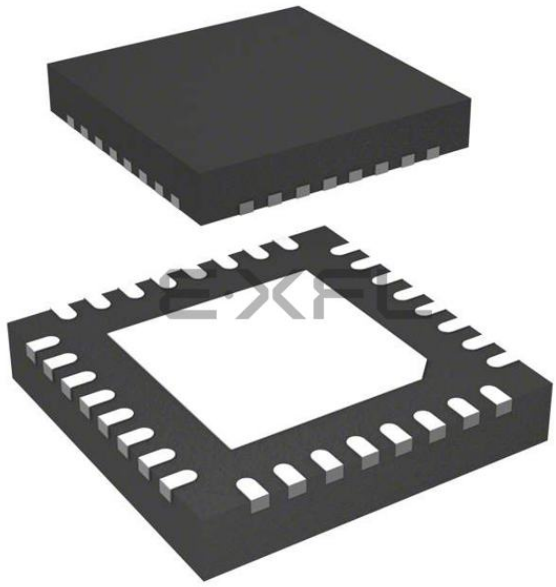

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16e5-m4nr

8.10 Device ID and Revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

8.11 I/O Memory Protection

Some features in the device are regarded as critical for safety in some applications. Due to this, it is possible to lock the I/O register related to the clock system, the event system, and the waveform extensions. As long as the lock is enabled, all related I/O registers are locked and they cannot be written from the application software. The lock registers themselves are protected by the configuration change protection mechanism.

8.12 Flash and EEPROM Page Size

The flash program memory and EEPROM data memory are organized in pages. The pages are word accessible for the flash and byte accessible for the EEPROM.

Table 8-2 shows the Flash Program Memory organization and Program Counter (PC) size. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) give the page number and the least significant address bits (FWORD) give the word in the page.

Table 8-2. Number of Words and Pages in the Flash

Devices	PC size	Flash size	Page Size	FWORD	FPAGE	Application		Boot	
	bits	bytes	words			Size	No. of pages	Size	No. of pages
ATxmega32E5	15	32K+4K	64	Z[6:0]	Z[14:7]	32K	256	4K	32
ATxmega16E5	14	16K+4K	64	Z[6:0]	Z[13:7]	16K	128	4K	32
ATxmega8E5	13	8K+2K	64	Z[6:0]	Z[12:7]	8K	64	2K	16

Table 8-3 shows EEPROM memory organization for the Atmel AVR XMEGA E5 devices. EEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM address register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

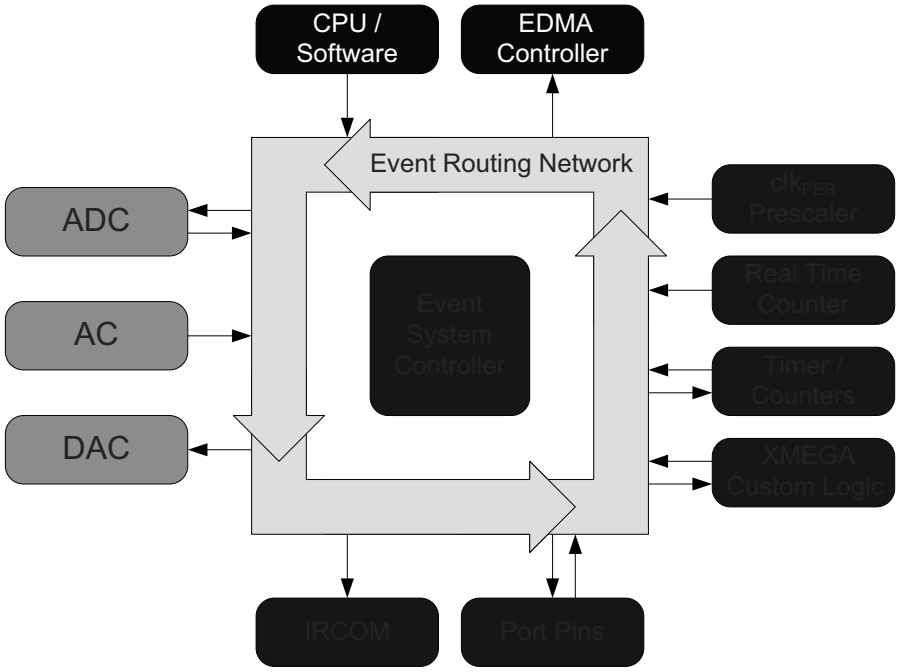
Table 8-3. Number of Words and Pages in the EEPROM

Devices	EEPROM	Page Size	E2BYTE	E2PAGE	No. of Pages
	Size	bytes			
ATxmega32E5	1K	32	ADDR[4:0]	ADDR[10:5]	32
ATxmega16E5	512Bytes	32	ADDR[4:0]	ADDR[10:5]	16
ATxmega8E5	512Bytes	32	ADDR[4:0]	ADDR[10:5]	16

The EDMA controller supports extended features such as double buffering, data match for peripherals and data search for SRAM or EEPROM.

The EDMA controller supports two types of channel. Each channel type can be selected individually.

Figure 10-1. Event System Overview and Connected Peripherals



The event routing network consists of eight software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow up to eight parallel event configurations and routing. The maximum routing latency of an external event is two peripheral clock cycles due to re-synchronization, but several peripherals can directly use the asynchronous event without any clock delay. The event system works in all power sleep modes, but only asynchronous events can be routed in sleep modes where the system clock is not available.

15. Interrupts and Programmable Multilevel Interrupt Controller

15.1 Features

- Short and predictable interrupt response time
- Separate interrupt configuration and vector address for each interrupt
- Programmable multilevel interrupt controller
  - Interrupt prioritizing according to level and vector address
  - Three selectable interrupt levels for all interrupts: low, medium, and high
  - Selectable, round-robin priority scheme within low-level interrupts
  - Non-maskable interrupts for critical functions
- Interrupt vectors optionally placed in the application section or the boot loader section

15.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

15.3 Interrupt Vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA E5 devices are shown in Table 15-1. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA AU manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 15-1. The program address is the word address.

Table 15-1. Peripheral Module Address Map

Program address (base address)	Source	Interrupt description
0x0000	RESET	
0x0002	OSCF_INT_vect	Crystal oscillator failure and PLL lock failure interrupt vector (NMI)
0x0004	PORTR_INT_vect	Port R Interrupt vector
0x0006	EDMA_INT_base	EDMA Controller Interrupt base
0x000E	RTC_INT_base	Real time counter interrupt base
0x0012	PORTC_INT_vect	Port C interrupt vector
0x0014	TWIC_INT_base	Two-wire interface on Port C interrupt base
0x0018	TCC4_INT_base	Timer/counter 4 on port C interrupt base

19. Hi-Res – High Resolution Extension

19.1 Features

- Increases waveform generator resolution up to 8x (three bits)
- Supports frequency, single-slope PWM, and dual-slope PWM generation
- Supports the WeX when this is used for the same timer/counter

19.2 Overview

The high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the WeX if this is used for the same timer/counter.

The hi-res extension uses the peripheral 4x clock (ClkPER4). The system clock prescalers must be configured so the peripheral 4x clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

There is one hi-res extension that can be enabled for timer/counters pair on PORTC. The notation of this is HIRESC.

The clock generator includes a fractional baud rate generator that is able to generate a wide range of USART baud rates from any system clock frequencies. This removes the need to use an external crystal oscillator with a specific frequency to achieve a required baud rate. It also supports external clock input in synchronous slave operation.

An IRCOM module can be enabled for one USART to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2Kbps.

One USART can be connected to the XMEGA Custom Logic module (XCL). When used with the XCL, the data length within an USART/SPI frame can be controlled by the peripheral counter (PEC) within the XCL. This enables configurable frame length up to 256 bits. In addition, the TxD/RxD data can be encoded/decoded before the signal is fed into the USART receiver, or after the signal is output from transmitter when the USART is connected to XCL LUT outputs.

When the USART is set in master SPI mode, all USART-specific logic is disabled, leaving the transmit and receive buffers, shift registers, and baud rate generator enabled. The registers are used in both modes, but their functionality differs for some control settings. Pin control and interrupt generation are identical in both modes.

PORTC and PORTD each has one USART. Notation of these peripherals are USARTC0 and USARTD0, respectively.

30. AC – Analog Comparator

30.1 Features

- Two Analog Comparators
- Selectable propagation delay
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog Comparator output available on pin
- Flexible Input Selection
  - All pins on the port
  - Output from the DAC
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal AVCC voltage
- Interrupt and event generation on
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection
- Source of asynchronous event

30.2 Overview

The Analog Comparator (AC) compares the voltage level on two inputs and gives a digital output based on this comparison. The Analog Comparator may be configured to give interrupt requests and/or synchronous/asynchronous events upon several different combinations of input change.

One important property of the Analog Comparator when it comes to the dynamic behavior, is the hysteresis. This parameter may be adjusted in order to find the optimal operation for each application.

The input section includes analog port pins, several internal signals and a 64-level programmable voltage scaler. The analog comparator output state can also be directly available on a pin for use by external devices. Using as pair they can also be set in Window mode to monitor a signal compared to a voltage window instead of a voltage level.

A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

PORTA has one AC pair. Notation is ACA.

31. Programming and Debugging

31.1 Features

- Programming
  - External programming through PDI interface
    - Minimal protocol overhead for fast operation
    - Built-in error detection and handling for reliable operation
  - Boot loader support for programming through any communication interface
- Debugging
  - Nonintrusive, real-time, on-chip debug system
  - No software or hardware resources required from device except pin connection
  - Program flow control
  - Go, Stop, Reset, Step Into, Step Over, Step Out, Run-to-Cursor
  - Unlimited number of user program breakpoints
  - Unlimited number of user data breakpoints, break on:
    - Data location read, write, or both read and write
    - Data location content equal or not equal to a value
    - Data location content is greater or smaller than a value
    - Data location content is within or outside a range
  - No limitation on device clock frequency
- Program and Debug Interface (PDI)
  - Two-pin interface for external programming and debugging
  - Uses the Reset pin and a dedicated pin
  - No I/O pins required during programming or debugging

31.2 Overview

The Program and Debug Interface (PDI) is an Atmel proprietary interface for external programming and on-chip debugging of a device. The PDI supports fast programming of nonvolatile memory (NVM) spaces; flash, EEPOM, fuses, lock bits, and the user signature row.

Debug is supported through an on-chip debug system that offers nonintrusive, real-time debug. It does not require any software or hardware resources except for the device pin connection. Using the Atmel tool chain, it offers complete program flow control and support for an unlimited number of program and complex data breakpoints. Application debug can be done from a C or other high-level language source code level, as well as from an assembler and disassemble level.

Programming and debugging can be done through the PDI physical layer. This is a two-pin interface that uses the Reset pin for the clock input (PDI_CLK) and one other dedicated pin for data input and output (PDI_DATA). Any external programmer or on-chip debugger/emulator can be directly connected to this interface.

32.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.

Table 32-1. PORT A – Alternate Functions

PORT A	Pin#	ADCA POS/ GAINPOS	ADCA NEG/ GAINNEG	DACA	ACA POS	ACA NEG	ACA OUT	REFA
PA0	6	ADC 0	ADC 0		AC0	AC0		AREF
PA1	5	ADC 1	ADC 1		AC1	AC1		
PA2	4	ADC 2	ADC 2	DAC0	AC2			
PA3	3	ADC 3	ADC 3	DAC1	AC3	AC3		
PA4	2	ADC 4	ADC 4		AC4			
PA5	31	ADC 5	ADC 5		AC5	AC5		
PA6	30	ADC 6	ADC 6		AC6		AC1OUT	
PA7	29	ADC 7	ADC 7			AC7	AC0OUT	

Table 32-2. PORT C – Alternate Functions

PORT C	Pin #	TCC4	WEXC	TCC5	USARTC0	SPIC	TWI	XCL (LUT)	EXTCLK	AC OUT
PC0	16	OC4A	OC4ALS				SDA	IN1/OUT0		
PC1	15	OC4B	OC4AHS		XCK0		SCL	IN2		
PC2	14	OC4C	OC4BLS		RXD0			IN0		
PC3	13	OC4D	OC4BHS		TXD0			IN3		
PC4	12	OC4A	OC4CLS	OC5A		$\overline{SS}$		IN1/OUT0	EXTCLK	
PC5	11	OC4B	OC4CHS	OC5B	XCK0	SCK		IN2		
PC6	10	OC4C	OC4DLS		RXD0	MISO		IN0		AC1OUT
PC7	9	OC4D	OC4DHS		TXD0	MOSI		IN3		AC0OUT

Table 32-3. Debug – Program and Debug Functions

DEBUG	Pin #	PROG
RESET	8	PDI CLOCK
PDI	7	PDI DATA

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two's Complement Overflow	V ← 1	V	1
CLV		Clear Two's Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU control instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

Notes: 1. Cycle times for data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.
2. One extra cycle must be added when accessing internal SRAM.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Gain error	0.5x gain		-1		%
		1x gain		-1		
		8x gain		-1		
		64x gain		-1.5		
	Offset error, input referred	0.5x gain		10		mV
		1x gain		5		
		8x gain		5		
		64x gain		5		

36.7 DAC Characteristics

Table 36-11. Power Supply, Reference, and Output Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	
AV_{REF}	External reference voltage		1.0		V_{CC}- 0.6	V
$R_{channel}$	DC output impedance				50	Ω
	Linear output voltage range		0.15		V_{REF}-0.15	V
R_{AREF}	Reference input resistance			>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
	Minimum Resistance load		1			kΩ
	Maximum capacitance load				100	pF
		1000Ω serial resistance			1	nF
	Output sink/source	Operating within accuracy specification			AV_{CC}/1000	mA
		Safe operation			10	

Table 36-12. Clock and Timing

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
f_{DAC}	Conversion rate	C_{load}=100pF, maximum step size	Normal mode	0		1000	ksps
			Low power mode	0		500	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	64-Level Voltage Scaler Integral non-linearity (INL)			0.3	0.5	lsb
	Current source accuracy after calibration			5		%
	Current source calibration range	Single mode	4		6	µA
	Current source calibration range	Double mode	8		12	

36.9 Bandgap and Internal 1.0V Reference Characteristics

Table 36-15. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC	1 Clk_{PER} + 2.5µs			µs
		As input voltage to ADC and AC		1.5		
BANDGAP	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference for ADC and DAC	T= 25°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Calibrated at T= 25°C		±3		%

36.9.1 Brownout Detection Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.50	1.65	1.75	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
T_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1.0		ms
V_{HYST}	Hysteresis	BOD level 0 - 7. Min value measured at BOD level 0		1.0		%

Table 36-29. SPI Timing Characteristics and Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master				ns
t_{SCKW}	SCK high/low width	Master		0.5×SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5×SCK		
t_{MOH}	MOSI hold after SCK	Master		1.0		
t_{SSCK}	Slave SCK Period	Slave	4×t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2×t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3.0			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8.0		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8.0		

Figure 37-11.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

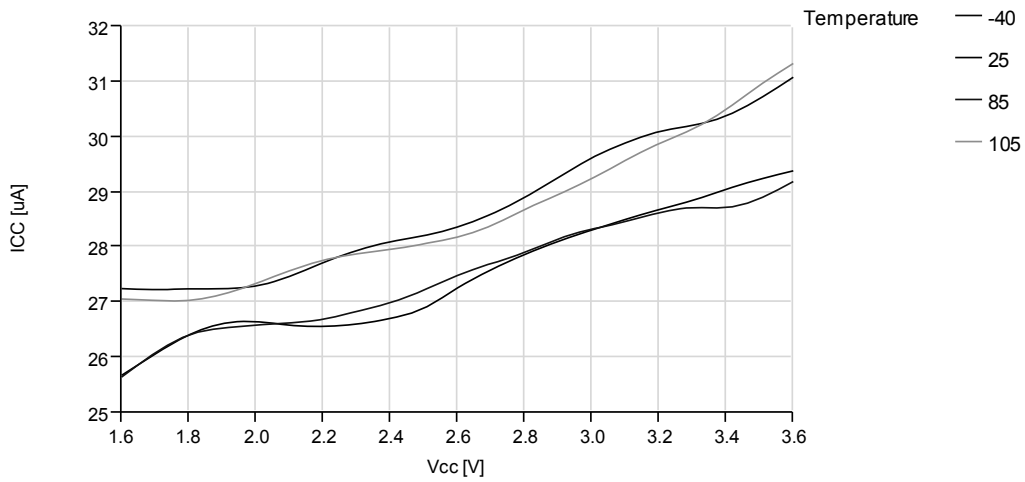


Figure 37-12.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

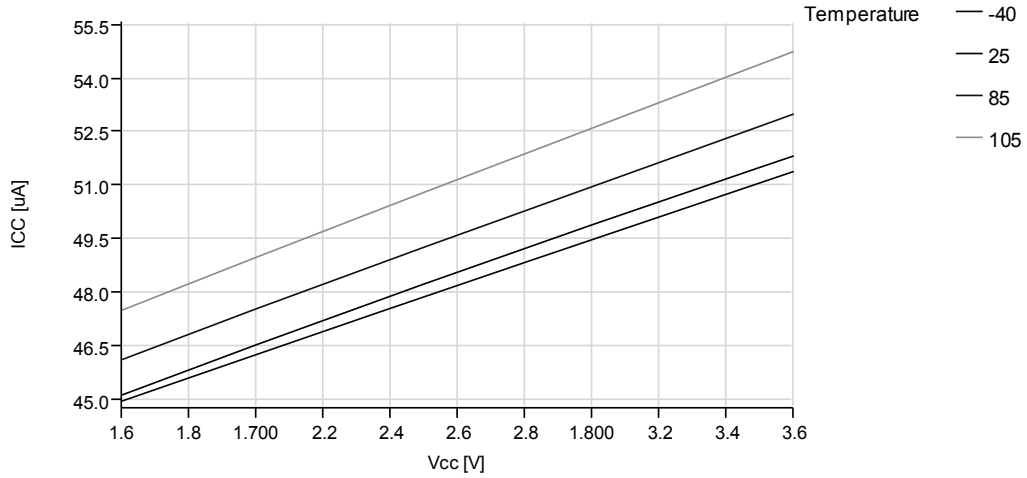


Figure 37-41. ADC Gain Error vs. V_{CC}

T = 25°C, V_{REF} = 1.0V, ADC sample rate = 300ksps

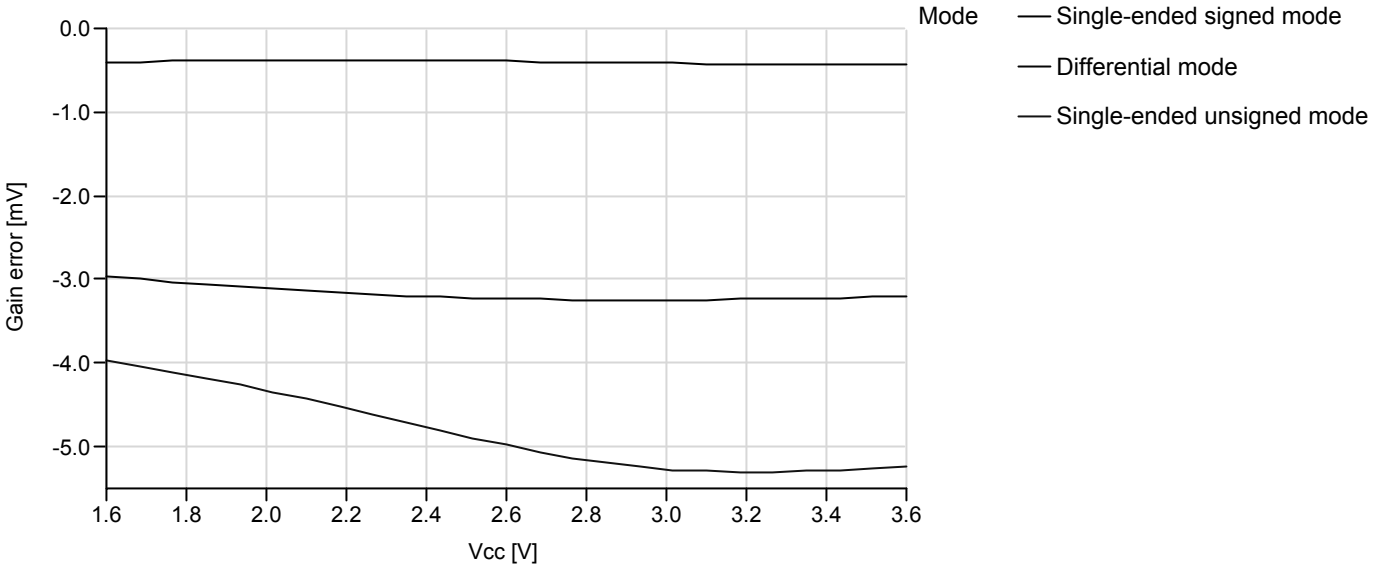
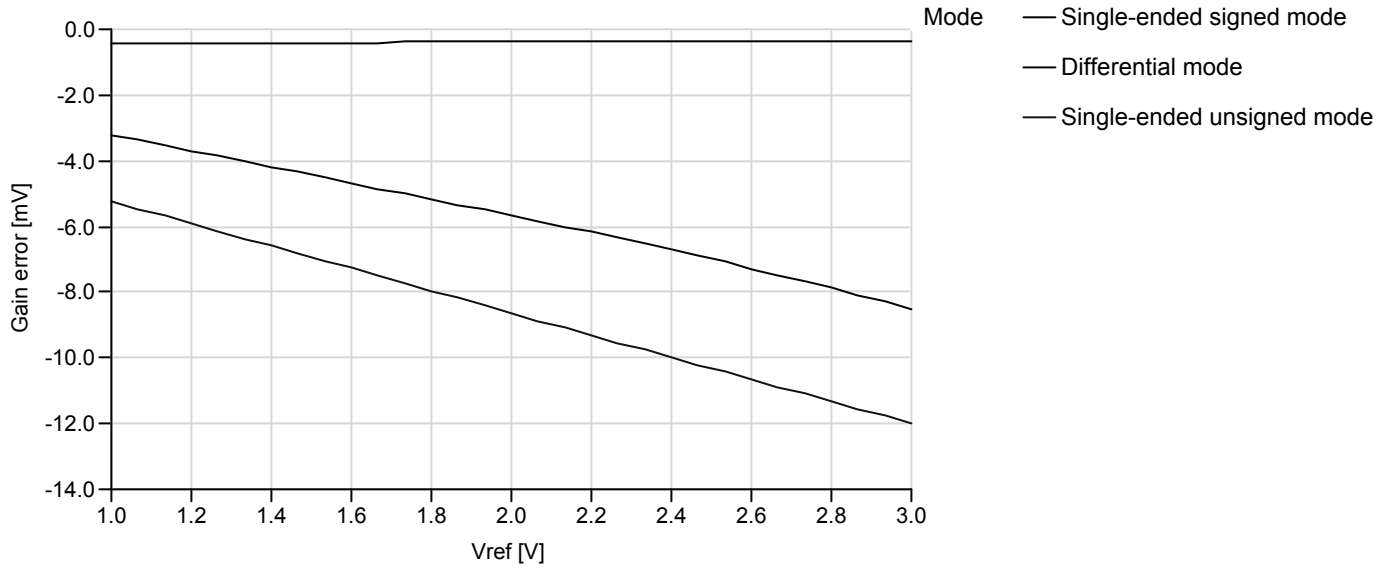


Figure 37-42. ADC Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps



37.4 DAC Characteristics

Figure 37-47.DAC INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V

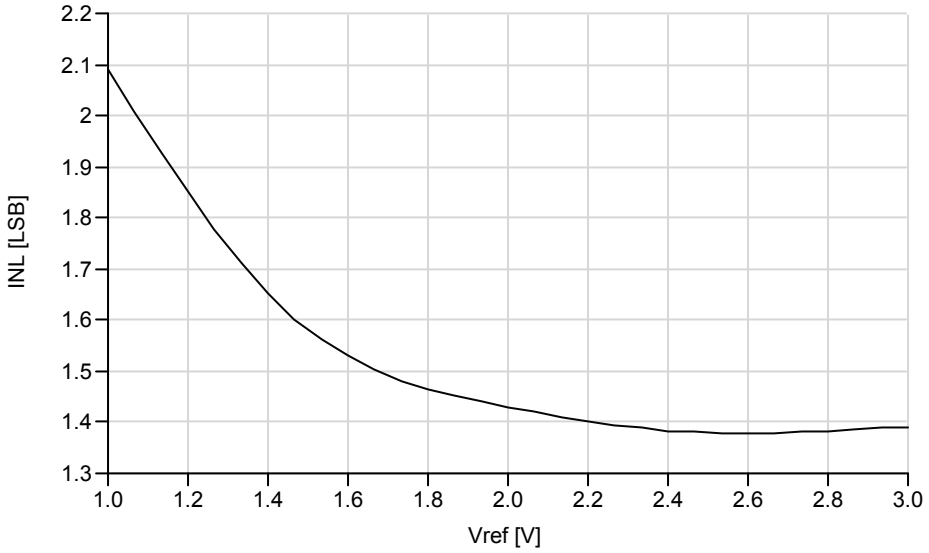
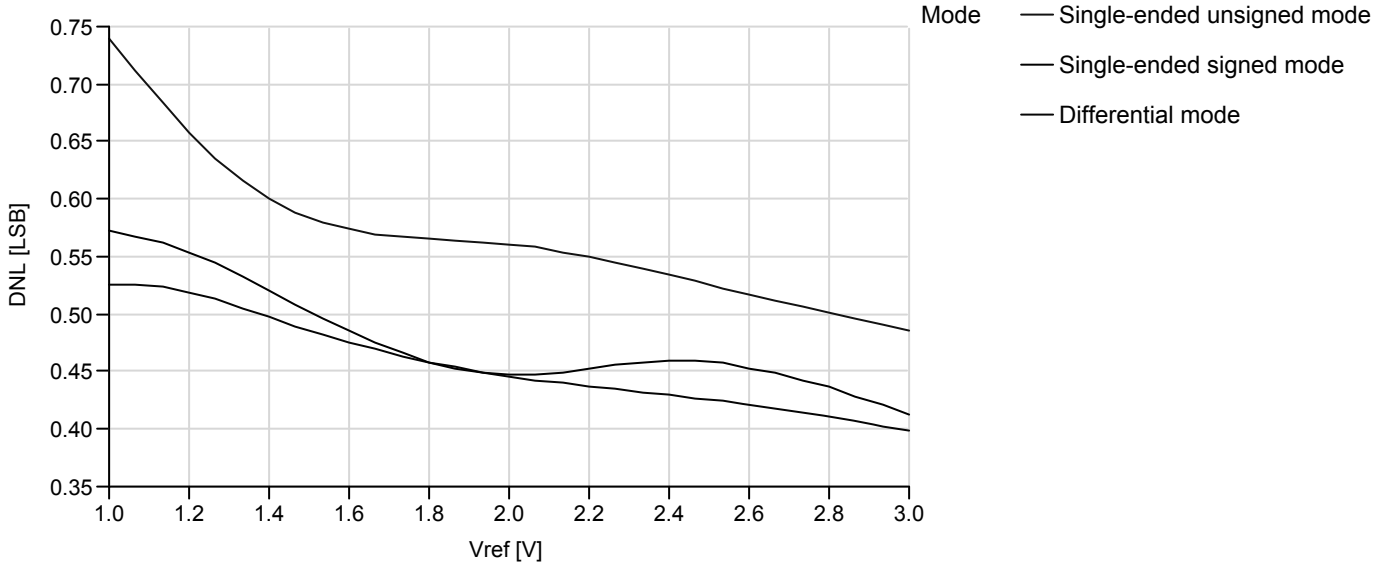


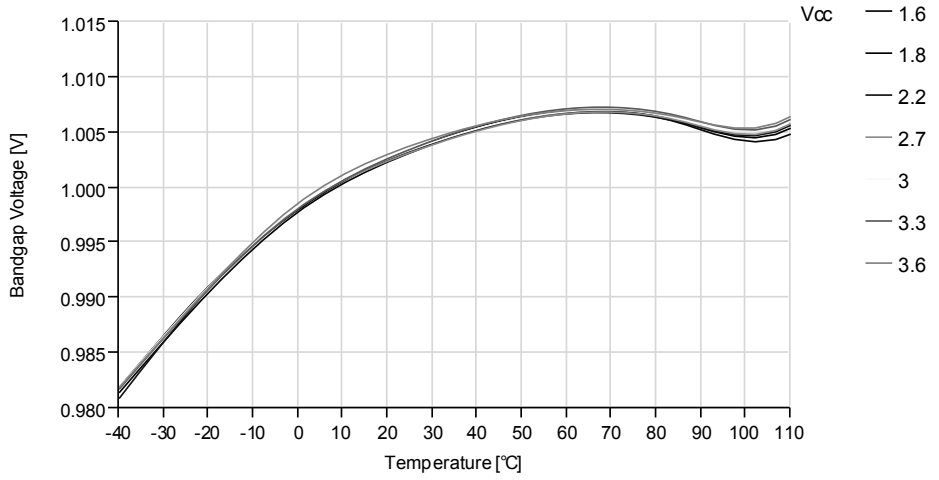
Figure 37-48.DNL Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V



37.6 Internal 1.0V Reference Characteristics

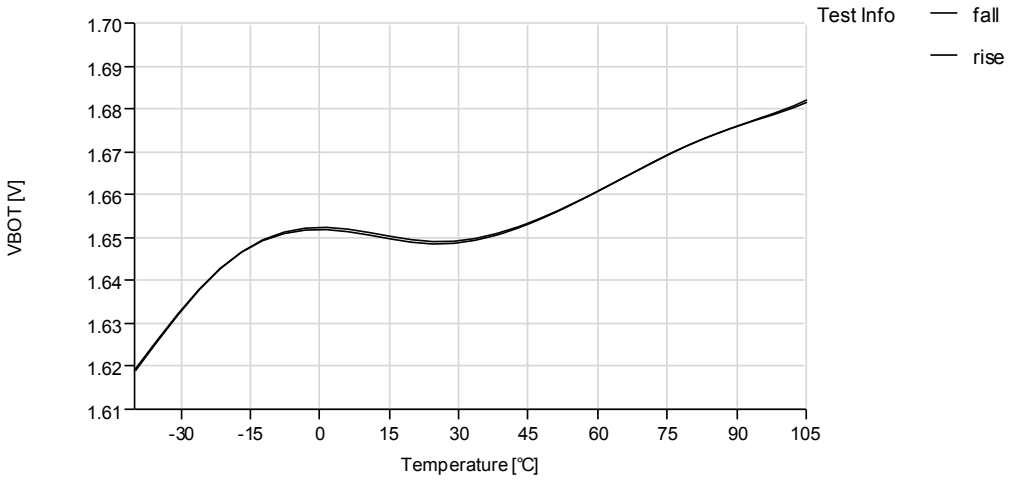
Figure 37-59.ADC/DAC Internal 1.0V Reference vs. Temperature



37.7 BOD Characteristics

Figure 37-60.BOD Thresholds vs. Temperature

BOD level = 1.6V



37.10.3 8MHz Internal Oscillator

Figure 37-74. 8MHz Internal Oscillator Frequency vs. Temperature

Normal mode

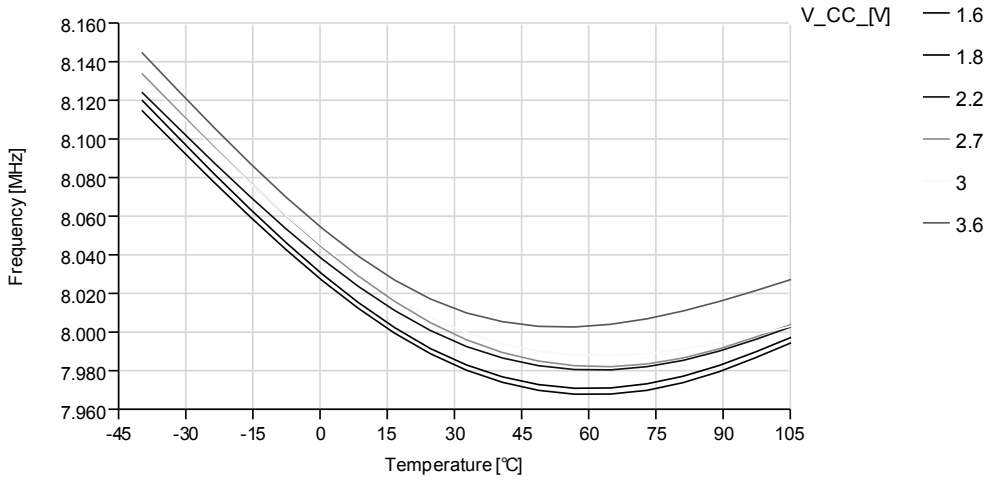


Figure 37-75. 8MHz Internal Oscillator Frequency vs. Temperature

Low power mode

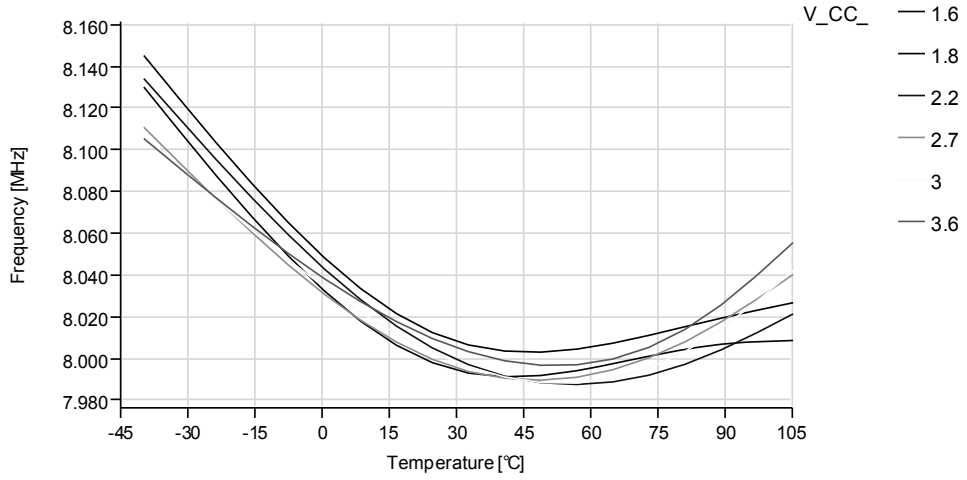
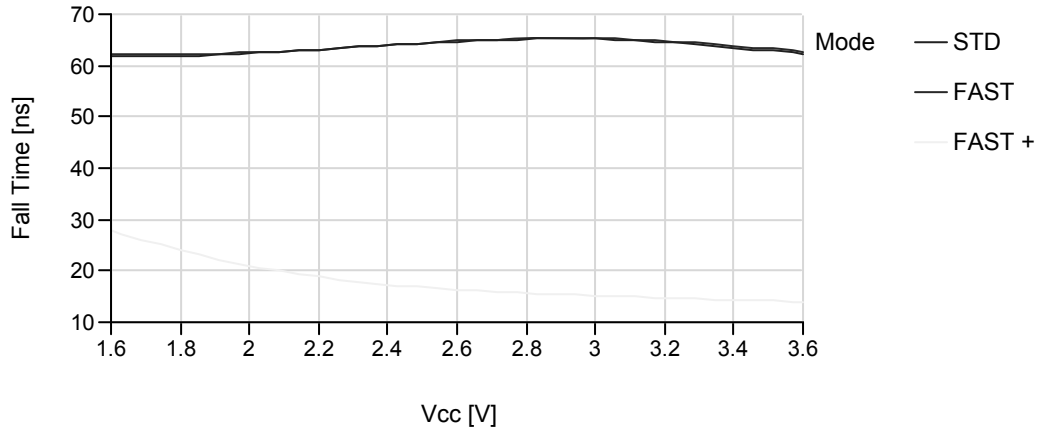
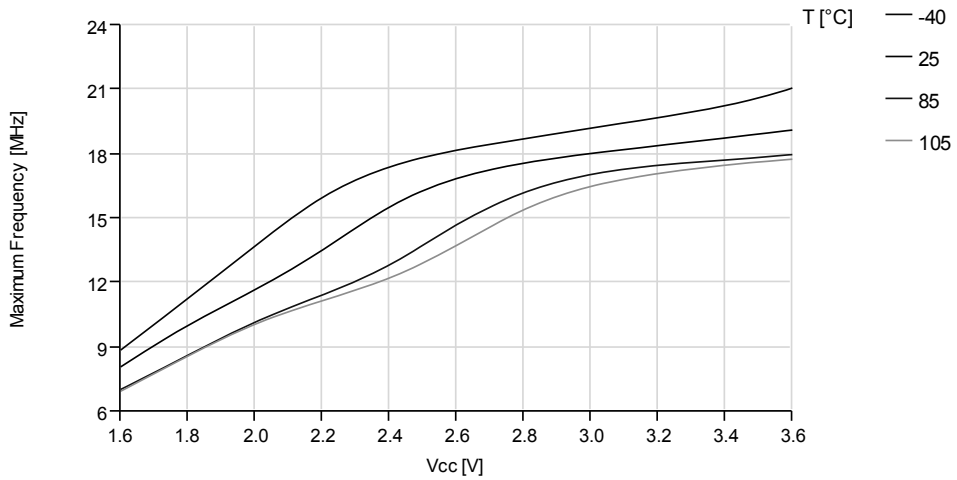


Figure 37-84. SDA Fall Time vs. V_{CC}



37.12 PDI Characteristics

Figure 37-85. Maximum PDI Frequency vs. V_{CC}



38.2 Rev. A

- DAC: AREF on PD0 is not available for the DAC
- EDMA: Channel transfer never stops when double buffering is enabled on sub-sequent channels
- ADC: Offset correction fails in unsigned mode
- ADC: Averaging is failing when channel scan is enabled
- ADC: Averaging in single conversion requires multiple conversion triggers
- ADC accumulator sign extends the result in unsigned mode averaging
- ADC: Free running average mode issue
- ADC: Event triggered conversion in averaging mode
- AC: Flag can not be cleared if the module is not enabled
- USART: Receiver not functional when variable data length and start frame detector are enabled
- T/C: Counter does not start when CLKSEL is written
- EEPROM write and Flash write operations fails under 2.0V
- TWI master or slave remembering data
- Temperature Sensor not calibrated

Issue: DAC: AREF on PD0 is not available for the DAC

The AREF external reference input on pin PD0 is not available for the DAC.

Workaround:

No workaround. Only AREF on pin PA0 can be used as external reference input for the DAC.

Issue: EDMA: Channel transfer never stops when double buffering is enabled on sub-sequent channels

When the double buffering is enabled on two channels, the channels which are not set in double buffering mode are never disabled at the end of the transfer. A new transfer can start if the channel is not disabled by software.

Workaround:

- CHMODE = 00

  Enable double buffering on all channels or do not use channels which are not set the double buffering mode.
- CHMODE = 01 or 10

  Do not use the channel which is not supporting the double buffering mode.

Issue: ADC: Offset correction fails in unsigned mode

In single ended, unsigned mode, a problem appears in low saturation (zero) when the offset correction is activated. The offset is removed from result and when a negative result appears, the result is not correct.

Workaround:

No workaround, but avoid using this correction method to cancel ΔV effect.