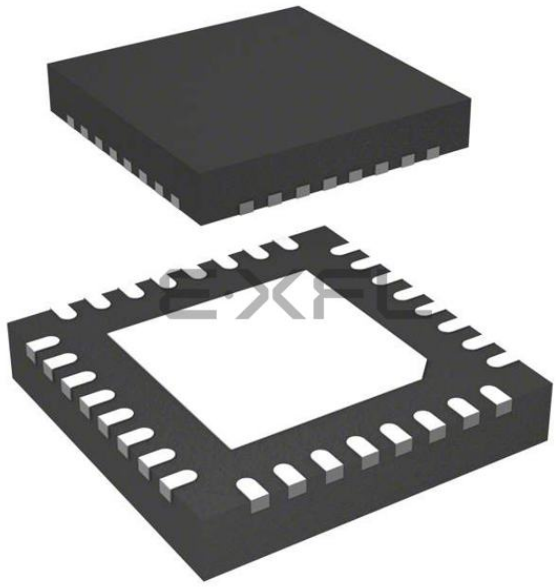

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16e5-m4ur

1. Ordering Information

Ordering Code	Package[1][2][3]	Flash [Bytes]	EEPROM [Bytes]	SRAM [Bytes]	Speed [MHz]	Power supply [V]	Temp. [°C]
ATxmega8E5-AU	32A (7x7mm TQFP)	8K + 2K	512	1K	32	1.6 – 3.6	-40 – 85
ATxmega8E5-AUR[4]							
ATxmega8E5-MU	32Z (5x5mm VQFN)						
ATxmega8E5-MUR[4]							
ATxmega8E5-M4U	32MA (4x4mm UQFN)						
ATxmega8E5-M4UR[4]							
ATxmega16E5-AU	32A (7x7mm TQFP)	16K + 4K	512	2K	32	1.6 – 3.6	-40 – 85
ATxmega16E5-AUR[4]							
ATxmega16E5-MU	32Z (5x5mm VQFN)						
ATxmega16E5-MUR[4]							
ATxmega16E5-M4U	32MA (4x4mm UQFN)						
ATxmega16E5-M4UR[4]							
ATxmega32E5-AU	32A (7x7mm TQFP)	32K + 4K	1K	4K	32	1.6 – 3.6	-40 – 85
ATxmega32E5AUR[4]							
ATxmega32E5-MU	32Z (5x5mm VQFN)						
ATxmega32E5-MUR[4]							
ATxmega32E5-M4U	32MA (4x4mm UQFN)						
ATxmega32E5-M4UR[4]							
ATxmega8E5-AN	32A (7x7mm TQFP)	8K + 2K	512	1K	32	1.6 – 3.6	-40 – 105
ATxmega8E5-ANR[4]							
ATxmega8E5-MN	32Z (5x5mm VQFN)						
ATxmega8E5-MNR[4]							
ATxmega8E5-M4UN	32MA (4x4mm UQFN)						
ATxmega8E5-M4UNR[4]							
ATxmega16E5-AN	32A (7x7mm TQFP)	16K + 4K	512	2K	32	1.6 – 3.6	-40 – 105
ATxmega16E5-ANR[4]							
ATxmega16E5-MN	32Z (5x5mm VQFN)						
ATxmega16E5-MNR[4]							
ATxmega16E5-M4UN	32MA (4x4mm UQFN)						
ATxmega16E5-M4UNR[4]							

Ordering Code	Package[1][2][3]	Flash [Bytes]	EEPROM [Bytes]	SRAM [Bytes]	Speed [MHz]	Power supply [V]	Temp. [°C]
ATxmega32E5-AN	32A (7x7mm TQFP)	32K + 4K	1K	4K	32	1.6 – 3.6	-40 – 105
ATxmega32E5ANR[4]							
ATxmega32E5-MN	32Z (5x5mm VQFN)						
ATxmega32E5-MNR[4]							
ATxmega32E5-M4UN	32MA (4x4mm UQFN)						
ATxmega32E5-M4UNR[4]							

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see “Packaging Information” on page 68.
4. Tape and Reel.

Package Type	
32A	32-lead, 7x7mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
32Z	32-lead, 0.5mm pitch, 5x5mm Very Thin quad Flat No Lead Package (VQFN) Sawn
32MA	32-lead, 0.4mm pitch, 4x4x0.60mm Ultra Thin Quad No Lead (UQFN) Package

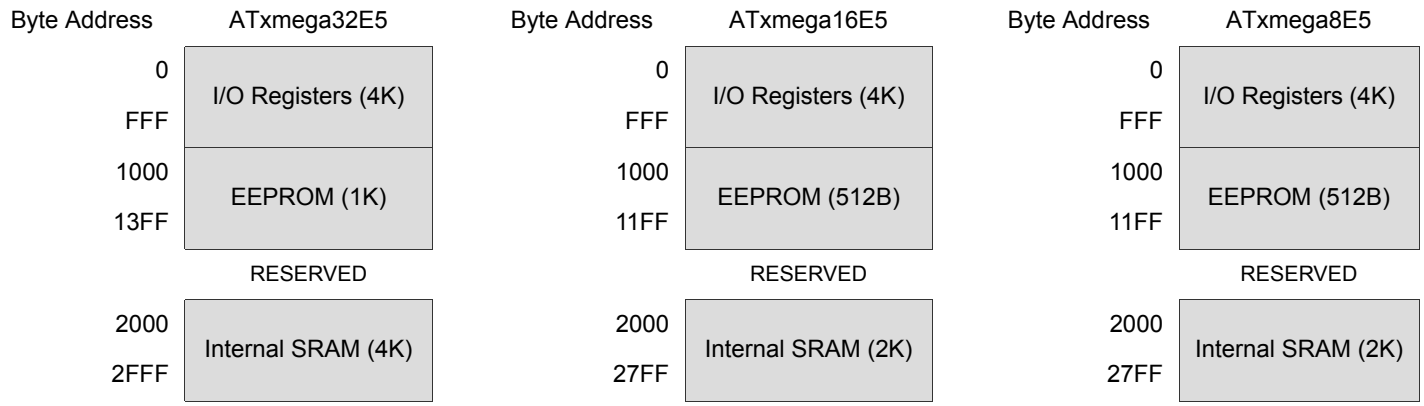
2. Typical Applications

Board controller	Sensor control	Motor control
User interface	Industrial control	Ballast control, Inverters
Communication bridges	Battery charger	Utility metering
Appliances		

8.5 Data Memory

The data memory contains the I/O memory, internal SRAM and EEPROM. The data memory is organized as one continuous memory section, see Table 8-2 on page 15. To simplify development, I/O Memory, EEPROM and SRAM will always have the same start addresses for all XMEGA devices.

Figure 8-2. Data Memory Map (hexadecimal value)



8.6 EEPROM

Atmel AVR XMEGA E5 devices have EEPROM for nonvolatile data storage. It is memory mapped and accessed in normal data space. The EEPROM supports both byte and page access. EEPROM allows highly efficient EEPROM reading and EEPROM buffer loading. When doing this, EEPROM is accessible using load and store instructions. EEPROM will always start at hexadecimal address 0x1000.

8.7 I/O Memory

The status and configuration registers for peripherals and modules, including the CPU, are addressable through I/O memory locations. All I/O locations can be accessed by the load (LD/LDS/LDD) and store (ST/STS/STD) instructions, which are used to transfer data between the 32 registers in the register file and the I/O memory. The IN and OUT instructions can address I/O memory locations in the range of 0x00 to 0x3F directly. In the address range 0x00 - 0x1F, single-cycle instructions for manipulation and checking of individual bits are available.

The I/O memory address for all peripherals and modules in XMEGA E5 is shown in the “Peripheral Module Address Map” on page 61.

8.7.1 General Purpose I/O Registers

The lowest four I/O memory addresses are reserved as general purpose I/O registers. These registers can be used for storing global variables and flags, as they are directly bit-accessible using the SBI, CBI, SBIS, and SBIC instructions.

8.8 Data Memory and Bus Arbitration

Since the data memory is organized as three separate sets of memories, the different bus masters (CPU, EDMA controller read and EDMA controller write, etc.) can access different memory sections at the same time.

8.9 Memory Timing

Read and write access to the I/O memory takes one CPU clock cycle. A write to SRAM takes one cycle, and a read from SRAM takes two cycles. For burst read (EDMA), new data are available every cycle. EEPROM page load (write) takes one cycle, and three cycles are required for read. For burst read, new data are available every second cycle. Refer to the instruction summary for more details on instructions and instruction timing.

11.3.2 32.768kHz Calibrated Internal Oscillator

This oscillator provides an approximate 32.768kHz clock. It is calibrated during production to provide a default frequency close to its nominal frequency. The calibration register can also be written from software for run-time calibration of the oscillator frequency. The oscillator employs a built-in prescaler, which provides both a 32.768kHz output and a 1.024kHz output.

11.3.3 32.768kHz Crystal Oscillator

A 32.768kHz crystal oscillator can be connected between the TOSC1 and TOSC2 pins and enables a dedicated low frequency oscillator input circuit. A low power mode with reduced voltage swing on TOSC2 is available. This oscillator can be used as a clock source for the system clock and RTC, and as the DFLL reference clock.

11.3.4 0.4 - 16MHz Crystal Oscillator

This oscillator can operate in four different modes optimized for different frequency ranges, all within 0.4 - 16MHz.

11.3.5 8MHz Calibrated Internal Oscillator

The 8MHz calibrated internal oscillator is the default system clock source after reset. It is calibrated during production to provide a default frequency close to its nominal frequency. The calibration register can also be written from software for run-time calibration of the oscillator frequency. The oscillator employs a built-in prescaler, with 2MHz output. The default output frequency at start-up and after reset is 2MHz. A low power mode option can be used to enable fast system wake-up from power-save mode. In all other modes, the low power mode can be enabled to significantly reduce the power consumption of the internal oscillator.

11.3.6 32MHz Run-time Calibrated Internal Oscillator

The 32MHz run-time calibrated internal oscillator is a high-frequency oscillator. It is calibrated during production to provide a default frequency close to its nominal frequency. A digital frequency looked loop (DFLL) can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy. This oscillator can also be adjusted and calibrated to any frequency between 30 and 55MHz.

11.3.7 External Clock Sources

The XTAL1 and XTAL2 pins can be used to drive an external oscillator, either a quartz crystal or a ceramic resonator. XTAL1 or pin 4 of port C (PC4) can be used as input for an external clock signal. The TOSC1 and TOSC2 pins are dedicated to driving a 32.768kHz crystal oscillator.

11.3.8 PLL with 1x-31x Multiplication Factor

The built-in phase locked loop (PLL) can be used to generate a high-frequency system clock. The PLL has a user-selectable multiplication factor of from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

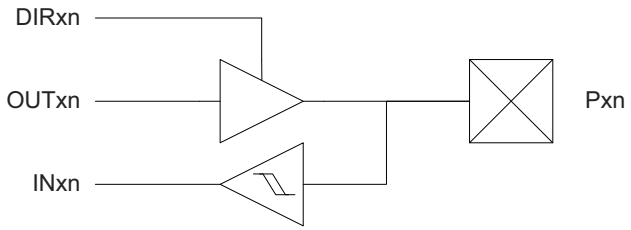
Program address (base address)	Source	Interrupt description
0x0024	TCC5_INT_base	Timer/counter 5 on port C interrupt base
0x002C	SPIC_INT_vect	SPI on port C interrupt vector
0x002E	USARTC0_INT_base	USART 0 on port C interrupt base
0x0034	NVM_INT_base	Non-Volatile Memory interrupt base
0x0038	XCL_INT_base	XCL (programmable logic) module interrupt base
0x003C	PORTA_INT_vect	Port A interrupt vector
0x003E	ACA_INT_base	Analog comparator on Port A interrupt base
0x0044	ADCA_INT_base	Analog to digital converter on Port A interrupt base
0x0046	PORTD_INT_vect	Port D interrupt vector
0x0048	TCD5_INT_base	Timer/counter 5 on port D interrupt base
0x0050	USARTD0_INT_base	USART 0 on port D interrupt base

16.3 Output Driver

All port pins (Pxn) have programmable output configuration. The port pins also have configurable slew rate limitation to reduce electromagnetic emission.

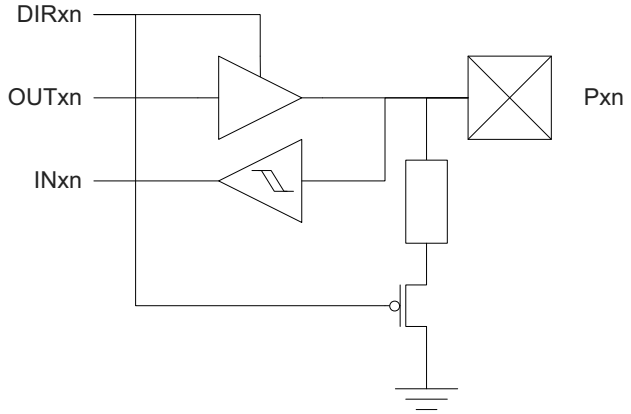
16.3.1 Push-pull

Figure 16-1. I/O Configuration - Totem-pole



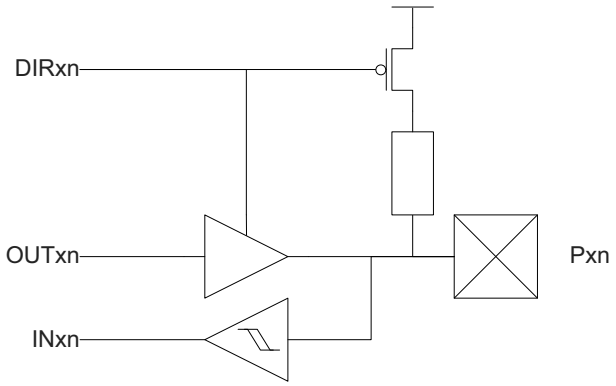
16.3.2 Pull-down

Figure 16-2. I/O Configuration - Totem-pole with Pull-down (on input)



16.3.3 Pull-up

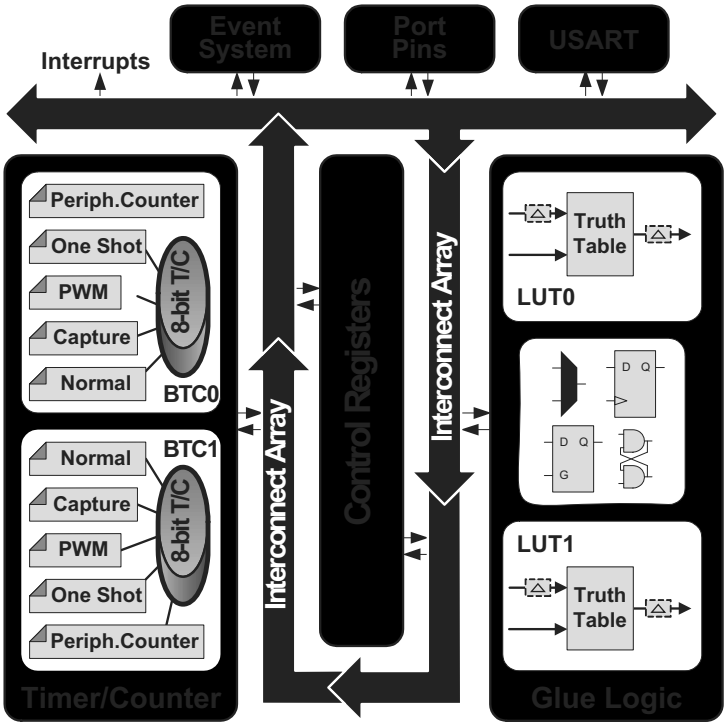
Figure 16-3. I/O Configuration - Totem-pole with Pull-up (on input)



The LUT works in all sleep modes. Combined with event system and one I/O pin, the LUT can wake-up the system if, and only if, condition on up to three input pins is true.

A block diagram of the programmable logic unit with extensions and closely related peripheral modules (in grey) is shown in Figure 26-1.

Figure 26-1. XMEGA Custom Logic Module and Closely Related Peripherals



30. AC – Analog Comparator

30.1 Features

- Two Analog Comparators
- Selectable propagation delay
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog Comparator output available on pin
- Flexible Input Selection
  - All pins on the port
  - Output from the DAC
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal AVCC voltage
- Interrupt and event generation on
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection
- Source of asynchronous event

30.2 Overview

The Analog Comparator (AC) compares the voltage level on two inputs and gives a digital output based on this comparison. The Analog Comparator may be configured to give interrupt requests and/or synchronous/asynchronous events upon several different combinations of input change.

One important property of the Analog Comparator when it comes to the dynamic behavior, is the hysteresis. This parameter may be adjusted in order to find the optimal operation for each application.

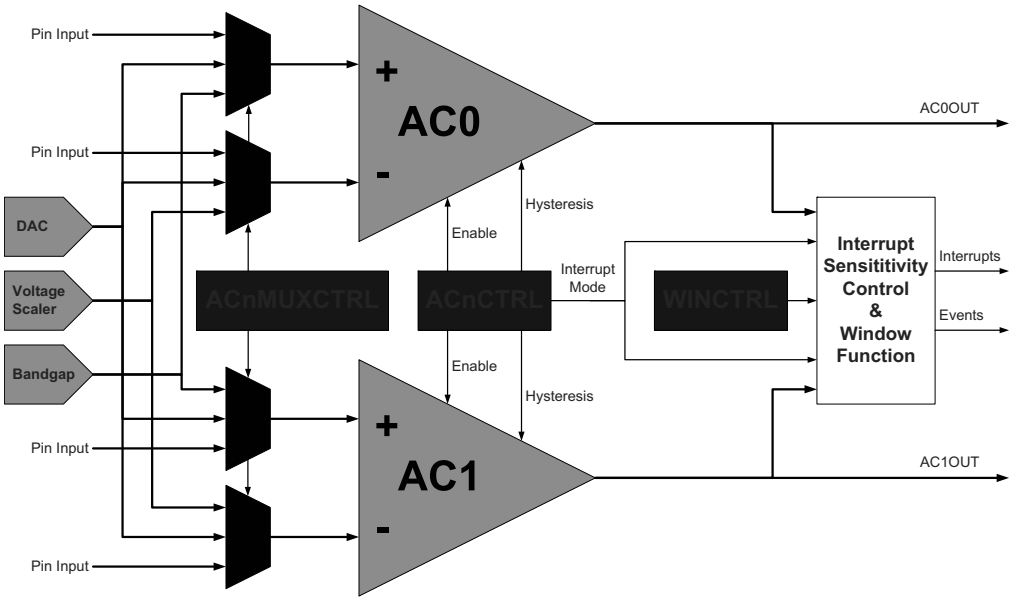
The input section includes analog port pins, several internal signals and a 64-level programmable voltage scaler. The analog comparator output state can also be directly available on a pin for use by external devices. Using as pair they can also be set in Window mode to monitor a signal compared to a voltage window instead of a voltage level.

A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

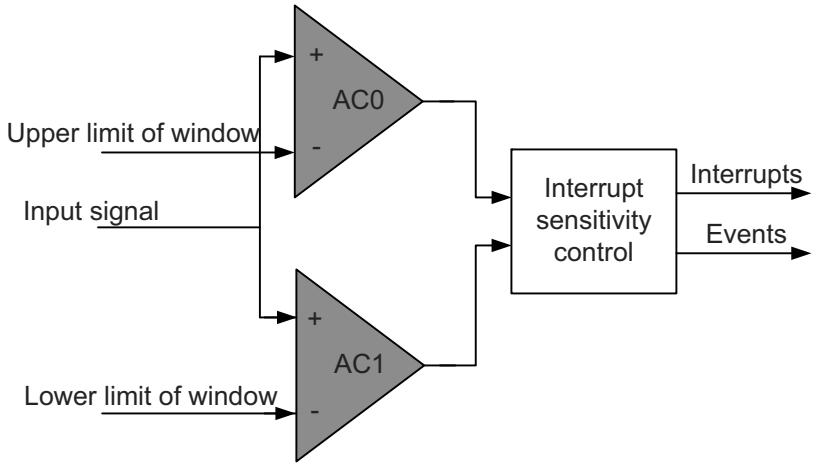
PORTA has one AC pair. Notation is ACA.

Figure 30-1. Analog Comparator Overview



The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 30-2.

Figure 30-2. Analog Comparator Window Function



Mnemonics	Operands	Description	Operation	Flags	#Clocks
SPM	Z+	Store Program Memory and Post-Increment by 2	(RAMPZ:Z) ← R1:R0, Z ← Z + 2	None	-
IN	Rd, A	In From I/O Location	Rd ← I/O(A)	None	1
OUT	A, Rr	Out To I/O Location	I/O(A) ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	1(1)
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2(1)
XCH	Z, Rd	Exchange RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp	None	2
LAS	Z, Rd	Load and Set RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp v (Z)	None	2
LAC	Z, Rd	Load and Clear RAM location	Temp ← Rd, Rd ← (Z), (Z) ← ($FFh – Rd) ● (Z)	None	2
LAT	Z, Rd	Load and Toggle RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp ⊕ (Z)	None	2
Bit and bit-test instructions					
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0, C ← Rd(7)	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0, C ← Rd(0)	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7)	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0) ↔ Rd(7..4)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	I/O(A, b) ← 1	None	1
CBI	A, b	Clear Bit in I/O Register	I/O(A, b) ← 0	None	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Gain error	0.5x gain		-1		%
		1x gain		-1		
		8x gain		-1		
		64x gain		-1.5		
	Offset error, input referred	0.5x gain		10		mV
		1x gain		5		
		8x gain		5		
		64x gain		5		

36.7 DAC Characteristics

Table 36-11. Power Supply, Reference, and Output Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	
AV_{REF}	External reference voltage		1.0		V_{CC}- 0.6	V
$R_{channel}$	DC output impedance				50	Ω
	Linear output voltage range		0.15		V_{REF}-0.15	V
R_{AREF}	Reference input resistance			>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
	Minimum Resistance load		1			kΩ
	Maximum capacitance load				100	pF
		1000Ω serial resistance			1	nF
	Output sink/source	Operating within accuracy specification			AV_{CC}/1000	mA
		Safe operation			10	

Table 36-12. Clock and Timing

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
f_{DAC}	Conversion rate	C_{load}=100pF, maximum step size	Normal mode	0		1000	ksps
			Low power mode	0		500	

36.14 SPI Characteristics

Figure 36-5. SPI Timing Requirements in Master Mode

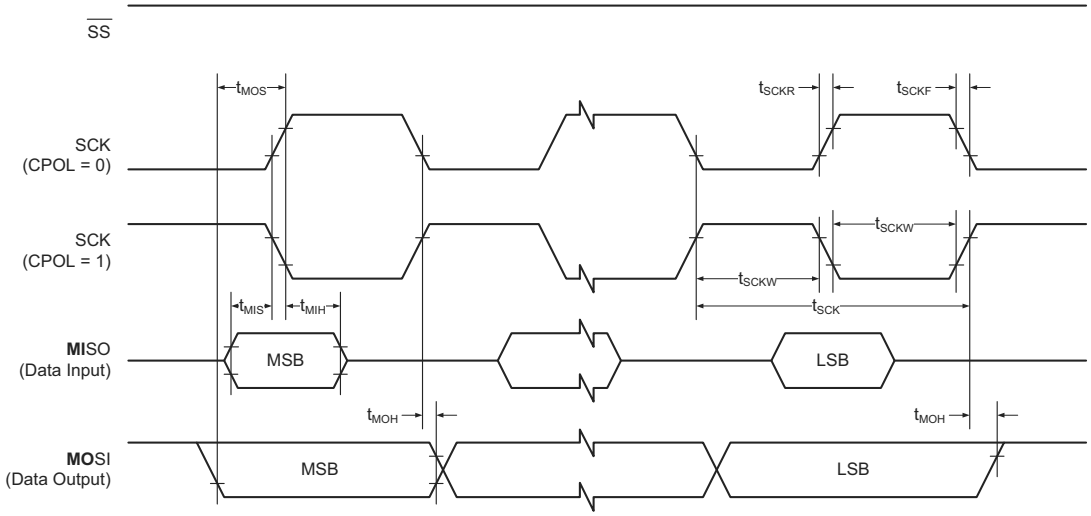
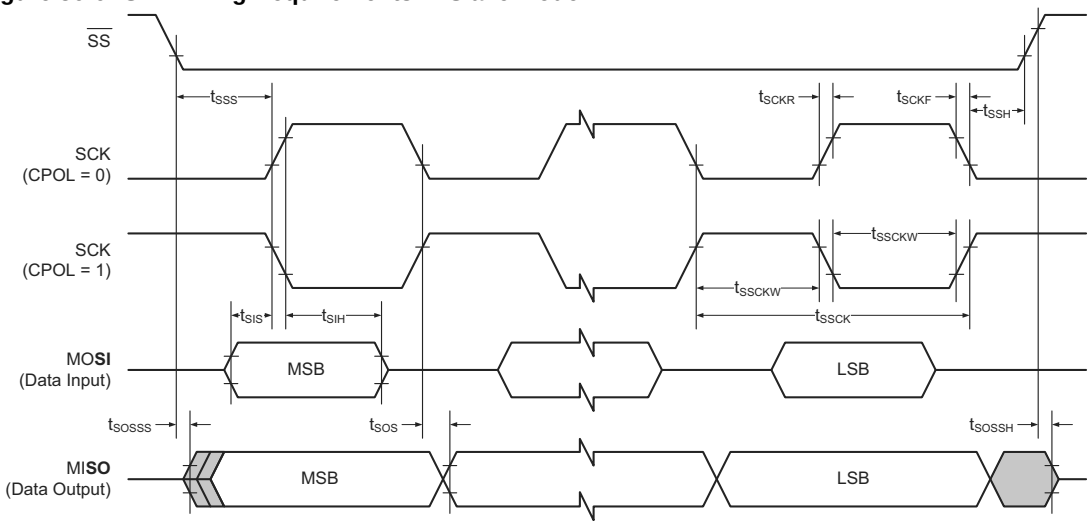


Figure 36-6. SPI Timing Requirements in Slave Mode



37. Typical Characteristics

37.1 Current Consumption

37.1.1 Active Mode Supply Current

Figure 37-1. Active Mode Supply Current vs. Frequency

f_{SYS} = 0 – 1MHz external clock, T = 25°C

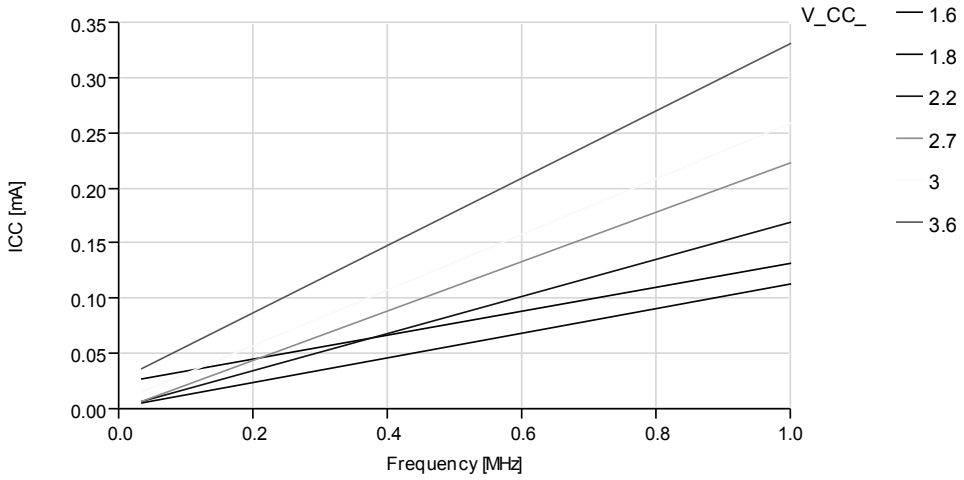


Figure 37-2. Active Mode Supply Current vs. Frequency

f_{SYS} = 0 – 32MHz external clock, T = 25°C

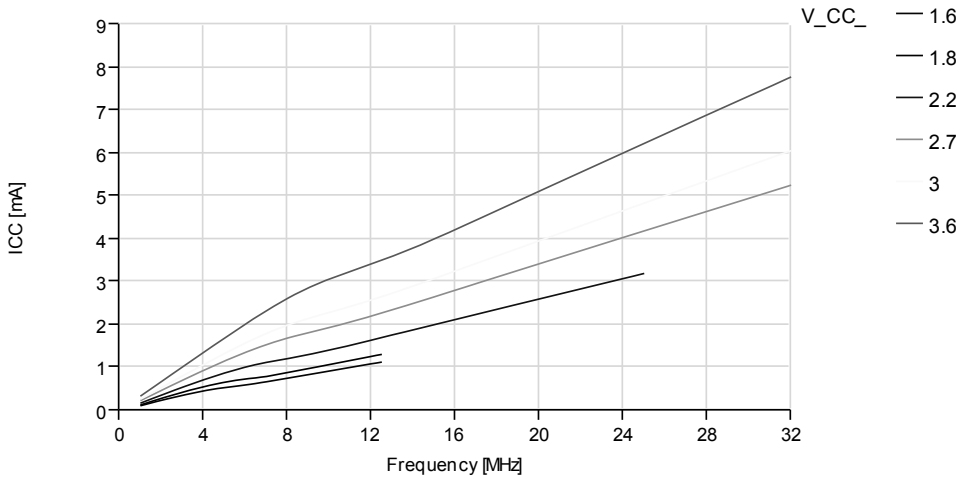


Figure 37-15.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

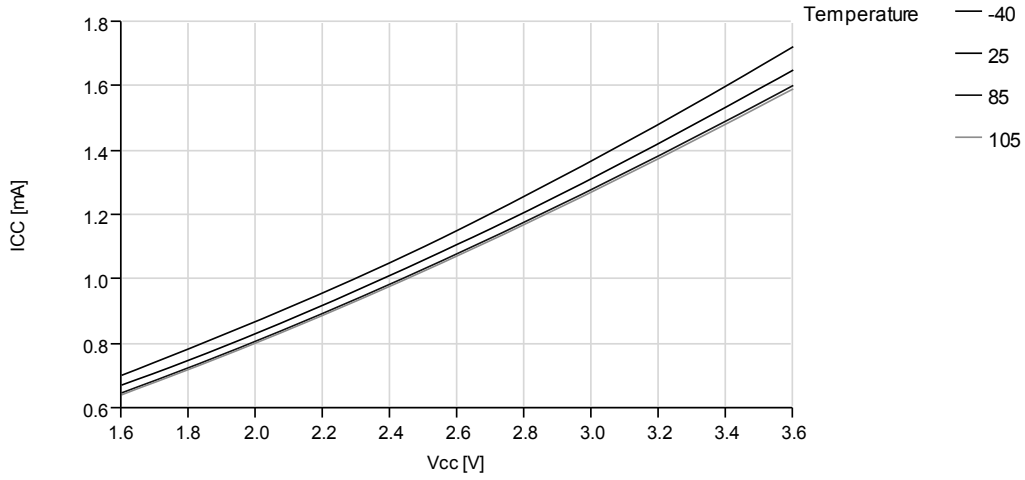
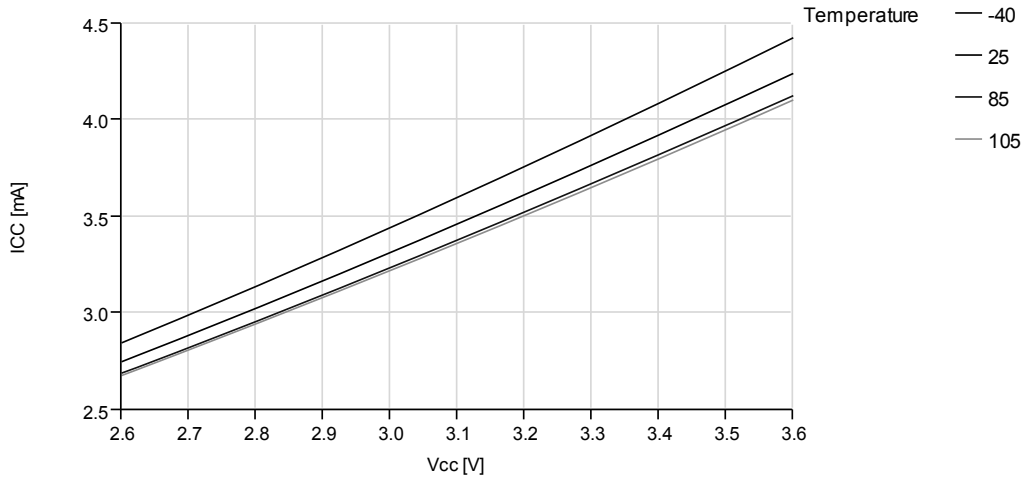


Figure 37-16.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator



37.2 I/O Pin Characteristics

37.2.1 Pull-up

Figure 37-23.I/O pin pull-up Resistor Current vs. Input Voltage

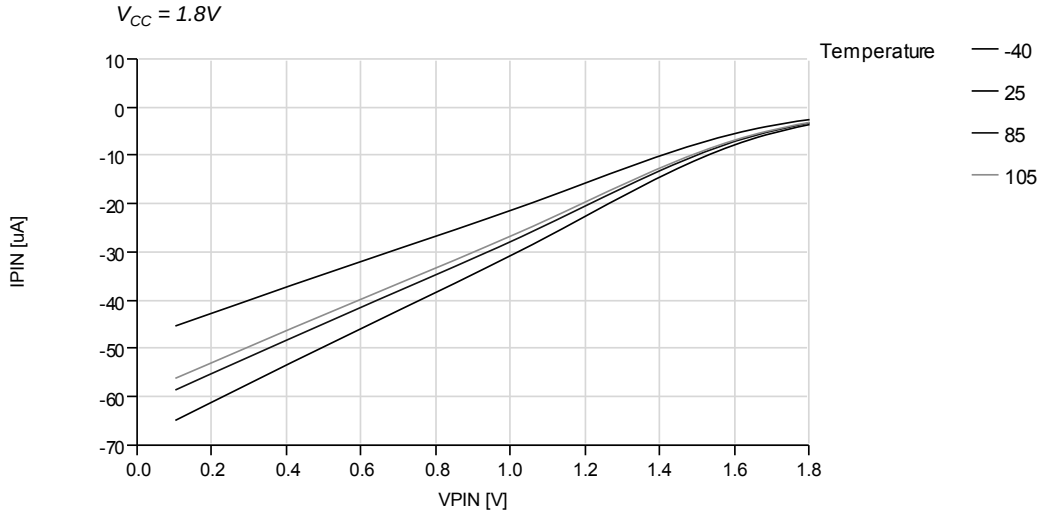


Figure 37-24.I/O Pin Pull-up Resistor Current vs. Input Voltage

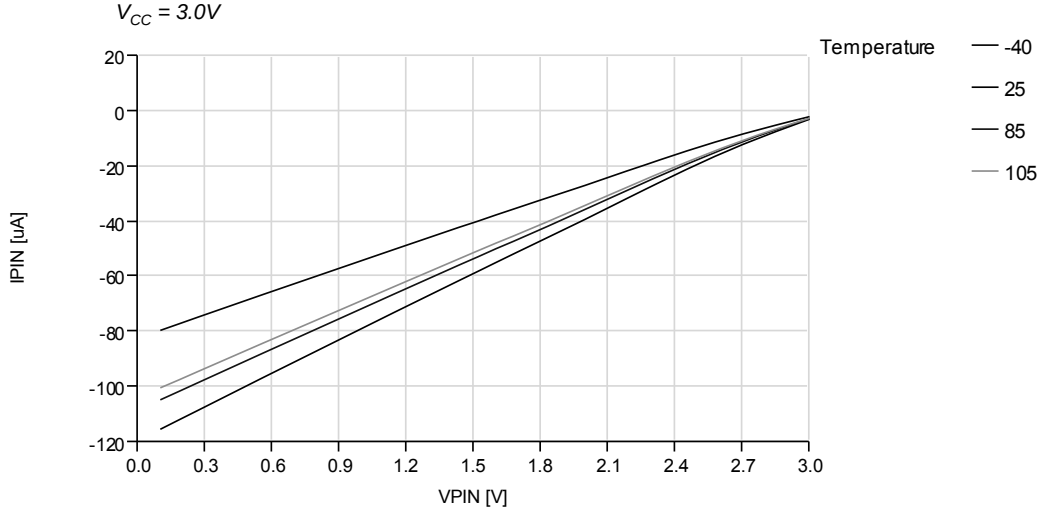
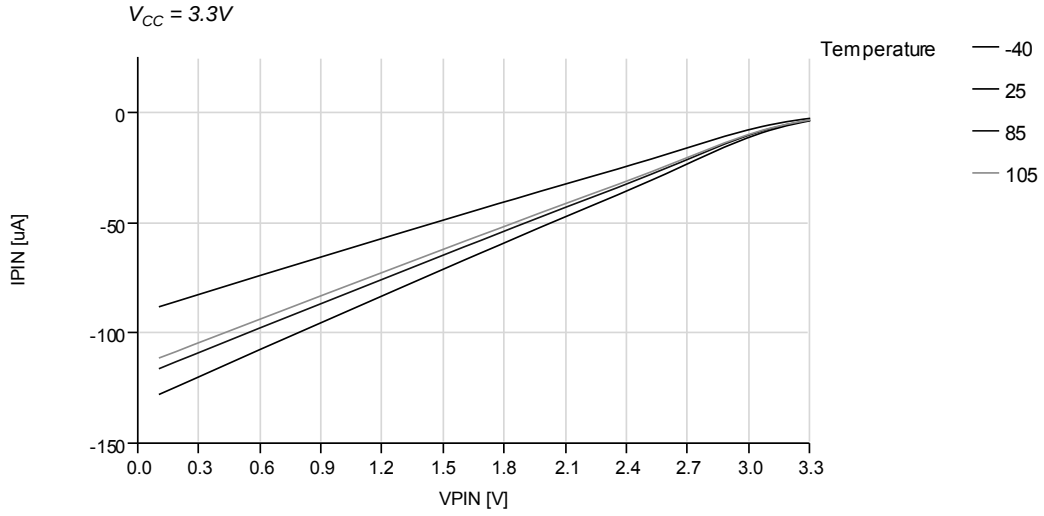


Figure 37-25.I/O Pin Pull-up Resistor Current vs. Input Voltage



37.2.2 Output Voltage vs. Sink/Source Current

Figure 37-26.I/O Pin Output Voltage vs. Source Current

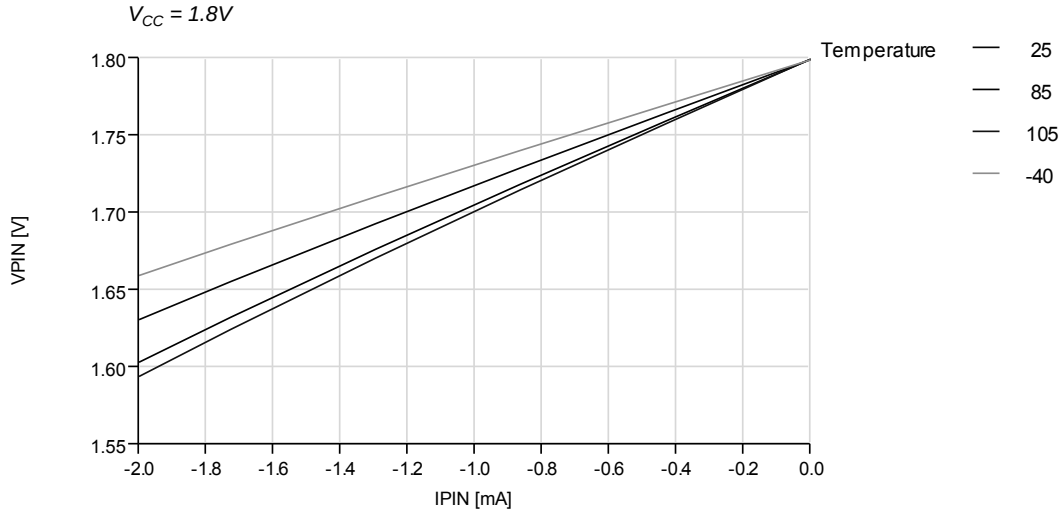


Figure 37-51.Analog Comparator Hysteresis vs. V_{CC}

Large hysteresis

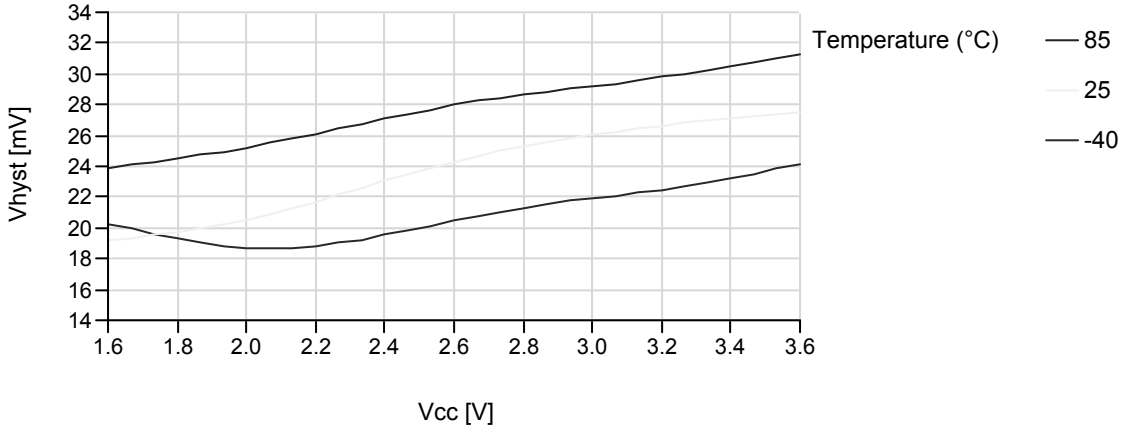


Figure 37-52.Analog Comparator Propagation Delay vs. V_{CC}

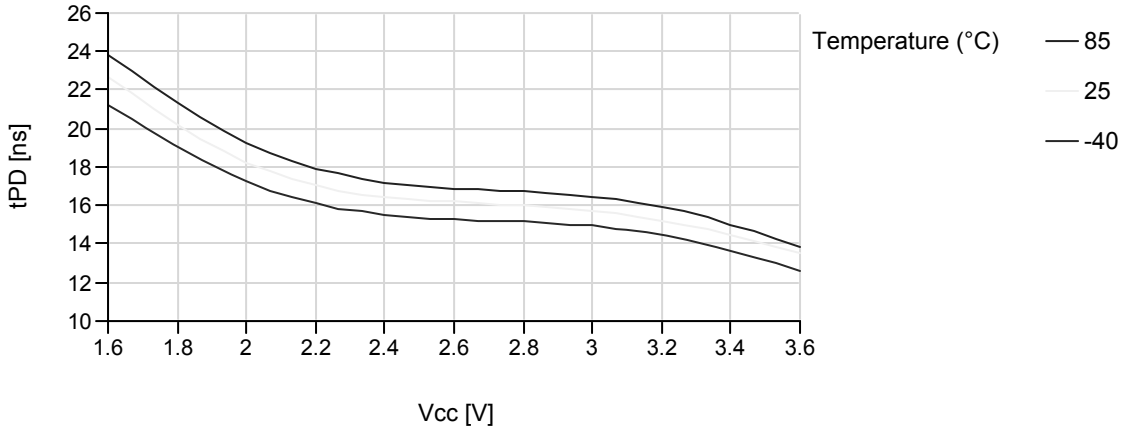
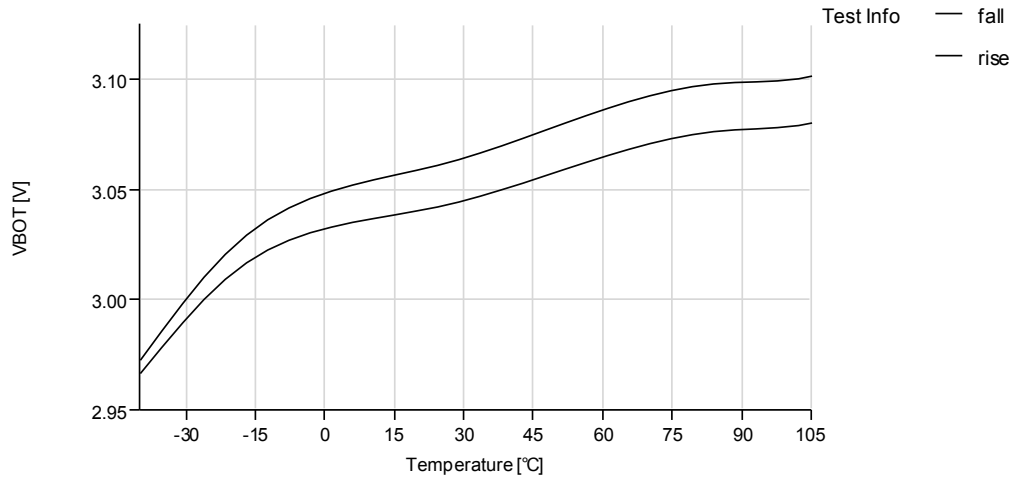


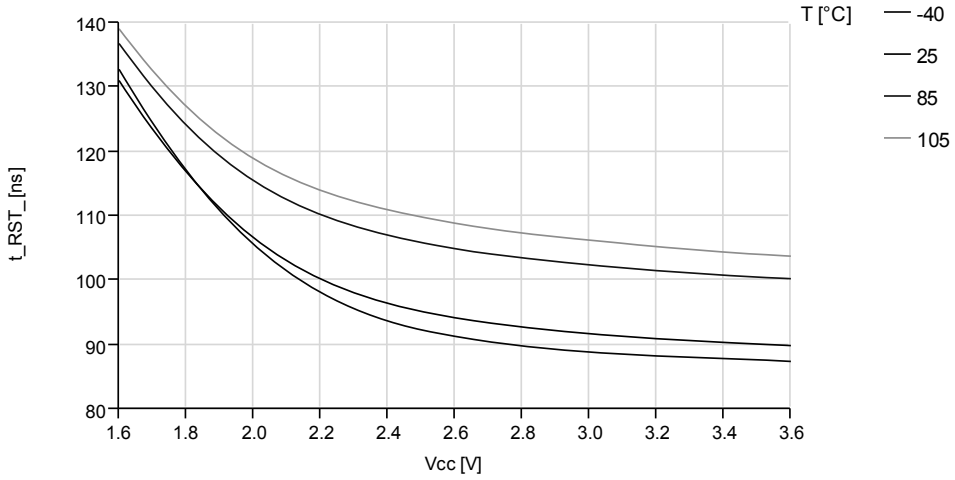
Figure 37-61.BOD Thresholds vs. Temperature

BOD level = 3.0V



37.8 External Reset Characteristics

Figure 37-62.Minimum Reset Pin Pulse Width vs. V_{CC}



Issue: ADC: Averaging is failing when channel scan is enabled

For a correct operation, the averaging must complete on the on-going channel before incrementing the input offset. In the current implementation, the input offset is incremented after the ADC sampling is done.

Workaround:

None.

Issue: ADC: Averaging in single conversion requires multiple conversion triggers

For a normal operation, an unique start of conversion trigger starts a complete average operation. Then, for N-samples average operation, we should have:

- One start of conversion
- N conversions + average
- Optional interrupt when the Nth conversion/last average is completed

On silicon we need:

- N start of conversion

The two additional steps are well done.

Workaround:

- Set averaging configuration
- N starts of conversion by polling the reset of START bit
- Wait for interrupt flag (end of averaging)

Issue: ADC accumulator sign extends the result in unsigned mode averaging

In unsigned mode averaging, when the msb is going high(1), measurements are considered as negative when right shift is used. This sets the unused most significant bits once the shift is done.

Workaround:

Mask to zero the unused most significant bits once shift is done.

Issue: ADC: Free running average mode issue

In free running mode the ADC stops the ongoing averaging as soon as free running bit is disabled. This creates the need to flush the ADC before starting the next conversion since one or two conversions might have taken place in the internal accumulator.

Workaround:

Disable and re-enable the ADC before the start of next conversion in free running average mode.

Issue: ADC: Event triggered conversion in averaging mode

If the ADC is configured as event triggered in averaging mode, then a single event does not complete the entire averaging as it should be.

Workaround:

In the current revision, N events are needed for completing averaging on N samples.

39. Revision History

Please note that referring page numbers in this section are referred to this document. The referring revision in this document section are referring to the document revision.

39.1 8153K – 08/2016

1.	“Ordering Information” on page 2: Ordering codes for UQFN packages corrected from M4N/M4NR to M4UN/M4UNR.

39.2 8153J – 11/2014

1.	Changed error for ESR parameter in Table 36-27 on page 86.
2.	Changed the use of capital letters in heading, figure titles, and table headings.

39.3 8153I – 08/2014

1.	Removed preliminary from the front page.
2.	Updated with ESR info in Table 36-27 on page 86.
3.	Added errata on Automatic port override on PORT C in Section 38. “Errata – ATxmega32E5 / ATxmega16E5 / ATxmega8E5” on page 136.
4.	Added errata on Sext timer not implemented in slave mode in Section 38. “Errata – ATxmega32E5 / ATxmega16E5 / ATxmega8E5” on page 136.

39.4 8153H – 07/2014

1.	“Ordering Information” on page 2: Added ordering codes for XMEGA E5 devices @105°C.
2.	Electrical characteristics updates: “Current Consumption” : Added power-down numbers for 105°C and updated values in Table 36-3 on page 73. “ Flash and EEPROM Characteristics” : Added Flash and EEPROM write/erase cycles and data retention for 105°C in Table 36-18 on page 82.
3.	Changed Vcc to AVcc in Section 28. “ADC – 12-bit Analog to Digital Converter” on page 51 and in Section 30.1 “Features” on page 54.
4.	32.768 KHz changed to 32 kHz in the heading in Section 36.13.4 on page 84 and in Table 36-23 on page 84.
5.	Changed back page according to datasheet template 2014-0502.

39.5 8153G – 10/2013

1.	Updated wake-up time from power-save mode for 32MHz internal oscillator from 0.2µs to 5.0µs in Table 36-5 on page 75.

39.6 8153F – 08/2013

1.	TWI characteristics: Units of Data setup time ($t_{SU;DAT}$) changed from µs to ns in Table 36-30 on page 91.