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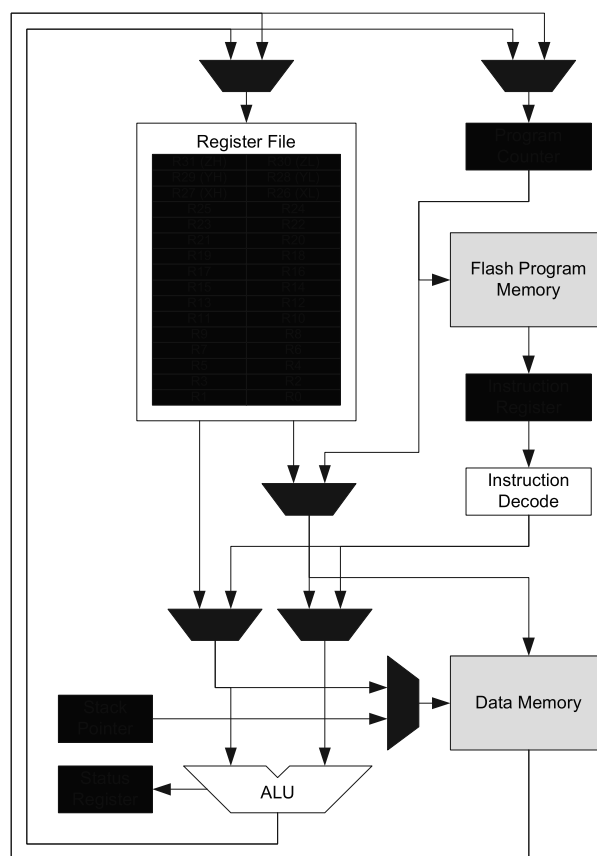
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32e5-an

Figure 7-1. Block Diagram of the AVR CPU Architecture



The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The ALU is directly connected to the fast-access register file. The 32 x 8-bit general purpose working registers all have single clock cycle access time allowing single-cycle arithmetic logic unit (ALU) operation between registers or between a register and an immediate. Six of the 32 registers can be used as three 16-bit address pointers for program and data space addressing, enabling efficient address calculations.

The memory spaces are linear. The data memory space and the program memory space are two different memory spaces.

The data memory space is divided into I/O registers, SRAM, and memory mapped EEPROM.

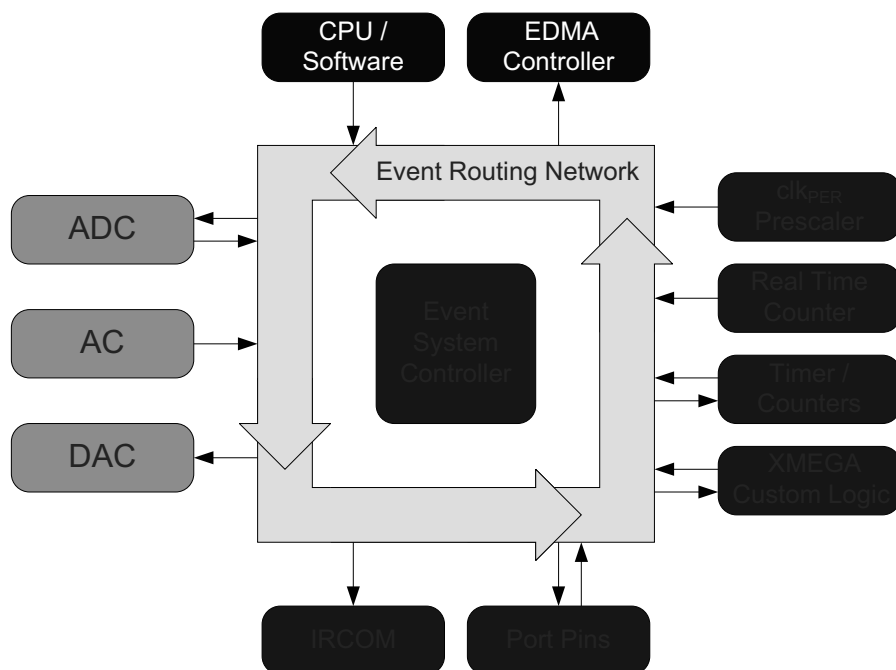
All I/O status and control registers reside in the lowest 4KB addresses of the data memory. This is referred to as the I/O memory space. The lowest 64 addresses can be accessed directly, or as the data space locations from 0x00 to 0x3F. The rest is the extended I/O memory space, ranging from 0x0040 to 0x0FFF. I/O registers here must be accessed as data space locations using load (LD/LDS/LDD) and store (ST/STS/STD) instructions.

The SRAM holds data. Code execution from SRAM is not supported. It can easily be accessed through the five different addressing modes supported in the AVR architecture. The first SRAM address is 0x2000.

Data addresses 0x1000 to 0x1FFF are reserved for EEPROM.

The program memory is divided in two sections, the application program section and the boot program section. Both sections have dedicated lock bits for write and read/write protection. The SPM instruction that is used for self-programming of the application flash memory must reside in the boot program section. The application section contains an application table section with separate lock bits for write and read/write protection. The application table section can be used for save storing of nonvolatile data in the program memory.

Figure 10-1. Event System Overview and Connected Peripherals



The event routing network consists of eight software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow up to eight parallel event configurations and routing. The maximum routing latency of an external event is two peripheral clock cycles due to re-synchronization, but several peripherals can directly use the asynchronous event without any clock delay. The event system works in all power sleep modes, but only asynchronous events can be routed in sleep modes where the system clock is not available.

11. System Clock and Clock options

11.1 Features

- Fast start-up time
- Safe run-time clock switching
- Internal Oscillators:
 - 32MHz run-time calibrated and tuneable oscillator
 - 8MHz calibrated oscillator with 2MHz output option and fast start-up
 - 32.768kHz calibrated oscillator
 - 32kHz Ultra Low Power (ULP) oscillator with 1kHz output
- External clock options
 - 0.4 - 16MHz Crystal Oscillator
 - 32kHz crystal oscillator with digital correction
 - External clock input in selectable pin location
- PLL with 20 - 128MHz output frequency
 - Internal and external clock options and 1 to 31x multiplication
 - Lock detector
- Clock Prescalers with 1x to 2048x division
- Fast peripheral clocks running at two and four times the CPU clock frequency
- Automatic Run-Time Calibration of the 32MHz internal oscillator
- External oscillator and PLL lock failure detection with optional non maskable interrupt

11.2 Overview

Atmel AVR XMEGA E5 devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the 32MHz internal oscillator to remove frequency drift over voltage and temperature. An oscillator failure monitor can be enabled to issue a nonmaskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz output of the 8MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

Figure 11-1 on page 21 presents the principal clock system in the XMEGA E5 family of devices. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers, as described in “Power Management and Sleep Modes” on page 23.

12.3.3 Power-save Mode

Power-save mode is identical to power down, with one exception. If the real-time counter (RTC) is enabled, it will keep running during sleep, and the device can also wake up from either an RTC overflow or compare match interrupt. Low power mode option of 8MHz internal oscillator enables instant oscillator wake-up time. This reduces the MCU wake-up time or enables the MCU wake-up from UART bus.

12.3.4 Standby Mode

Standby mode is identical to power down, with the exception that the enabled system clock sources are kept running while the CPU, peripheral, and RTC clocks are stopped. This reduces the wake-up time. The low power option of 8MHz internal oscillator can be enabled to further reduce the power consumption.

12.3.5 Extended Standby Mode

Extended standby mode is identical to power-save mode, with the exception that the enabled system clock sources are kept running while the CPU and peripheral clocks are stopped. This reduces the wake-up time. The low power option of 8MHz internal oscillator can be enabled to further reduce the power consumption.

13.4.2 Brownout Detection

The on-chip brownout detection (BOD) circuit monitors the V_{CC} level during operation by comparing it to a fixed, programmable level that is selected by the BODLEVEL fuses. If disabled, BOD is forced on at the lowest level during chip erase and when the PDI is enabled.

13.4.3 External Reset

The external reset circuit is connected to the external RESET pin. The external reset will trigger when the RESET pin is driven below the RESET pin threshold voltage, V_{RST} , for longer than the minimum pulse period, t_{EXT} . The reset will be held as long as the pin is kept low. The RESET pin includes an internal pull-up resistor.

13.4.4 Watchdog Reset

The watchdog timer (WDT) is a system function for monitoring correct program operation. If the WDT is not reset from the software within a programmable timeout period, a watchdog reset will be given. The watchdog reset is active for one to two clock cycles of the 2MHz internal oscillator. For more details, see “WDT – Watchdog Timer” on page 27.

13.4.5 Software Reset

The software reset makes it possible to issue a system reset from software by writing to the software reset bit in the reset control register. The reset will be issued within two CPU clock cycles after writing the bit. It is not possible to execute any instruction from when a software reset is requested until it is issued.

13.4.6 Program and Debug Interface Reset

The program and debug interface reset contains a separate reset source that is used to reset the device during external programming and debugging. This reset source is accessible only from external debuggers and programmers.

15. Interrupts and Programmable Multilevel Interrupt Controller

15.1 Features

- Short and predictable interrupt response time
- Separate interrupt configuration and vector address for each interrupt
- Programmable multilevel interrupt controller
 - Interrupt prioritizing according to level and vector address
 - Three selectable interrupt levels for all interrupts: low, medium, and high
 - Selectable, round-robin priority scheme within low-level interrupts
 - Non-maskable interrupts for critical functions
- Interrupt vectors optionally placed in the application section or the boot loader section

15.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

15.3 Interrupt Vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA E5 devices are shown in Table 15-1. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA AU manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 15-1. The program address is the word address.

Table 15-1. Peripheral Module Address Map

Program address (base address)	Source	Interrupt description
0x0000	RESET	
0x0002	OSCF_INT_vect	Crystal oscillator failure and PLL lock failure interrupt vector (NMI)
0x0004	PORTR_INT_vect	Port R Interrupt vector
0x0006	EDMA_INT_base	EDMA Controller Interrupt base
0x000E	RTC_INT_base	Real time counter interrupt base
0x0012	PORTC_INT_vect	Port C interrupt vector
0x0014	TWIC_INT_base	Two-wire interface on Port C interrupt base
0x0018	TCC4_INT_base	Timer/counter 4 on port C interrupt base

16. I/O Ports

16.1 Features

- 26 general purpose input and output pins with individual configuration
- Output driver with configurable driver and pull settings:
 - Totem-pole
 - Wired-AND
 - Wired-OR
 - Bus-keeper
 - Inverted I/O
- Input with asynchronous sensing with interrupts and events
 - Sense both edges
 - Sense rising edges
 - Sense falling edges
 - Sense low level
- Optional pull-up and pull-down resistor on input and Wired-OR/AND configurations
- Optional slew rate control per I/O port
- Asynchronous pin change sensing that can wake the device from all sleep modes
- One port interrupt with pin masking per I/O port
- Efficient and safe access to port pins
 - Hardware read-modify-write through dedicated toggle/clear/set registers
 - Configuration of multiple pins in a single operation
 - Mapping of port registers into bit-accessible I/O memory space
- Peripheral clocks output on port pin
- Real-time counter clock output to port pin
- Event channels can be output on port pin
- Remapping of digital peripheral pin functions
 - Selectable USART and timer/counters input/output pin locations
 - Selectable Analog Comparator output pin locations

16.2 Overview

One port consists of up to eight pins ranging from pin 0 to 7. Each port pin can be configured as input or output with configurable driver and pull settings. They also implement asynchronous input sensing with interrupt and events for selectable pin change conditions.

Asynchronous pin-change sensing means that a pin change can wake the device from all sleep modes, including the modes where no clocks are running.

All functions are individual and configurable per pin, but several pins can be configured in a single operation. The pins have hardware read-modify-write (RMW) functionality for safe and correct change of drive value and/or pull resistor configuration. The direction of one port pin can be changed without unintentionally changing the direction of any other pin.

The port pin configuration also controls input and output selection of other device functions. It is possible to have both the peripheral clock and the real-time clock output to a port pin, and available for external use. The same applies to events from the event system that can be used to synchronize and control external functions. Other digital peripherals, such as USART, timer/counters, and analog comparator output can be remapped to selectable pin locations in order to optimize pin-out versus application needs.

The notations of the ports are PORTA, PORTC, PORTD, and PORTR.

27. CRC – Cyclic Redundancy Check Generator

27.1 Features

- Cyclic redundancy check (CRC) generation and checking for
 - Communication data
 - Program or data in flash memory
 - Data in SRAM and I/O memory space
- Integrated with flash memory, EDMA controller, and CPU
 - Continuous CRC on data going through an EDMA channel
 - Automatic CRC of the complete or a selectable range of the flash memory
 - CPU can load data to the CRC generator through the I/O interface
- CRC polynomial software selectable to:
 - CRC-16 (CRC-CCITT)
 - CRC-32 (IEEE 802.3)
- Zero remainder detection

27.2 Overview

A cyclic redundancy check (CRC) is an error detection technique test algorithm used to find accidental errors in data, and it is commonly used to determine the correctness of a data transmission, and data present in the data and program memories. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum. When the same data are later received or read, the device or application repeats the calculation. If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

Typically, an n-bit CRC applied to a data block of arbitrary length will detect any single error burst not longer than n bits (any single alteration that spans no more than n bits of the data), and will detect the fraction $1-2^{-n}$ of all longer error bursts. The CRC module in XMEGA devices supports two commonly used CRC polynomials; CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3).

- CRC-16:
 - Polynomial: $x^{16} + x^{12} + x^5 + 1$
 - Hex Value: 0x1021
- CRC-32:
 - Polynomial: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
 - Hex Value: 0x04C11DB7

32. Pinout and Pin Functions

The device pinout is shown in “Pinout and Block Diagram” on page 4. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

32.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

32.1.1 Operation/Power Supply

V _{CC}	Digital supply voltage
AV _{CC}	Analog supply voltage
GND	Ground

32.1.2 Port Interrupt Functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNCR	Port pin with full synchronous and full asynchronous interrupt function

32.1.3 Analog Functions

ACn	Analog Comparator input pin n
ACnOUT	Analog Comparator n Output
ADCn	Analog to Digital Converter input pin n
DACn	Digital to Analog Converter output pin n
A _{REF}	Analog Reference input pin

32.1.4 Timer/Counter and WEX Functions

OCnx	Output Compare Channel x for timer/counter n
OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

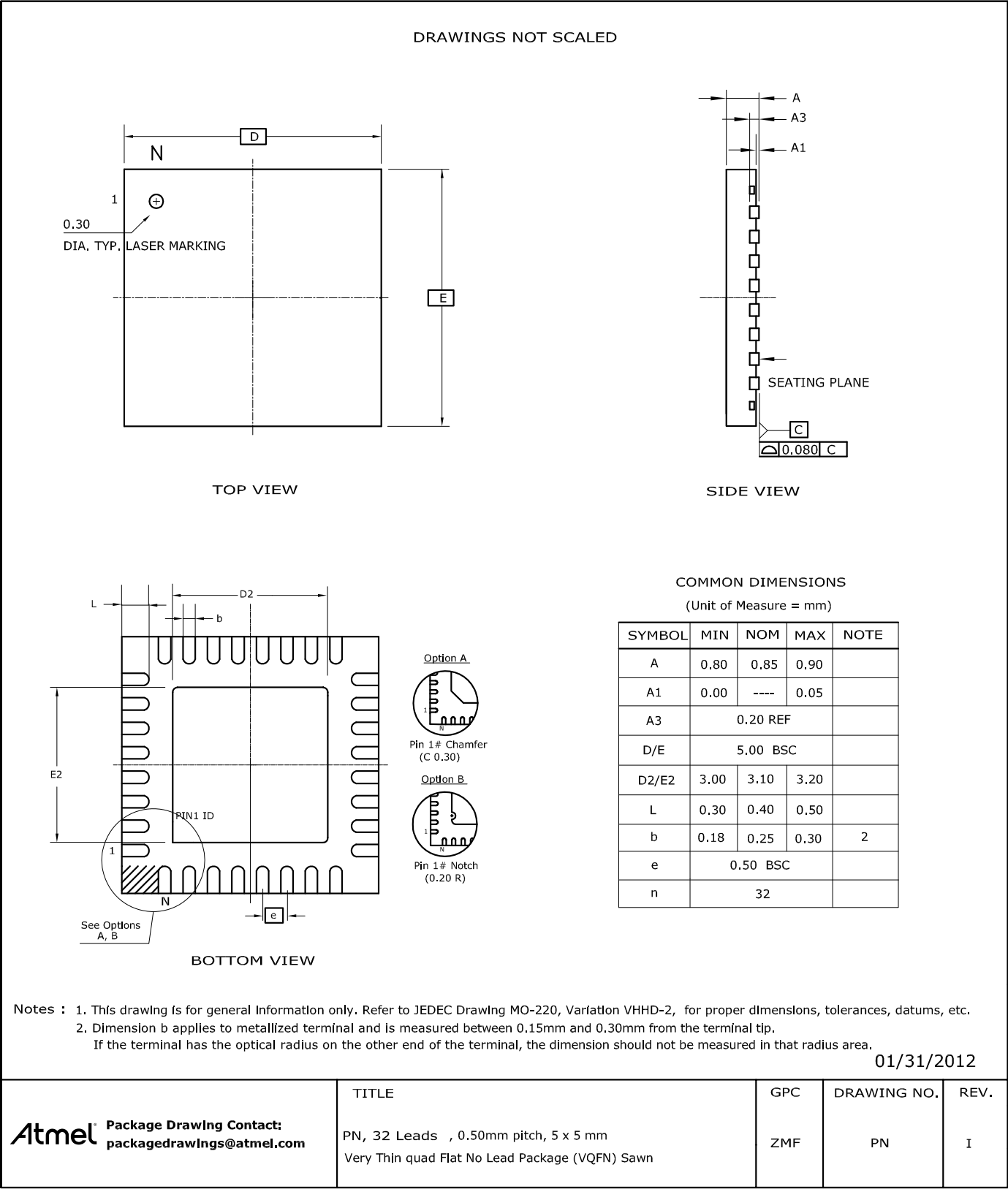
32.1.5 Communication Functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
SCLIN	Serial Clock In for TWI when external driver interface is enabled
SCLOUT	Serial Clock Out for TWI when external driver interface is enabled
SDAIN	Serial Data In for TWI when external driver interface is enabled
SDAOUT	Serial Data Out for TWI when external driver interface is enabled

34. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	$Rd \leftarrow Rd + Rr$	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	$Rd \leftarrow Rd + 1:Rd + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	$Rd \leftarrow Rd - Rr$	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	$Rd \leftarrow Rd - K$	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	$Rd \leftarrow Rd - K - C$	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	$Rd + 1:Rd \leftarrow Rd + 1:Rd - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	$Rd \leftarrow Rd \bullet Rr$	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	$Rd \leftarrow Rd \bullet K$	Z,N,V,S	1
OR	Rd, Rr	Logical OR	$Rd \leftarrow Rd \vee Rr$	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	$Rd \leftarrow Rd \oplus Rr$	Z,N,V,S	1
COM	Rd	One's Complement	$Rd \leftarrow \$FF - Rd$	Z,C,N,V,S	1
NEG	Rd	Two's Complement	$Rd \leftarrow \$00 - Rd$	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (\$FFh - K)$	Z,N,V,S	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V,S	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V,S	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V,S	1
SER	Rd	Set Register	$Rd \leftarrow \$FF$	None	1
MUL	Rd,Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr (UU)$	Z,C	2
MULS	Rd,Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr (SS)$	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr (SU)$	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr << 1 (UU)$	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	$R1:R0 \leftarrow Rd \times Rr << 1 (SS)$	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr << 1 (SU)$	Z,C	2
DES	K	Data Encryption	if (H = 0) then R15:R0 \leftarrow Encrypt(R15:R0, K) else if (H = 1) then R15:R0 \leftarrow Decrypt(R15:R0, K)		1/2
Branch instructions					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow 0$	None	2
EIJMP		Extended Indirect Jump to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow EIND$	None	2
JMP	k	Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Call Subroutine	$PC \leftarrow PC + k + 1$	None	2 / 3 ⁽¹⁾

Mnemonics	Operands	Description	Operation	Flags	#Clocks
SPM	Z+	Store Program Memory and Post-Increment by 2	(RAMPZ:Z) ← R1:R0, Z ← Z + 2	None	-
IN	Rd, A	In From I/O Location	Rd ← I/O(A)	None	1
OUT	A, Rr	Out To I/O Location	I/O(A) ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	1 ⁽¹⁾
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2 ⁽¹⁾
XCH	Z, Rd	Exchange RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp	None	2
LAS	Z, Rd	Load and Set RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp v (Z)	None	2
LAC	Z, Rd	Load and Clear RAM location	Temp ← Rd, Rd ← (Z), (Z) ← (\$FFh – Rd) • (Z)	None	2
LAT	Z, Rd	Load and Toggle RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp ⊕ (Z)	None	2
Bit and bit-test instructions					
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0, C ← Rd(7)	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0, C ← Rd(0)	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7)	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0) ↔ Rd(7..4)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	I/O(A, b) ← 1	None	1
CBI	A, b	Clear Bit in I/O Register	I/O(A, b) ← 0	None	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1



36. Electrical Characteristics

All typical values are measured at $T = 25^{\circ}\text{C}$ unless other temperature condition is given. All minimum and maximum values are valid across operating temperature and voltage unless other conditions are given.

36.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage	-0.3		4	V
I_{VCC}	Current into a V_{CC} pin			200	mA
I_{GND}	Current out of a Gnd pin			200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}	-0.5		$V_{CC}+0.5$	V
I_{PIN}	I/O pin sink/source current	-25		25	mA
T_A	Storage temperature	-65		150	$^{\circ}\text{C}$
T_j	Junction temperature			150	

36.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-1 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 36-1. General Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage	1.6		3.6	V
AV_{CC}	Analog supply voltage	1.6		3.6	
T_A	Temperature range	-40		85	$^{\circ}\text{C}$
T_j	Junction temperature	-40		105	

Table 36-2. Operating Voltage and Frequency

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	$V_{CC} = 1.6\text{V}$	0		12	MHz
		$V_{CC} = 1.8\text{V}$	0		12	
		$V_{CC} = 2.7\text{V}$	0		32	
		$V_{CC} = 3.6\text{V}$	0		32	

The maximum CPU clock frequency depends on V_{CC} . As shown in Figure 36-1 the frequency vs. V_{CC} curve is linear between $1.8\text{V} < V_{CC} < 2.7\text{V}$.

36.5 I/O Pin Characteristics

The I/O pins comply with the JEDEC LVTTTL and LVCMOS specification and the high- and low-level input and output voltage limits reflect or exceed this specification.

Table 36-6. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
$I_{OH}^{(1)}$ / $I_{OL}^{(2)}$	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage, except XTAL1 and RESET pin	$V_{CC} = 2.4 - 3.6V$		$0.7 \cdot V_{CC}$		$V_{CC} + 0.5$	V
		$V_{CC} = 1.6 - 2.4V$		$0.8 \cdot V_{CC}$		$V_{CC} + 0.5$	
V_{IL}	Low level input voltage, except XTAL1 and RESET pin	$V_{CC} = 2.4 - 3.6V$		-0.5		$0.3 \cdot V_{CC}$	
		$V_{CC} = 1.6 - 2.4V$		-0.5		$0.2 \cdot V_{CC}$	
V_{OH}	High level output voltage	$V_{CC} = 3.3V$	$I_{OH} = -4mA$	2.6	3.1		
		$V_{CC} = 3.0V$	$I_{OH} = -3mA$	2.1	2.7		
		$V_{CC} = 1.8V$	$I_{OH} = -1mA$	1.4	1.7		
V_{OL}	Low level output voltage	$V_{CC} = 3.3V$	$I_{OL} = 8mA$		0.20	0.76	
		$V_{CC} = 3.0V$	$I_{OL} = 5mA$		0.15	0.64	
		$V_{CC} = 1.8V$	$I_{OL} = 3mA$		0.10	0.46	
I_{IN}	Input leakage current	$T = 25^{\circ}C$			<0.01	1.0	μA
R_P	Pull/buss keeper resistor				27		k Ω

- Notes:
1. The sum of all I_{OH} for PA[7:5] on PORTA must not exceed 100mA.
The sum of all I_{OH} for PA[4:0] on PORTA must not exceed 200mA.
The sum of all I_{OH} for PORTD and PORTR must not exceed 100mA.
The sum of all I_{OH} for PORTC and PDI must not exceed 100mA.
 2. The sum of all I_{OL} for PA[7:5] on PORTA must not exceed 100mA.
The sum of all I_{OL} for PA[4:0] on PORTA must not exceed 100mA.
The sum of all I_{OL} for PORTD and PORTR must not exceed 100mA.
The sum of all I_{OL} for PORTC PDI must not exceed 100mA.

36.6 ADC Characteristics

Table 36-7. Power Supply, Reference, and Input Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		$V_{CC} - 0.3$		$V_{CC} + 0.3$	V
V_{REF}	Reference voltage		1		$AV_{CC} - 0.6$	
R_{in}	Input resistance	Switched			4.5	k Ω
C_{in}	Input capacitance	Switched			5	pF
R_{AREF}	Reference input resistance	(leakage only)		>10		M Ω
C_{AREF}	Reference input capacitance	Static load		7		pF

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Gain error	0.5x gain		-1		%
		1x gain		-1		
		8x gain		-1		
		64x gain		-1.5		
	Offset error, input referred	0.5x gain		10		mV
		1x gain		5		
		8x gain		5		
		64x gain		5		

36.7 DAC Characteristics

Table 36-11. Power Supply, Reference, and Output Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		$V_{CC} - 0.3$		$V_{CC} + 0.3$	
AV_{REF}	External reference voltage		1.0		$V_{CC} - 0.6$	V
$R_{channel}$	DC output impedance				50	Ω
	Linear output voltage range		0.15		$V_{REF} - 0.15$	V
R_{AREF}	Reference input resistance			>10		M Ω
C_{AREF}	Reference input capacitance	Static load		7		pF
	Minimum Resistance load		1			k Ω
	Maximum capacitance load				100	pF
		1000 Ω serial resistance			1	nF
	Output sink/source	Operating within accuracy specification			$AV_{CC}/1000$	mA
		Safe operation			10	

Table 36-12. Clock and Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{DAC}	Conversion rate	$C_{load}=100\text{pF}$, maximum step size	Normal mode	0	1000	ksp/s
			Low power mode	0	500	

Table 36-19. Programming Time

Parameter	Condition	Min.	Typ. ⁽¹⁾	Max.	Units
Chip Erase	32KB Flash, EEPROM ⁽²⁾		50		ms
	16KB Flash, EEPROM ⁽²⁾		45		
	8KB Flash, EEPROM ⁽²⁾		42		
Flash	Page erase		4		
	Page write		4		
	Atomic page erase and write		8		
EEPROM	Page erase		4		
	Page write		4		
	Atomic page erase and write		8		

- Notes:
1. Programming is timed from the 2MHz output of 8MHz internal oscillator.
 2. EEPROM is not erased if the EESAVE fuse is programmed.

Figure 37-3. Active Mode Supply Current vs. V_{CC}

$f_{SYS} = 32.768\text{kHz}$ internal oscillator

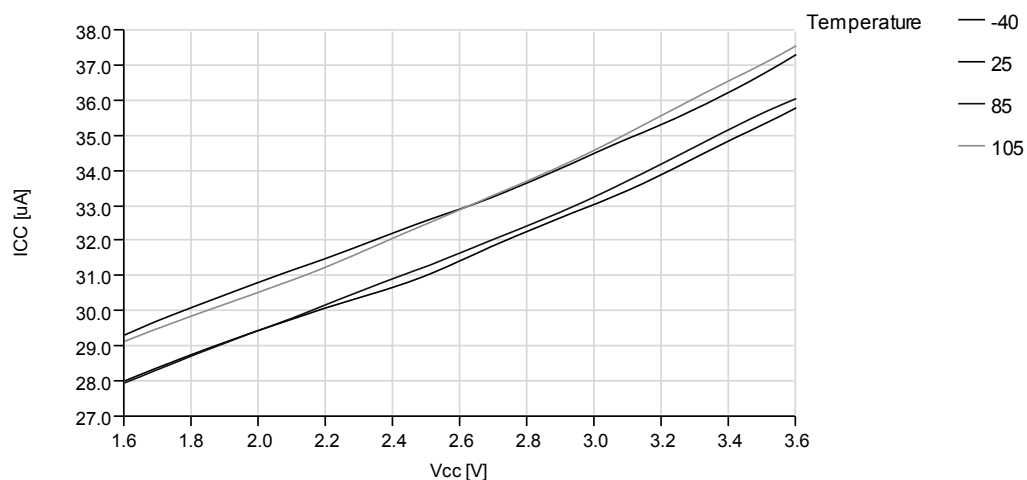


Figure 37-4. Active Mode Supply Current vs. V_{CC}

$f_{SYS} = 1\text{MHz}$ external clock

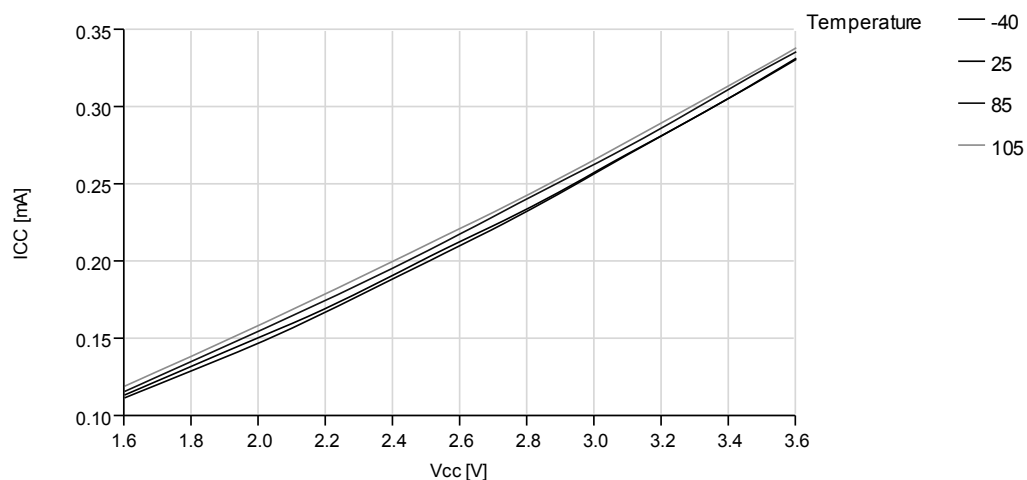


Figure 37-7. Active mode Supply Current vs. V_{CC}

$f_{SYS} = 32\text{MHz}$ internal oscillator prescaled to 8MHz

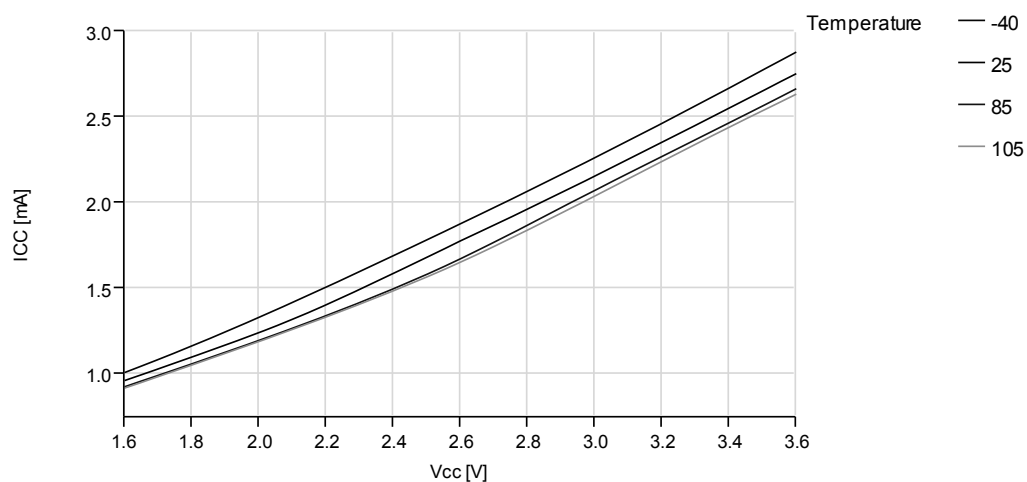
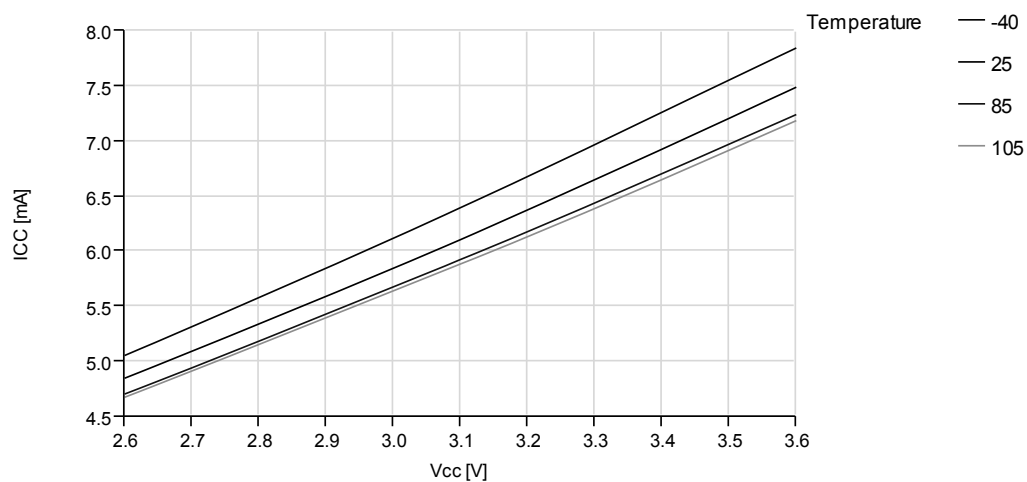


Figure 37-8. Active Mode Supply Current vs. V_{CC}

$f_{SYS} = 32\text{MHz}$ internal oscillator



37.2 I/O Pin Characteristics

37.2.1 Pull-up

Figure 37-23.I/O pin pull-up Resistor Current vs. Input Voltage

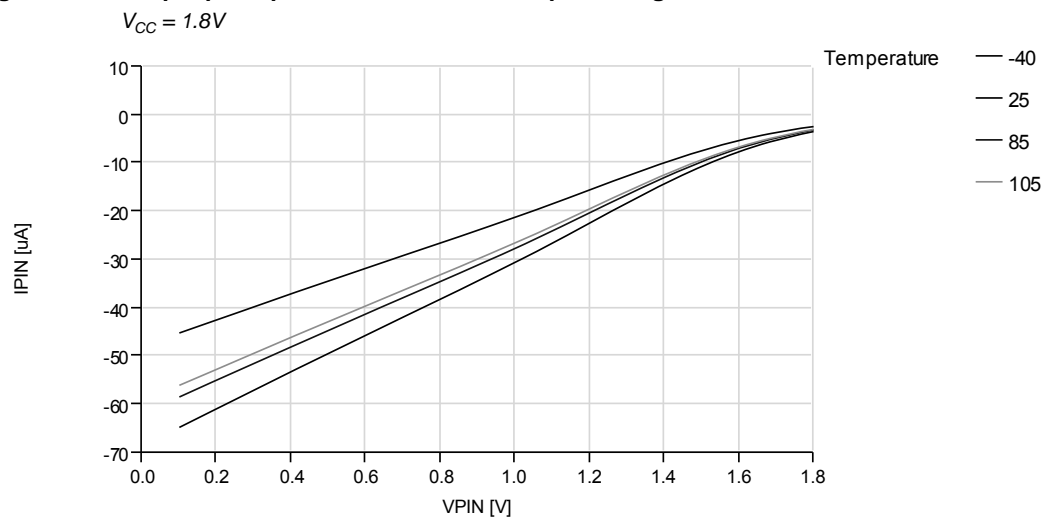
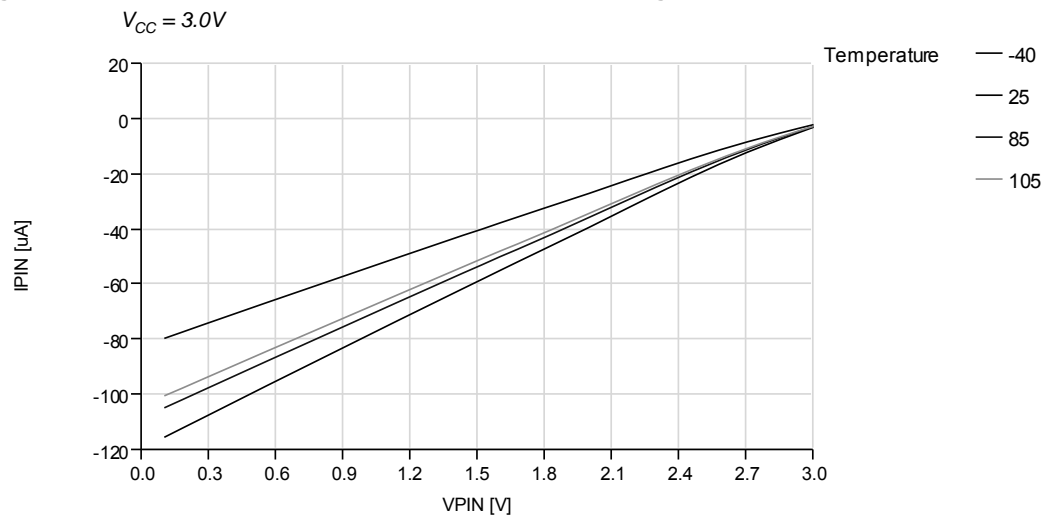


Figure 37-24.I/O Pin Pull-up Resistor Current vs. Input Voltage



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