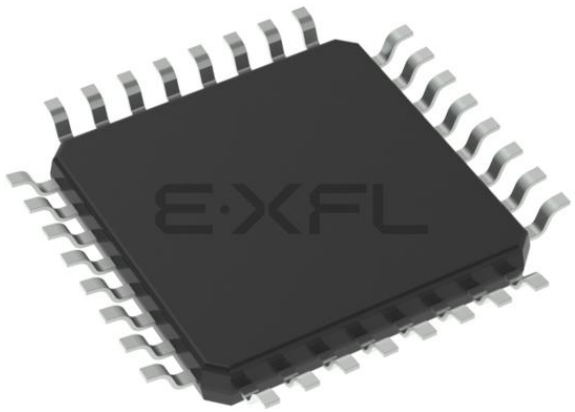

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32e5-anr

the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 71.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 8-1.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 8-1. Device ID Bytes for Atmel AVR XMEGA E5 Devices

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega32E5	4C	95	1E
ATxmega16E5	45	94	1E
ATxmega8E5	41	93	1E

8.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

8.4 Fuses and Lock Bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, startup configuration, etc.

The lock bits are used to set protection levels for the different flash sections (i.e., if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

An un-programmed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are reprogrammable like the flash program memory.

9. EDMA – Enhanced DMA Controller

9.1 Features

- The EDMA Controller allows data transfers with minimal CPU intervention
  - from data memory to data memory
  - from data memory to peripheral
  - from peripheral to data memory
  - from peripheral to peripheral
- Four peripheral EDMA channels with separate:
  - transfer triggers
  - interrupt vectors
  - addressing modes
  - data matching
- Two peripheral channels can be combined to one standard channel with separate:
  - transfer triggers
  - interrupt vectors
  - addressing modes
  - data search
- Programmable channel priority
- From 1byte to 128KB of data in a single transaction
  - Up to 64K block transfer with repeat
  - 1 or 2 bytes burst transfers
- Multiple addressing modes
  - Static
  - Increment
- Optional reload of source and destination address at the end of each
  - Burst
  - Block
  - Transaction
- Optional Interrupt on end of transaction
- Optional connection to CRC Generator module for CRC on EDMA data

9.2 Overview

The four-channel enhanced direct memory access (EDMA) controller can transfer data between memories and peripherals, and thus offload these tasks from the CPU. It enables high data transfer rates with minimum CPU intervention, and frees up CPU time. The four EDMA channels enable up to four independent and parallel transfers.

The EDMA controller can move data between SRAM and peripherals, between SRAM locations and directly between peripheral registers. With access to all peripherals, the EDMA controller can handle automatic transfer of data to/from communication modules. The EDMA controller can also read from EEPROM memory.

Data transfers are done in continuous bursts of 1 or 2 bytes. They build block transfers of configurable size from 1 byte to 64KB. Repeat option can be used to repeat once each block transfer for single transactions up to 128KB. Source and destination addressing can be static or incremental. Automatic reload of source and/or destination addresses can be done after each burst or block transfer, or when a transaction is complete. Application software, peripherals, and events can trigger EDMA transfers.

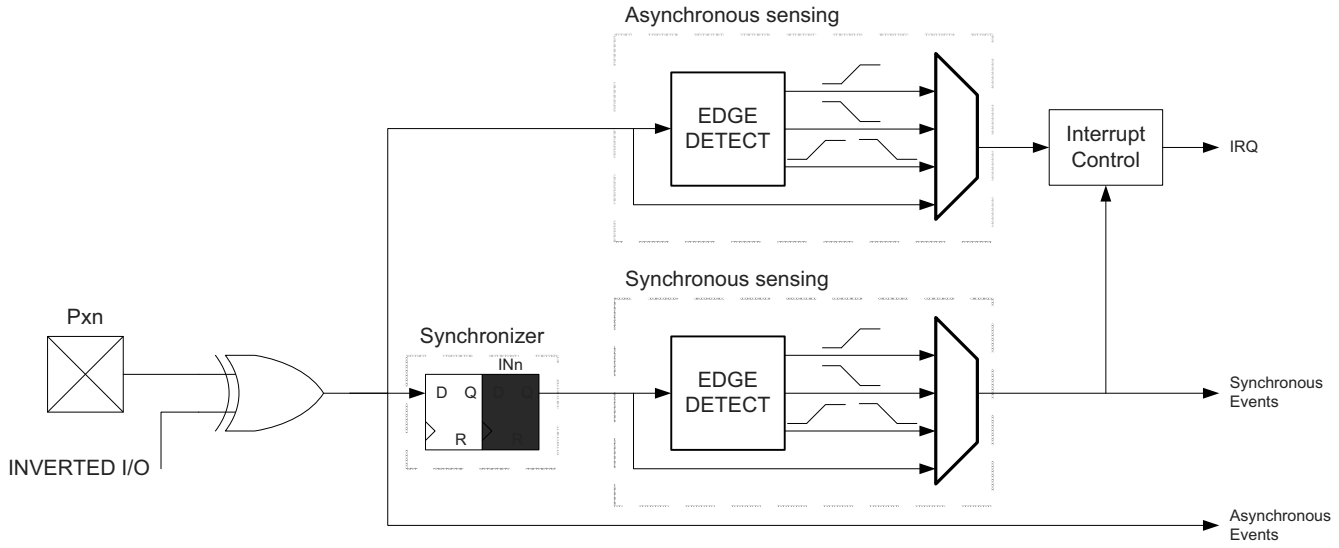
The four EDMA channels have individual configuration and control settings. This includes source, destination, transfer triggers, and transaction sizes. They have individual interrupt settings. Interrupt requests can be generated when a transaction is complete or when the EDMA controller detects an error on an EDMA channel.

To enable flexibility in transfers, channels can be interlinked so that the second takes over the transfer when the first is finished.

16.4 Input Sensing

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in Figure 16-7.

Figure 16-7. Input Sensing System Overview



When a pin is configured with inverted I/O, the pin value is inverted before the input sensing.

16.5 Alternate Port Functions

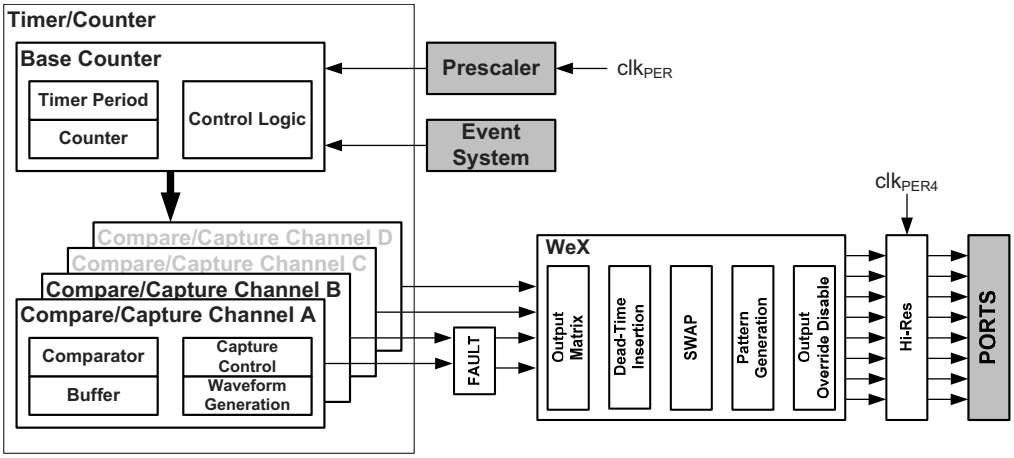
Most port pins have alternate pin functions in addition to being a general purpose I/O pin. When an alternate function is enabled, it might override the normal port pin function or pin value. This happens when other peripherals that require pins are enabled or configured to use pins. If and how a peripheral will override and use pins is described in the section for that peripheral. “Pinout and Pin Functions” on page 57 shows which modules on peripherals that enable alternate functions on a pin, and which alternate functions that are available on a pin.

There are two differences between timer/counter type 4 and type 5. Timer/counter 4 has four CC channels, and timer/counter 5 has two CC channels. Both timer/counter 4 and 5 can be set in 8-bit mode, allowing the application to double the number of compare and capture channels that then get 8-bit resolution.

Some timer/counters have extensions that enable more specialized waveform generation. The waveform extension (WeX) is intended for motor control, ballast, LED, H-bridge, power converters, and other types of power control applications. It enables more customized waveform output distribution, and low- and high-side channel output with optional dead-time insertion. It can also generate a synchronized bit pattern across the port pins. The high-resolution (hi-res) extension can increase the waveform resolution by four or eight times by using an internal clock source four times faster than the peripheral clock. The fault extension (FAULT) enables fault protection for safe and deterministic handling, disabling and/or shut down of external drivers.

A block diagram of the 16-bit timer/counter with extensions and closely related peripheral modules (in grey) is shown in Figure 17-1.

Figure 17-1. 16-bit Timer/counter and Closely Related Peripherals



PORTC has one timer/counter 4 and one timer/counter 5. PORTD has one timer/counter 5. Notation of these are TCC4 (timer/counter C4), TCC5, and TCD5, respectively.

19. Hi-Res – High Resolution Extension

19.1 Features

- Increases waveform generator resolution up to 8x (three bits)
- Supports frequency, single-slope PWM, and dual-slope PWM generation
- Supports the WeX when this is used for the same timer/counter

19.2 Overview

The high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the WeX if this is used for the same timer/counter.

The hi-res extension uses the peripheral 4x clock (ClkPER4). The system clock prescalers must be configured so the peripheral 4x clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

There is one hi-res extension that can be enabled for timer/counters pair on PORTC. The notation of this is HIRESC.

22. TWI – Two-Wire Interface

22.1 Features

- One two-wire interface
  - Phillips I^2C compatible
  - System Management Bus (SMBus) compatible
- Bus master and slave operation supported
  - Slave operation
  - Single bus master operation
  - Bus master in multi-master bus environment
  - Multi-master arbitration
  - Bridge mode with independent and simultaneous master and slave operation
- Flexible slave address match functions
  - 7-bit and general call address recognition in hardware
  - 10-bit addressing supported
  - Address mask register for dual address match or address range masking
  - Optional software address recognition for unlimited number of addresses
- Slave can operate in all sleep modes, including power-down
- Slave address match can wake device from all sleep modes
- 100kHz, 400kHz, and 1MHz bus frequency support
- Slew-rate limited output drivers
- Input filter for bus noise and spike suppression
- Support arbitration between start/repeated start and data bit (SMBus)
- Slave arbitration allows support for address resolve protocol (ARP) (SMBus)
- Supports SMBUS Layer 1 timeouts
- Configurable timeout values
- Independent timeout counters in master and slave (Bridge mode support)

22.2 Overview

The two-wire interface (TWI) is a bidirectional, two-wire communication interface. It is I^2C and System Management Bus (SMBus) compatible. The only external hardware needed to implement the bus is one pull-up resistor on each bus line.

A device connected to the bus must act as a master or a slave. One bus can have many slaves and one or several masters that can take control of the bus.

The TWI module supports master and slave functionality. The master and slave functionality are separated from each other, and can be enabled and operate simultaneously and separately. The master module supports multi-master bus operation and arbitration. It contains the baud rate generator. Quick command and smart mode can be enabled to auto-trigger operations and reduce software complexity. The master can support 100kHz, 400kHz, and 1MHz bus frequency.

The slave module implements 7-bit address match and general address call recognition in hardware. 10-bit addressing is also supported. A dedicated address mask register can act as a second address match register or as a register for address range masking. The slave continues to operate in all sleep modes, including power-down mode. This enables the slave to wake up the device from all sleep modes on TWI address match. It is possible to disable the address matching to let this be handled in software instead. By using the bridge option, the slave can be mapped to different pin locations. The master and slave can support 100kHz, 400kHz, and 1MHz bus frequency.

The TWI module will detect START and STOP conditions, bus collisions, and bus errors. Arbitration lost, errors, collision, and clock hold on the bus are also detected and indicated in separate status flags available in both master and slave modes.

25. IRCOM – IR Communication Module

25.1 Features

- Pulse modulation/demodulation for infrared communication
- IrDA compatible for baud rates up to 115.2Kbps
- Selectable pulse modulation scheme
  - 3/16 of the baud rate period
  - Fixed pulse period, 8-bit programmable
  - Pulse modulation disabled
- Built-in filtering
- Can be connected to and used by any USART

25.2 Overview

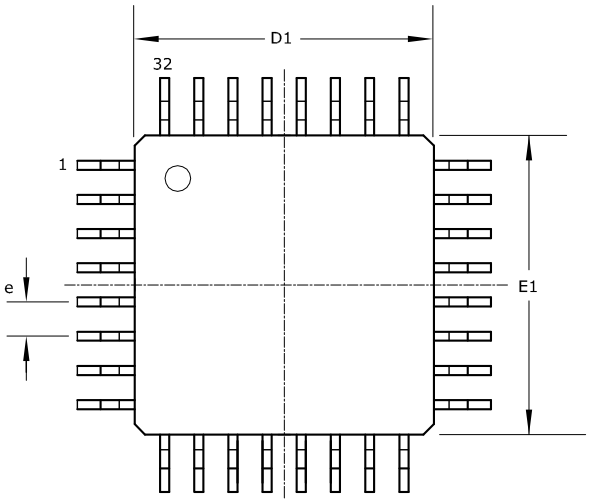
Atmel AVR XMEGA devices contain an infrared communication module (IRCOM) that is IrDA compatible for baud rates up to 115.2Kbps. It can be connected to any USART to enable infrared pulse encoding/decoding for that USART.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2[1][2]
LD	Rd, X	Load Indirect	Rd ← (X)	None	1[1][2]
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X) X ← X + 1	None	1[1][2]
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, ← X - 1 Rd ← (X) ← (X)	None	2[1][2]
LD	Rd, Y	Load Indirect	Rd ← (Y) ← (Y)	None	1[1][2]
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y) Y ← Y + 1	None	1[1][2]
LD	Rd, -Y	Load Indirect and Pre-Decrement	Y ← Y - 1 Rd ← (Y)	None	2[1][2]
LDD	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2[1][2]
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	1[1][2]
LD	Rd, Z+	Load Indirect and Post-Increment	Rd ← (Z), Z ← Z+1	None	1[1][2]
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z ← Z - 1, Rd ← (Z)	None	2[1][2]
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2[1][2]
STS	k, Rr	Store Direct to Data Space	(k) ← Rd	None	2[1]
ST	X, Rr	Store Indirect	(X) ← Rr	None	1[1]
ST	X+, Rr	Store Indirect and Post-Increment	(X) ← Rr, X ← X + 1	None	1[1]
ST	-X, Rr	Store Indirect and Pre-Decrement	X ← X - 1, (X) ← Rr	None	2[1]
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	1[1]
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) ← Rr, Y ← Y + 1	None	1[1]
ST	-Y, Rr	Store Indirect and Pre-Decrement	Y ← Y - 1, (Y) ← Rr	None	2[1]
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2[1]
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	1[1]
ST	Z+, Rr	Store Indirect and Post-Increment	(Z) ← Rr Z ← Z + 1	None	1[1]
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z ← Z - 1	None	2[1]
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2[1]
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	Rd ← (Z), Z ← Z + 1	None	3
ELPM		Extended Load Program Memory	R0 ← (RAMPZ:Z)	None	3
ELPM	Rd, Z	Extended Load Program Memory	Rd ← (RAMPZ:Z)	None	3
ELPM	Rd, Z+	Extended Load Program Memory and Post-Increment	Rd ← (RAMPZ:Z), Z ← Z + 1	None	3
SPM		Store Program Memory	(RAMPZ:Z) ← R1:R0	None	-

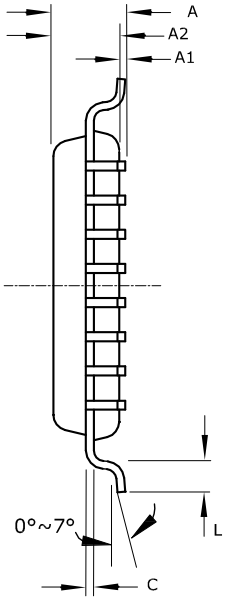
35. Packaging Information

35.1 32A

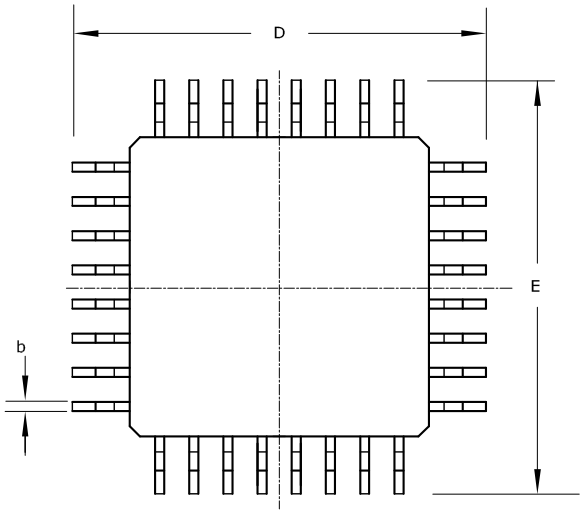
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	1.00	1.05	
D/E	8.75	9.00	9.25	
D1/E1	6.90	7.00	7.10	2
C	0.09	-----	0.20	
L	0.45	-----	0.75	
b	0.30	-----	0.45	
e	0.80 TYP			
n	32			

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

02/29/2012

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	MA, 32 Lds - 0.80mm Pitch, 7x7x1.00mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AUT	MA	C

36.13 Clock and Oscillator Characteristics

36.13.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 36-20. 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 25°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

36.13.2 Calibrated 8MHz Internal Oscillator Characteristics

Table 36-21. 8MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range		4.4		9.4	MHz
	Factory calibrated frequency			8		
	Factory calibration accuracy	T = 25°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

36.13.3 Calibrated and Tunable 32MHz Internal Oscillator Characteristics

Table 36-22. 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30		55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 25°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.23		

36.13.4 32 kHz Internal ULP Oscillator Characteristics

Table 36-23. 32 kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Output frequency			32		kHz
	Accuracy		-30		30	%

Figure 37-13.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 8MHz internal oscillator prescaled to 2MHz

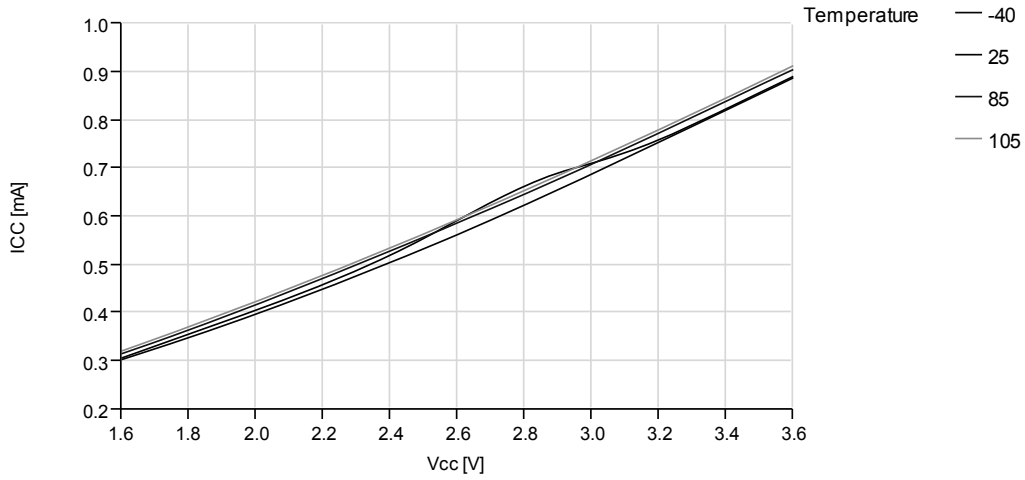
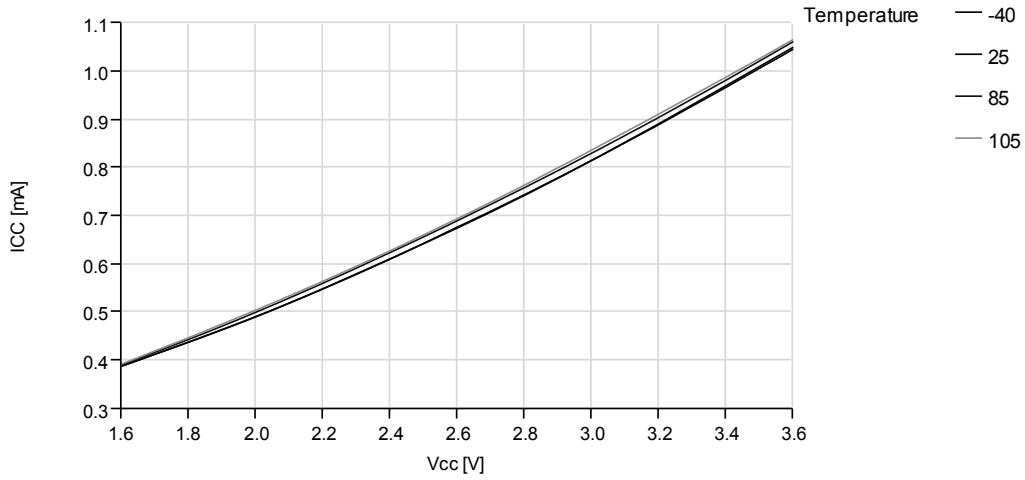


Figure 37-14.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 8MHz internal oscillator



37.1.3 Power-down Mode Supply Current

Figure 37-17.Power-down Mode Supply Current vs. Temperature

All functions disabled

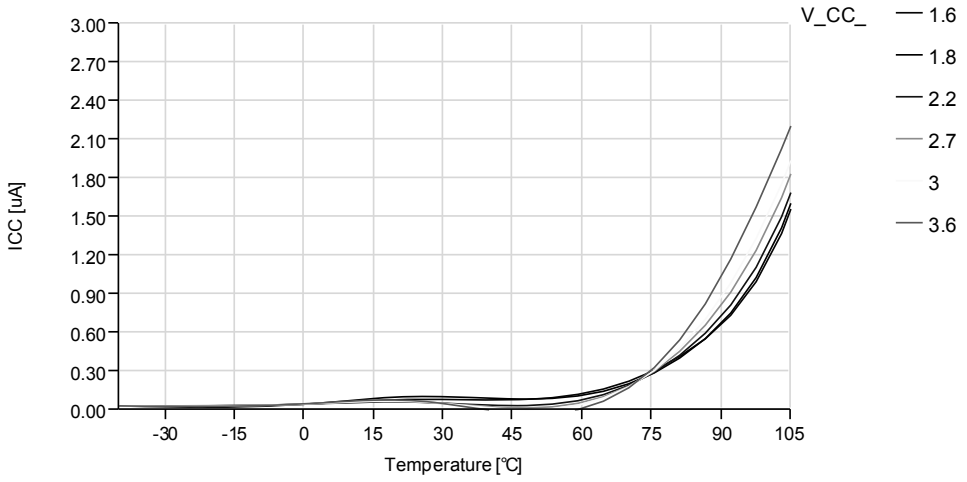


Figure 37-18.Power-down Mode supply Current vs. V_{CC}

All functions disabled

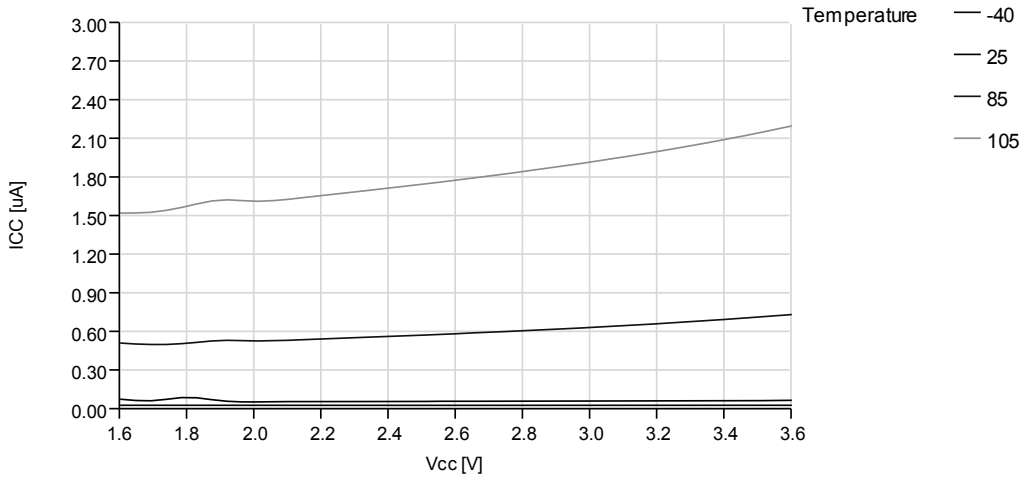
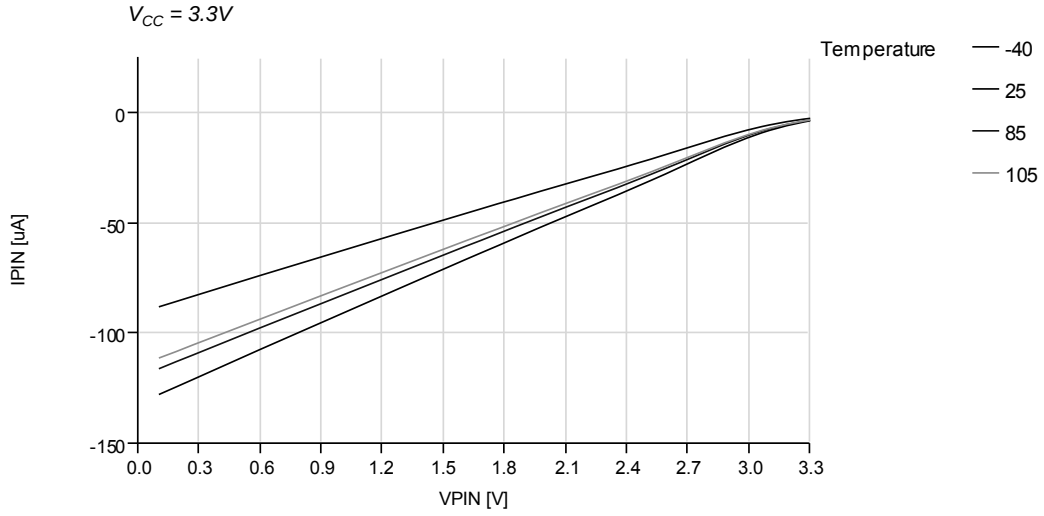


Figure 37-25.I/O Pin Pull-up Resistor Current vs. Input Voltage



37.2.2 Output Voltage vs. Sink/Source Current

Figure 37-26.I/O Pin Output Voltage vs. Source Current

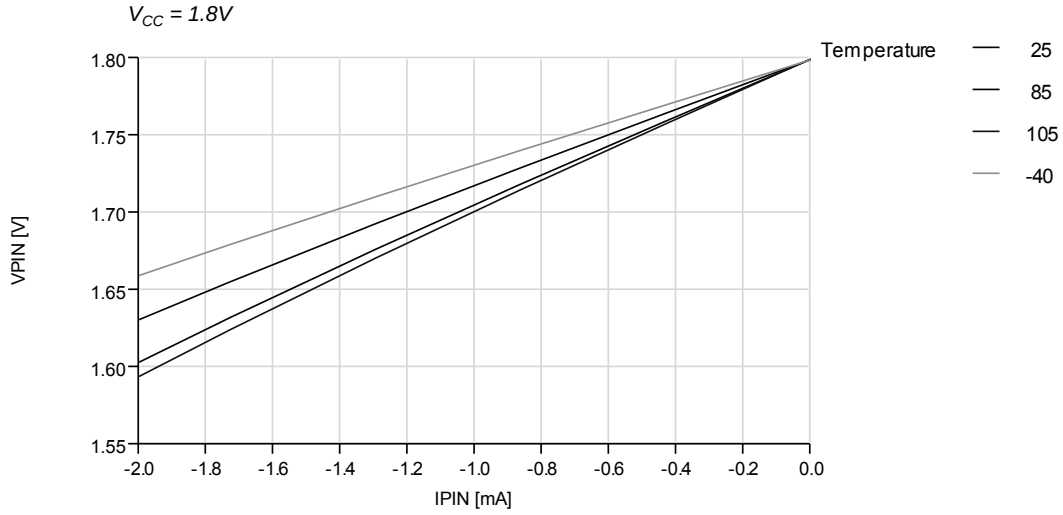
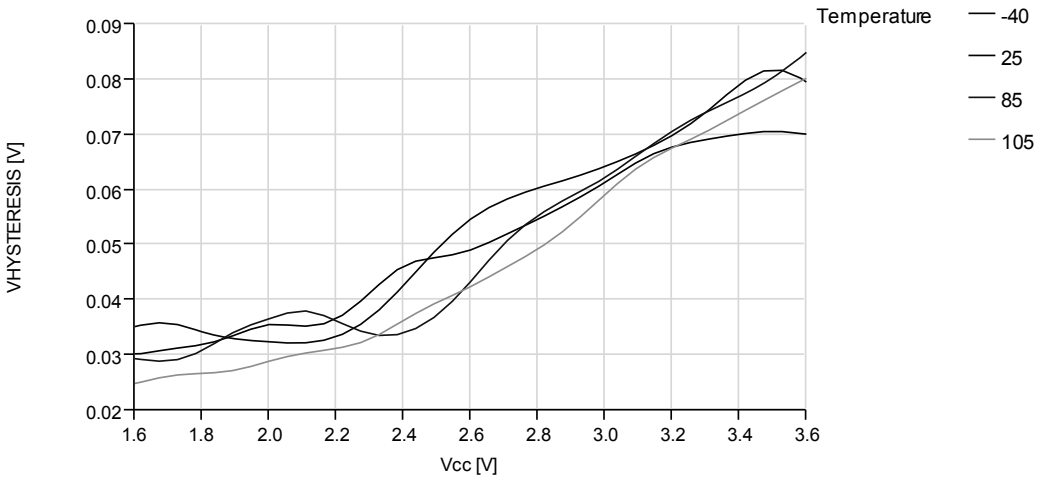


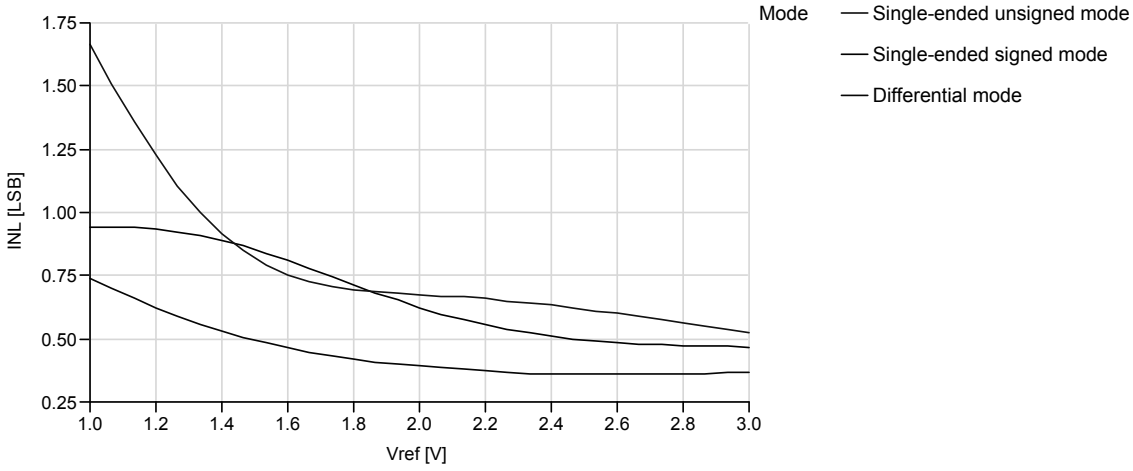
Figure 37-37.I/O Pin Input Hysteresis vs. V_{CC}



37.3 ADC Characteristics

Figure 37-38.ADC INL vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference



37.4 DAC Characteristics

Figure 37-47.DAC INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V

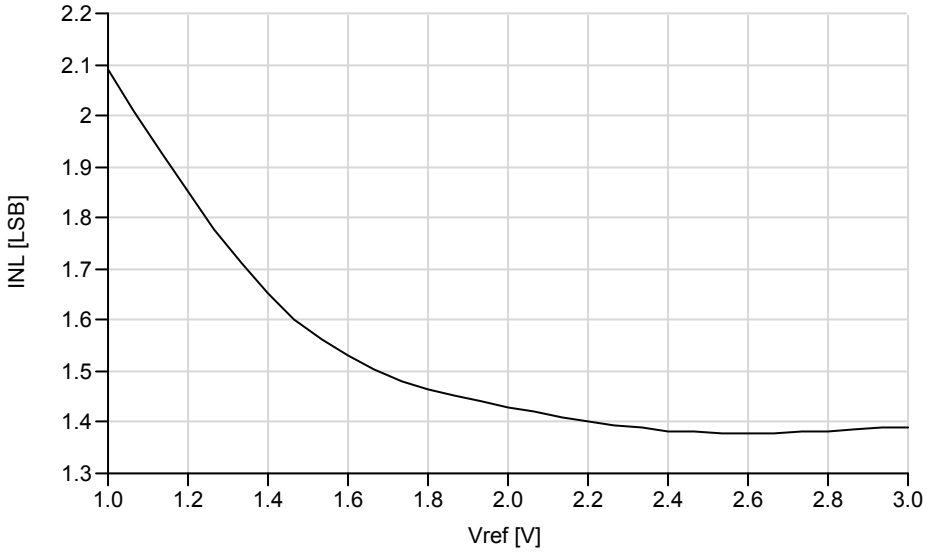


Figure 37-48.DNL Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V

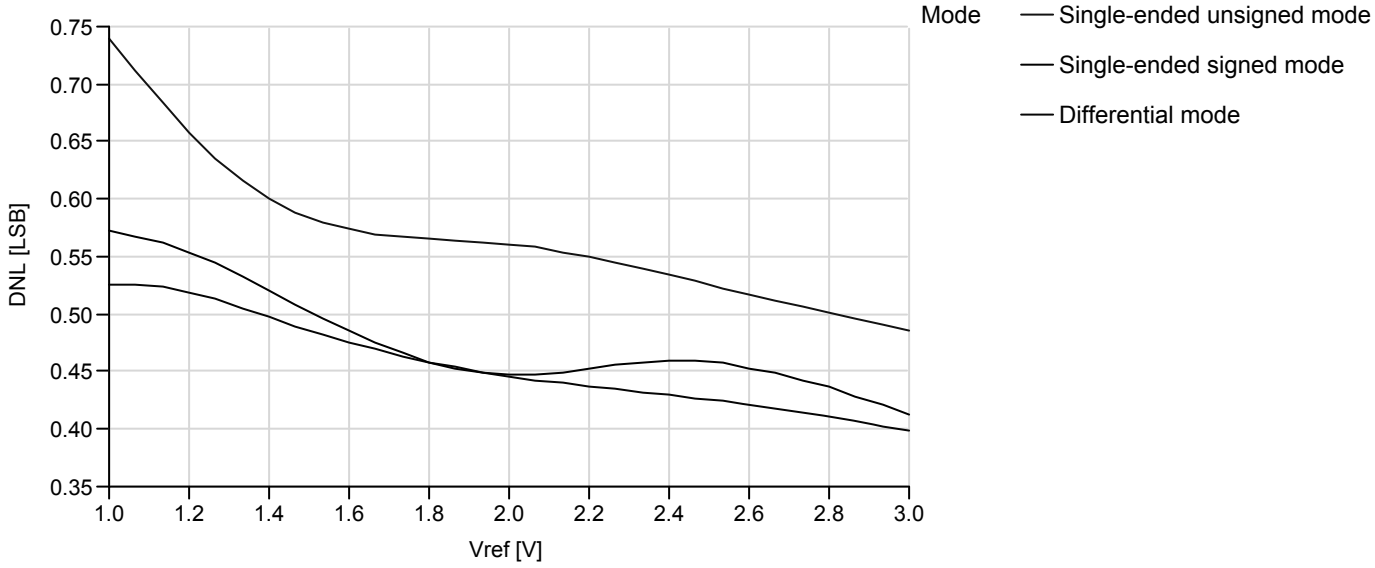


Figure 37-69.Power-on Reset Current Consumption vs. V_{CC}

BOD level = 3.0V, enabled in sampled mode

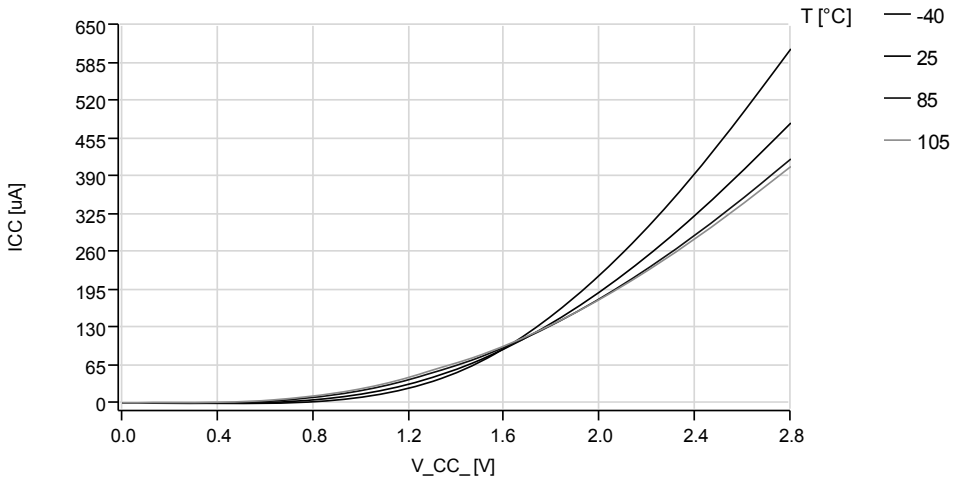


Figure 37-76. 8MHz Internal Oscillator CAL Calibration Step Size

V_{CC} = 3.0V

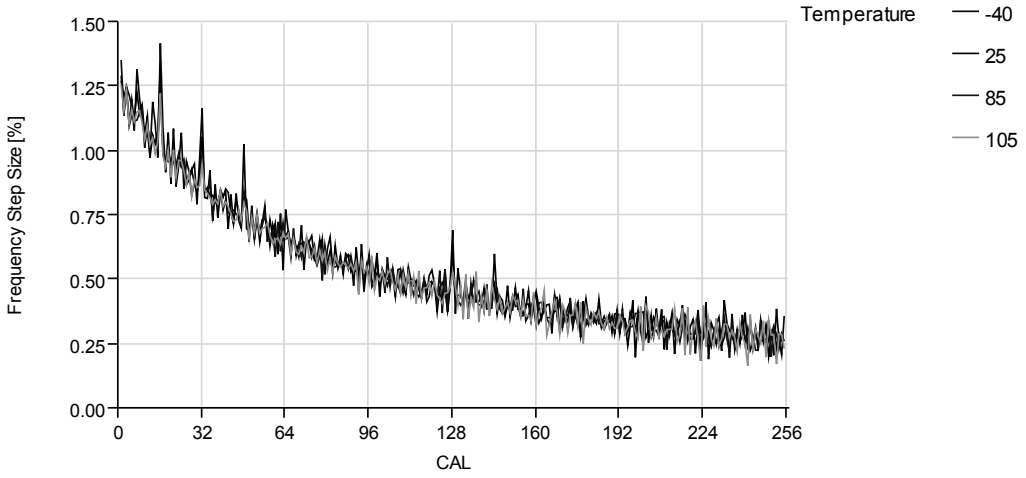


Figure 37-77. 8MHz Internal Oscillator Frequency vs. Calibration

V_{CC} = 3.0V, normal mode

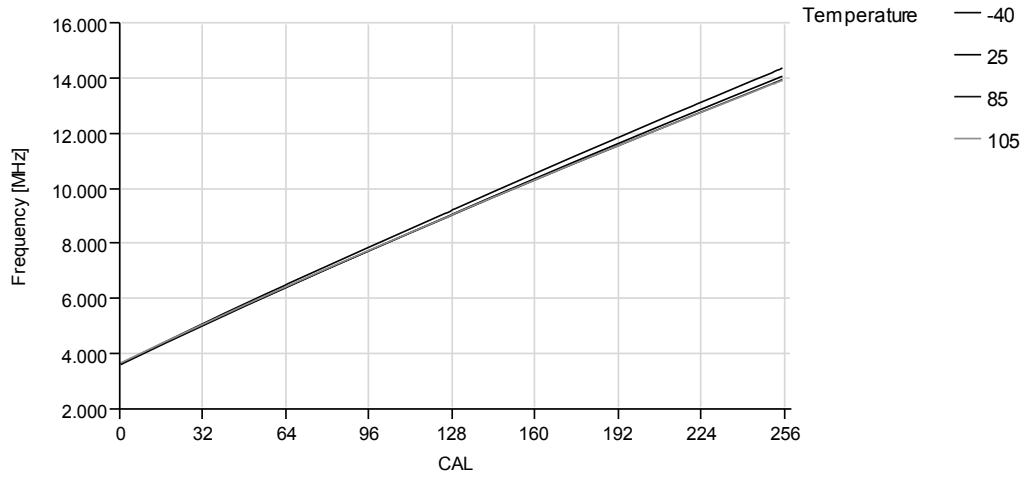


Figure 37-80. 32MHz Internal Oscillator CALA Calibration Step Size

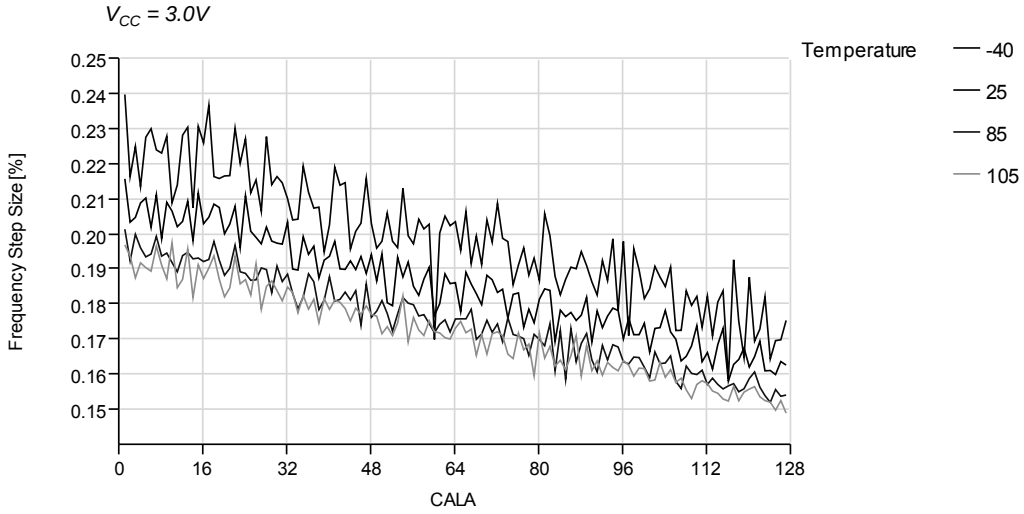
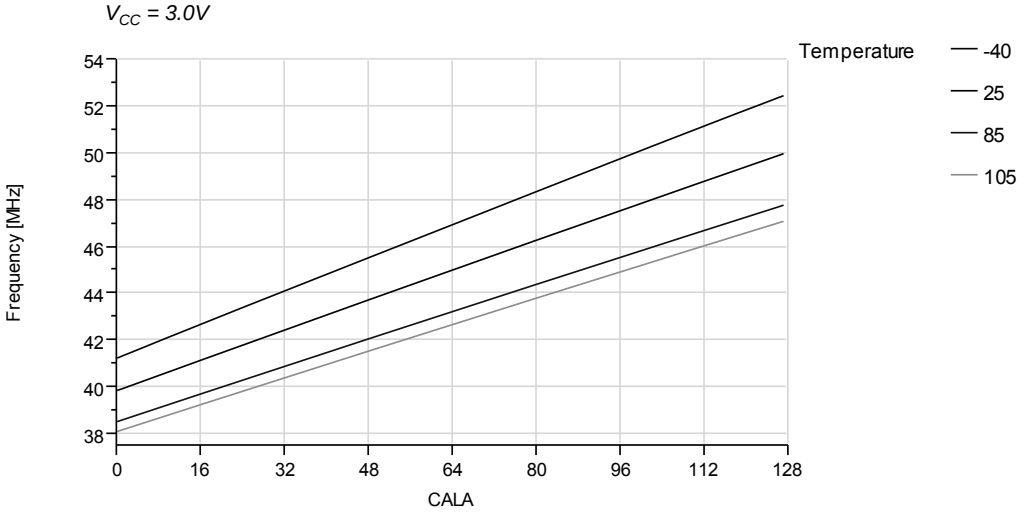


Figure 37-81. 32MHz Internal Oscillator Frequency vs. CALA Calibration Value



Issue: TWI SM bus level one Master or slave remembering data

If a write is made to Data register, prior to Address register, the TWI design sends the data as soon as the write to Address register is made. But the send data will be always 0x00.

Workaround:

Since single interrupt line is shared by both timeout interrupt and other TWI interrupt sources, there is a possibility in software that data register will be written after timeout is detected but before timeout interrupt routine is executed. To avoid this, in software, before writing data register, always ensure that timeout status flag is not set.

Issue: Temperature sensor not calibrated

Temperature sensor factory calibration is not implemented on devices before date code 1324.

Workaround:

None.

Issue: Automatic port override on PORT C

When Waveform generation is enabled on PORT C Timers, Automatic port override of peripherals other than Tc may not work even though the pin is not used as waveform output pin.

Workaround:

No workaround.

Issue: Sext timer is not implemented in slave mode

In slave mode, only Ttout timer is implemented. Sext timer is needed in slave mode to release the SCL line and to allow the master to send a STOP condition. If only master implements Sext timer, slave continues to stretch the SCL line (up to the Ttout timeout in the worse case). Sext = Slave cumulative timeout.

Workaround:

No workaround.

39.7 8153E – 06/2013

1.	Errata “Rev. B” : Updated date code from 1318 to 1324 in “Temperature sensor not calibrated” on page 137.

39.8 8153D – 06/2013

1.	Analog Comparator Characteristics: Updated minimum and maximum values of Input Voltage Range, Table 36-14 on page 80.

39.9 8153C – 05/2013

1.	Electrical Characteristics, Table on page 73: Updated typical value from 7mA to 6mA for Active Current Consumption, 32MHz, V_{CC}=3.0V.
2.	Errata “Rev. A” and “Rev. B” : Added DAC errata: AREF on PORT C0.

39.10 8153B – 04/2013

1.	“Rev. B” on page 136: Removed the “EDMA: Channel transfer never stops when double buffering is enabled on sub-sequent channels” errata.

39.11 8153A – 04/2013

1.	Initial revision.