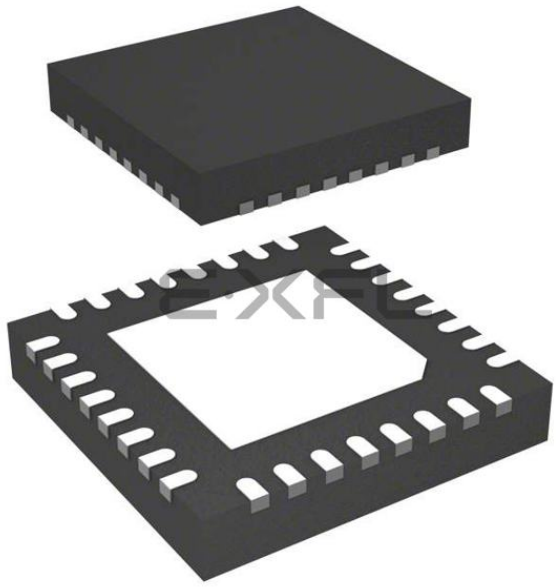

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32e5-m4nr

9. EDMA – Enhanced DMA Controller

9.1 Features

- The EDMA Controller allows data transfers with minimal CPU intervention
  - from data memory to data memory
  - from data memory to peripheral
  - from peripheral to data memory
  - from peripheral to peripheral
- Four peripheral EDMA channels with separate:
  - transfer triggers
  - interrupt vectors
  - addressing modes
  - data matching
- Two peripheral channels can be combined to one standard channel with separate:
  - transfer triggers
  - interrupt vectors
  - addressing modes
  - data search
- Programmable channel priority
- From 1byte to 128KB of data in a single transaction
  - Up to 64K block transfer with repeat
  - 1 or 2 bytes burst transfers
- Multiple addressing modes
  - Static
  - Increment
- Optional reload of source and destination address at the end of each
  - Burst
  - Block
  - Transaction
- Optional Interrupt on end of transaction
- Optional connection to CRC Generator module for CRC on EDMA data

9.2 Overview

The four-channel enhanced direct memory access (EDMA) controller can transfer data between memories and peripherals, and thus offload these tasks from the CPU. It enables high data transfer rates with minimum CPU intervention, and frees up CPU time. The four EDMA channels enable up to four independent and parallel transfers.

The EDMA controller can move data between SRAM and peripherals, between SRAM locations and directly between peripheral registers. With access to all peripherals, the EDMA controller can handle automatic transfer of data to/from communication modules. The EDMA controller can also read from EEPROM memory.

Data transfers are done in continuous bursts of 1 or 2 bytes. They build block transfers of configurable size from 1 byte to 64KB. Repeat option can be used to repeat once each block transfer for single transactions up to 128KB. Source and destination addressing can be static or incremental. Automatic reload of source and/or destination addresses can be done after each burst or block transfer, or when a transaction is complete. Application software, peripherals, and events can trigger EDMA transfers.

The four EDMA channels have individual configuration and control settings. This includes source, destination, transfer triggers, and transaction sizes. They have individual interrupt settings. Interrupt requests can be generated when a transaction is complete or when the EDMA controller detects an error on an EDMA channel.

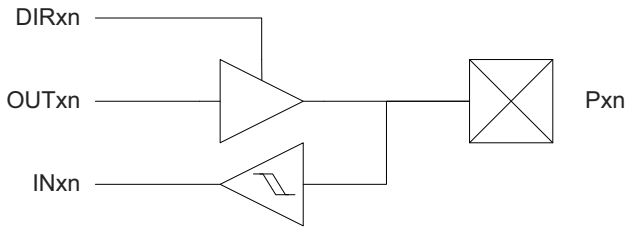
To enable flexibility in transfers, channels can be interlinked so that the second takes over the transfer when the first is finished.

16.3 Output Driver

All port pins (Pxn) have programmable output configuration. The port pins also have configurable slew rate limitation to reduce electromagnetic emission.

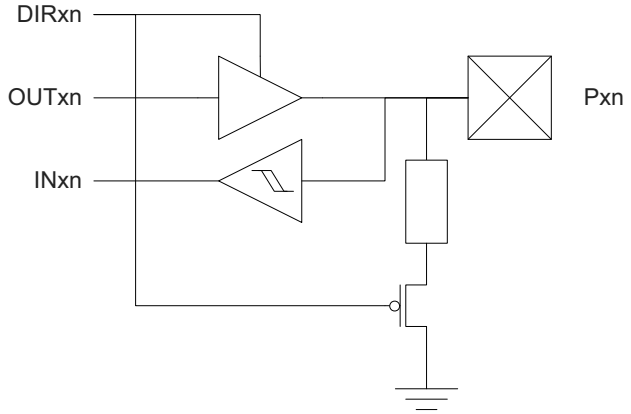
16.3.1 Push-pull

Figure 16-1. I/O Configuration - Totem-pole



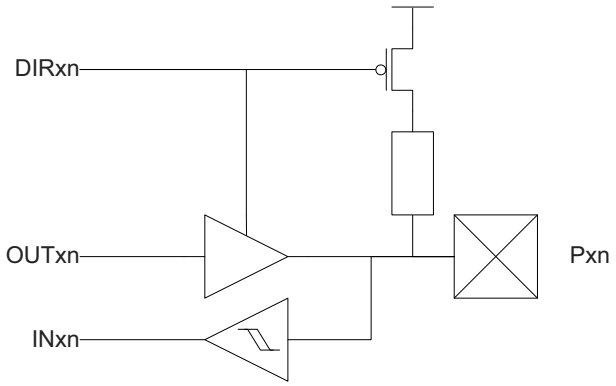
16.3.2 Pull-down

Figure 16-2. I/O Configuration - Totem-pole with Pull-down (on input)



16.3.3 Pull-up

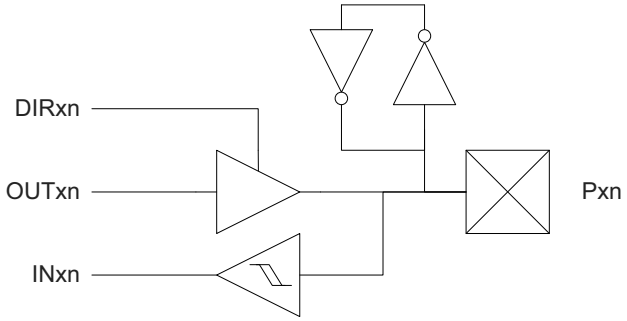
Figure 16-3. I/O Configuration - Totem-pole with Pull-up (on input)



16.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 16-4. I/O Configuration - Totem-pole with Bus-keeper



16.3.5 Others

Figure 16-5. Output Configuration - Wired-OR with Optional Pull-down

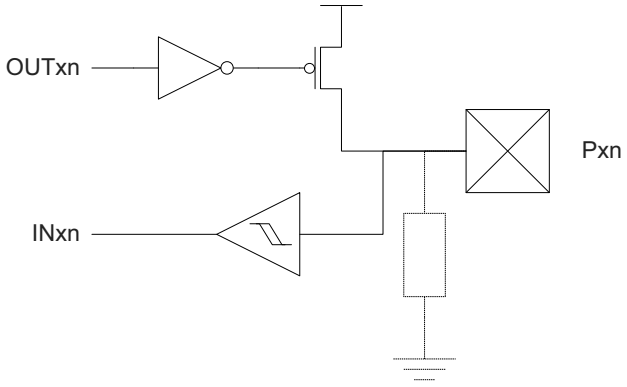
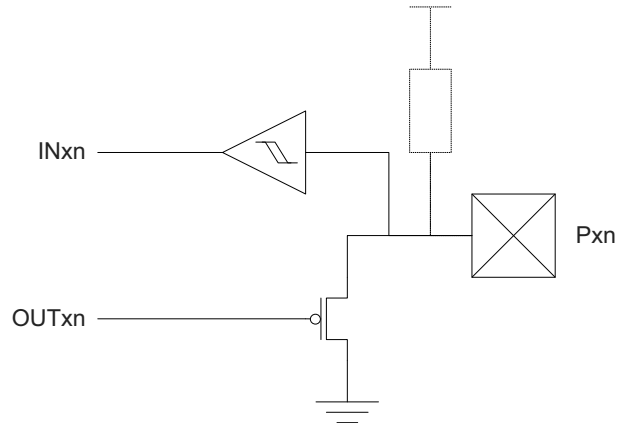


Figure 16-6. I/O Configuration - Wired-AND with Optional Pull-up



It is possible to disable the TWI drivers in the device, and enable a four-wire digital interface for connecting to an external TWI bus driver. This can be used for applications where the device operates from a different V_{CC} voltage than used by the TWI bus.

It is also possible to enable the bridge mode. In this mode, the slave I/O pins are selected from an alternative port, enabling independent and simultaneous master and slave operation.

PORTC has one TWI. Notation of this peripheral is TWIC. Alternative TWI Slave location in bridge mode is on PORTD.

23. SPI – Serial Peripheral Interface

23.1 Features

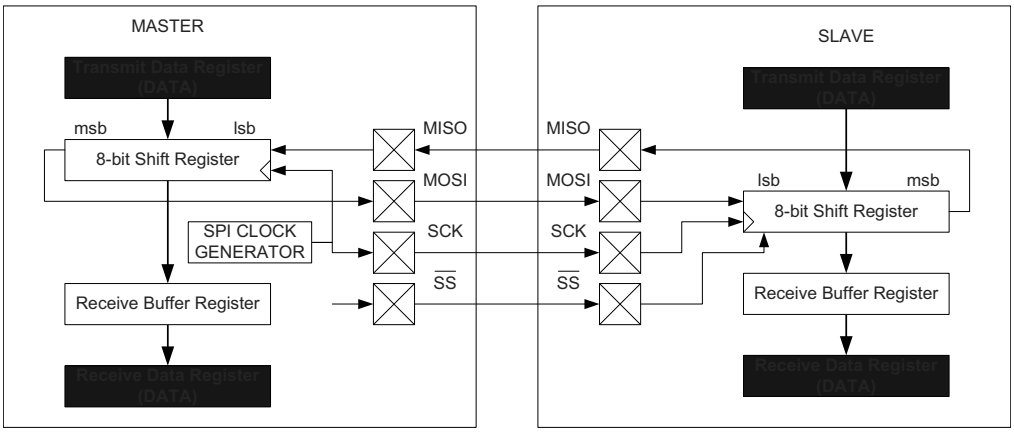
- One SPI peripheral
- Full-duplex, three-wire synchronous data transfer
- Master or slave operation
- lsb first or msb first data transfer
- Eight programmable bit rates
- Interrupt flag at the end of transmission
- Write collision flag to indicate data collision
- Wake up from idle sleep mode
- Double speed master mode

23.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed, full duplex, synchronous data transfer interface using three or four pins. It allows fast communication between an AVR XMEGA device and peripheral devices or between several microcontrollers.

A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions. The interconnection between master and slave devices with SPI is shown in Figure 23-1. The system consists of two shift registers and a clock generator. The SPI master initiates the communication by pulling the slave select (SS) signal low for the desired slave. Master and slave prepare the data to be sent in their respective shift registers, and the master generates the required clock pulses on the SCK line to interchange data. Data are always shifted from master to slave on the master output, slave input (MOSI) line, and from slave to master on the master input, slave output (MISO) line. After each data packet, the master can synchronize the slave by pulling the $\overline{SS}$ line high.

Figure 23-1. SPI Master-slave Interconnection



By default, the SPI module is single buffered and transmit direction and double buffered in the receive direction. A byte written to the transmit data register will be copied to the shift register when a full character has been received. When receiving data, a received character must be read from the transmit data register before the third character has been completely shifted in to avoid losing data. Optionally, buffer modes can be enabled. When used, one buffer is available for transmitter and a double buffer for reception.

PORTC has one SPI. Notation of this is SPIC.

26. XCL – XMEGA Custom Logic Module

26.1 Features

- Two independent 8-bit timer/counter with:
  - Period and compare channel for each timer/counter
  - Input Capture for each timer
  - Serial peripheral data length control for each timer
  - Timeout support for each timer
  - Timer underflow interrupt/event
  - Compare match or input capture interrupt/event for each timer
- One 16-bit timer/counter by cascading two 8-bit timer/counters with:
  - Period and compare channel
  - Input capture
  - Timeout support
  - Timer underflow interrupt/event
  - Compare match or input capture interrupt/event
- Programmable lookup table supporting multiple configurations:
  - Two 2-input units
  - One 3-input unit
  - RS configuration
  - Duplicate input with selectable delay on one input or output
  - Connection to external I/O pins, event system or one selectable USART
- Combinatorial Logic Functions using programmable truth table:
  - AND, NAND, OR, NOR, XOR, XNOR, NOT, MUX
- Sequential Logic Functions:
  - D-Flip-Flop, D Latch, RS Latch
- Input sources:
  - From external pins or the event system
  - One input source includes selectable delay or synchronizing option
  - Can be shared with selectable USART pin locations
- Outputs:
  - Available on external pins or event system
  - Includes selectable delay or synchronizing option
  - Can override selectable USART pin locations
- Operates in active mode and all sleep modes

26.2 Overview

The XMEGA Custom Logic module (XCL) consists of two sub-units, each including 8-bit timer/counter with flexible settings, peripheral counter working with one software selectable USART module, delay elements, glue logic with programmable truth table and a global logic interconnect array.

The timer/counter configuration allows for two 8-bits timer/counters. Each timer/counter supports normal, compare and input capture operation, with common flexible clock selections and event channels for each timer. By cascading the two 8-bit timer/counters, the XCL can be used as a 16-bit timer/counter.

The peripheral counter (PEC) configuration, the XCL is connected to one software selectable USART. This USART controls the counter operation, and the PEC can optionally control the data length within the USART frame.

The glue logic configuration, the XCL implements two programmable lookup tables (LUTs). Each defines the truth table corresponding to the logical condition between two inputs. Any combinatorial function logic is possible. The LUT inputs can be connected to I/O pins or event system channels. If the LUT is connected to the USART0 pin locations, the data lines (TXD/RXD) data encoding/decoding will be possible. Connecting together the LUT units, RS Latch, or any combinatorial logic between two operands or three inputs can be enabled.

32.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.

Table 32-1. PORT A – Alternate Functions

PORT A	Pin#	ADCA POS/ GAINPOS	ADCA NEG/ GAINNEG	DACA	ACA POS	ACA NEG	ACA OUT	REFA
PA0	6	ADC 0	ADC 0		AC0	AC0		AREF
PA1	5	ADC 1	ADC 1		AC1	AC1		
PA2	4	ADC 2	ADC 2	DAC0	AC2			
PA3	3	ADC 3	ADC 3	DAC1	AC3	AC3		
PA4	2	ADC 4	ADC 4		AC4			
PA5	31	ADC 5	ADC 5		AC5	AC5		
PA6	30	ADC 6	ADC 6		AC6		AC1OUT	
PA7	29	ADC 7	ADC 7			AC7	AC0OUT	

Table 32-2. PORT C – Alternate Functions

PORT C	Pin #	TCC4	WEXC	TCC5	USARTC0	SPIC	TWI	XCL (LUT)	EXTCLK	AC OUT
PC0	16	OC4A	OC4ALS				SDA	IN1/OUT0		
PC1	15	OC4B	OC4AHS		XCK0		SCL	IN2		
PC2	14	OC4C	OC4BLS		RXD0			IN0		
PC3	13	OC4D	OC4BHS		TXD0			IN3		
PC4	12	OC4A	OC4CLS	OC5A		$\overline{SS}$		IN1/OUT0	EXTCLK	
PC5	11	OC4B	OC4CHS	OC5B	XCK0	SCK		IN2		
PC6	10	OC4C	OC4DLS		RXD0	MISO		IN0		AC1OUT
PC7	9	OC4D	OC4DHS		TXD0	MOSI		IN3		AC0OUT

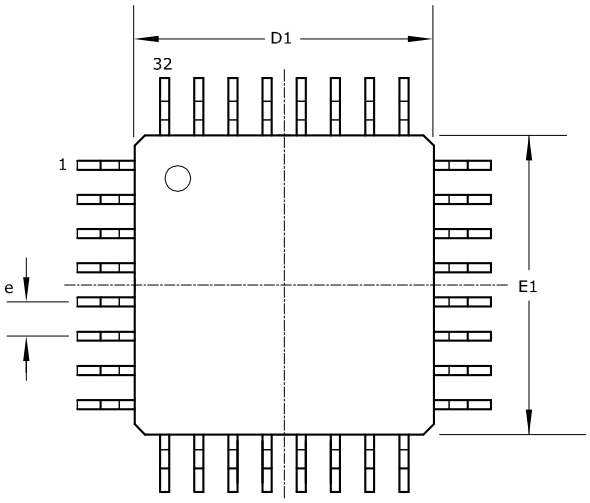
Table 32-3. Debug – Program and Debug Functions

DEBUG	Pin #	PROG
RESET	8	PDI CLOCK
PDI	7	PDI DATA

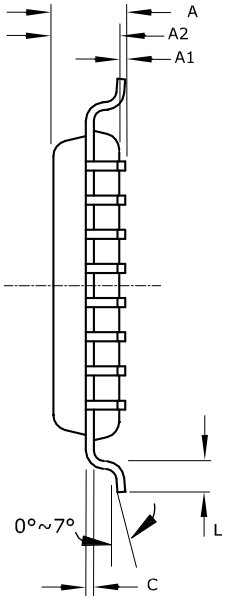
35. Packaging Information

35.1 32A

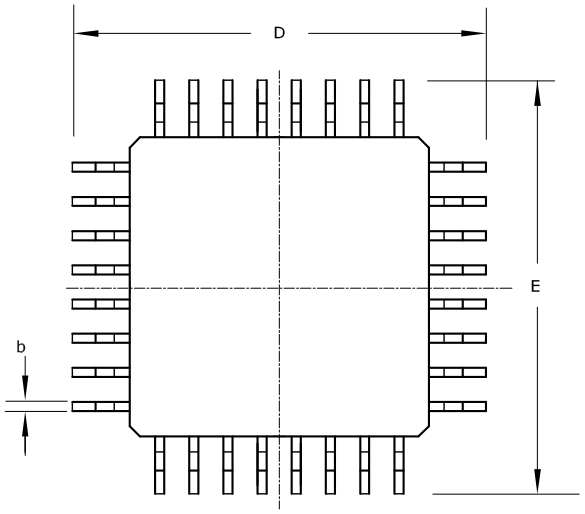
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	1.00	1.05	
D/E	8.75	9.00	9.25	
D1/E1	6.90	7.00	7.10	2
C	0.09	-----	0.20	
L	0.45	-----	0.75	
b	0.30	-----	0.45	
e	0.80 TYP			
n	32			

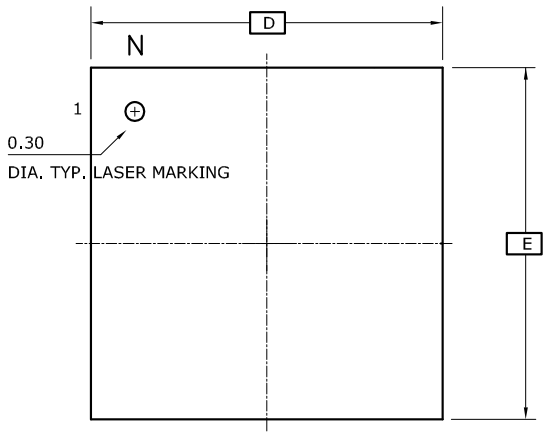
Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

02/29/2012

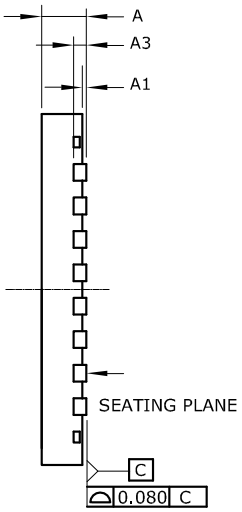
Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	MA, 32 Lds - 0.80mm Pitch, 7x7x1.00mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AUT	MA	C

35.2 32Z

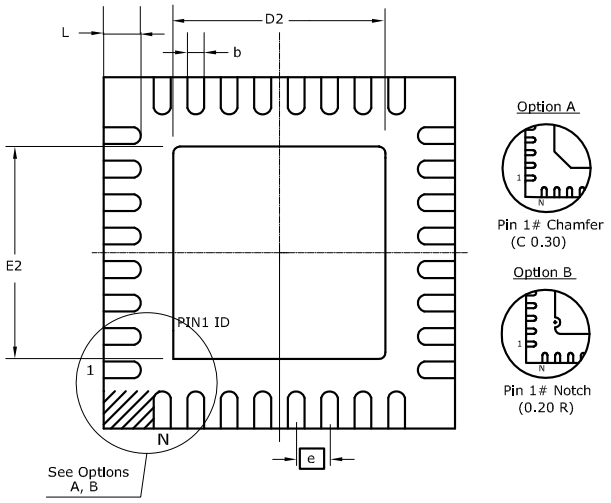
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
A1	0.00	----	0.05	
A3		0.20 REF		
D/E		5.00 BSC		
D2/E2	3.00	3.10	3.20	
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	2
e		0.50 BSC		
n		32		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VHHD-2, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

01/31/2012

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	PN, 32 Leads , 0.50mm pitch, 5 x 5 mm Very Thin quad Flat No Lead Package (VQFN) Sawn	ZMF	PN	I

36. Electrical Characteristics

All typical values are measured at T = 25°C unless other temperature condition is given. All minimum and maximum values are valid across operating temperature and voltage unless other conditions are given.

36.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage	-0.3		4	V
I_{VCC}	Current into a V_{CC} pin			200	mA
I_{GND}	Current out of a Gnd pin			200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}	-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current	-25		25	mA
T_A	Storage temperature	-65		150	°C
T_j	Junction temperature			150	

36.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-1 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 36-1. General Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage	1.6		3.6	V
AV_{CC}	Analog supply voltage	1.6		3.6	
T_A	Temperature range	-40		85	°C
T_j	Junction temperature	-40		105	

Table 36-2. Operating Voltage and Frequency

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 36-1 the frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Table 36-4. Current Consumption for Modules and Peripherals

Symbol	Parameter	Condition[1]		Min.	Typ.	Max.	Units
I_{CC}	Internal ULP oscillator				100		nA
	32.768kHz int. oscillator				27		μA
	8MHz int. oscillator	Normal power mode			65		
		Low power mode			45		
	32MHz int. oscillator				275		
		DFLL enabled with 32.768kHz int. osc. as reference			400		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			230		
	Watchdog timer				0.3		
	BOD	Continuous mode			245		
		Sampled mode			0.4		
	Internal 1.0V reference				200		
	Internal temperature sensor				100		
	ADC	16ksps V_{REF} = Ext. ref.			1.5		mA
			CURRLIMIT = LOW		1.4		
			CURRLIMIT = MEDIUM		1.3		
			CURRLIMIT = HIGH		1.2		
		75ksps, V_{REF} = Ext. ref.	CURRLIMIT = LOW		1.7		
		300ksps, V_{REF} = Ext. ref.			3.1		
	DAC	250ksps V_{REF} = Ext. ref. No load	Normal mode		1.9		
			Low Power mode		1.1		
	AC				200		μA
	EDMA				200		
	Timer/counter				25		
	USART	Rx and Tx enabled, 9600 BAUD			8		
	XCL	16-bit timer/counter			6		
	Flash memory and EEPROM programming				4		mA

Notes: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

Table 36-13. Accuracy Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
RES	Input Resolution					12	Bits
INL (1)	Integral non-linearity	V_{REF}= Ext 1.0V	V_{CC} = 1.6V		±2.0	±3	lsb
			V_{CC} = 3.6V		±1.5	±2.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±2.0	±4	
			V_{CC} = 3.6V		±1.5	±4	
		V_{REF}=INT1V	V_{CC} = 1.6V		±5.0		
			V_{CC} = 3.6V		±5.0		
DNL (1)	Differential non-linearity	V_{REF}=Ext 1.0V	V_{CC} = 1.6V		±1.5	3	
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±1.0	3.5	
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=INT1V	V_{CC} = 1.6V		±4.5		
			V_{CC} = 3.6V		±4.5		
	Gain error	After calibration			<4		
	Gain calibration step size				4		
	Gain calibration drift	V_{REF}= Ext 1.0V			<0.2		mV/K
	Offset error	After calibration			<1		lsb
	Offset calibration step size				1		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

36.8 Analog Comparator Characteristics

Table 36-14. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			10		mV
I_{lk}	Input leakage current			<10	50	nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			50		µs
V_{hys1}	Hysteresis, none	V_{CC} = 1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	V_{CC} = 1.6V - 3.6V		12		
V_{hys3}	Hysteresis, large	V_{CC} = 1.6V - 3.6V		28		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C		22	30	ns
		V_{CC} = 1.6V - 3.6V		21	40	

Table 36-19. Programming Time

Parameter	Condition	Min.	Typ.[1]	Max.	Units
Chip Erase	32KB Flash, EEPROM[2]		50		ms
	16KB Flash, EEPROM[2]		45		
	8KB Flash, EEPROM[2]		42		
Flash	Page erase		4		
	Page write		4		
	Atomic page erase and write		8		
EEPROM	Page erase		4		
	Page write		4		
	Atomic page erase and write		8		

Notes:
1. Programming is timed from the 2MHz output of 8MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

Figure 37-13.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 8MHz internal oscillator prescaled to 2MHz

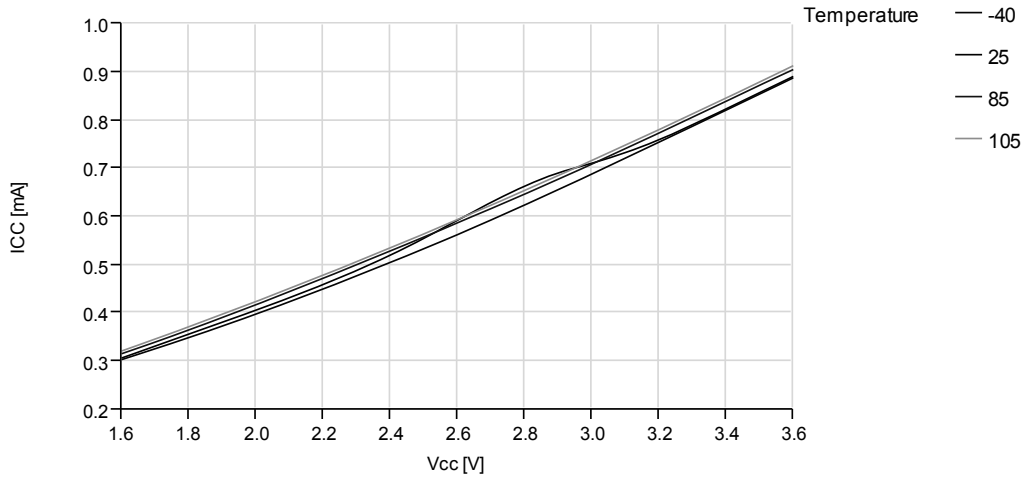
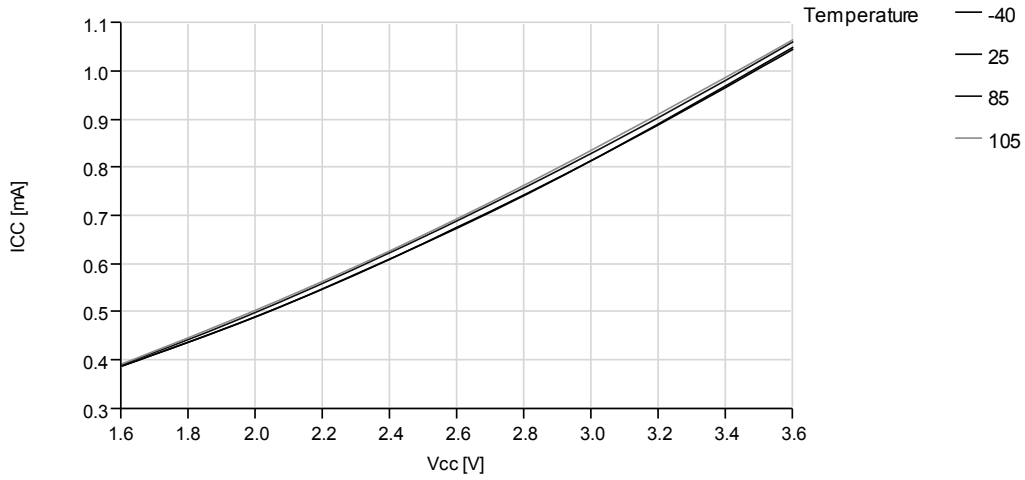


Figure 37-14.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 8MHz internal oscillator



37.1.3 Power-down Mode Supply Current

Figure 37-17.Power-down Mode Supply Current vs. Temperature

All functions disabled

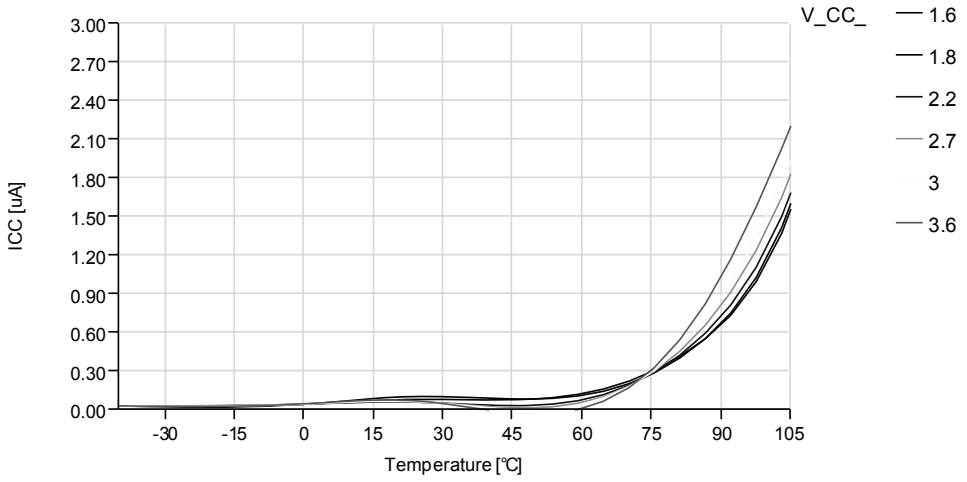
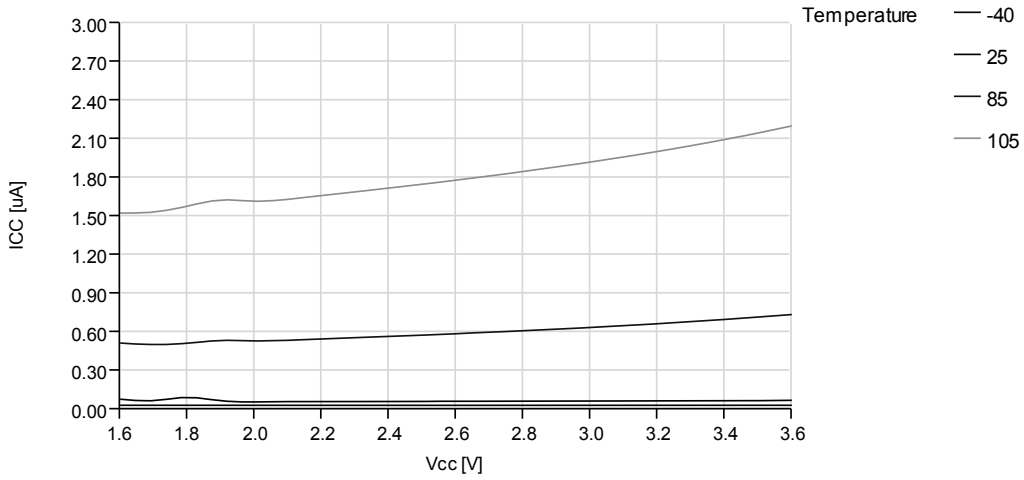


Figure 37-18.Power-down Mode supply Current vs. V_{CC}

All functions disabled



37.1.5 Standby Mode Supply Current

Figure 37-21.Standby Supply Current vs. V_{CC}

Standby, f_{SYS} = 1MHz

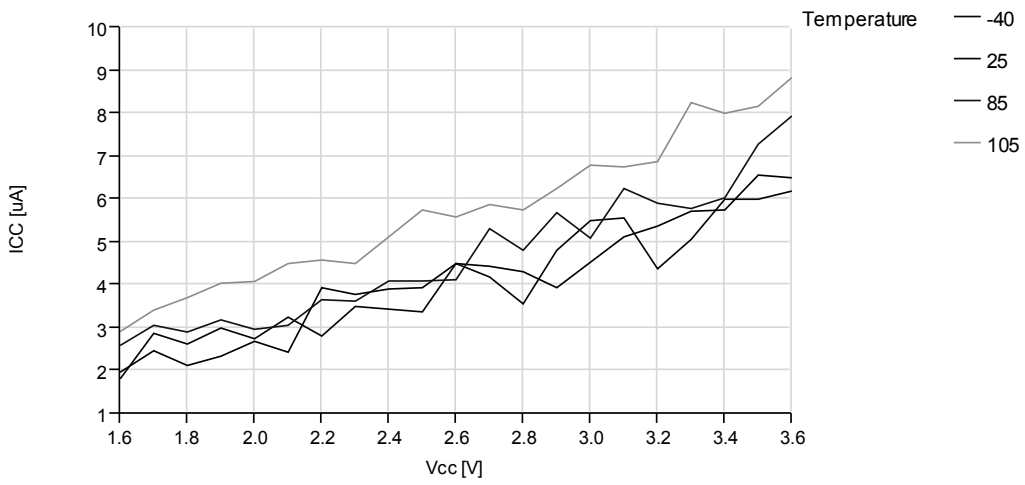


Figure 37-22.Standby Supply Current vs. V_{CC}

25°C, running from different crystal oscillators

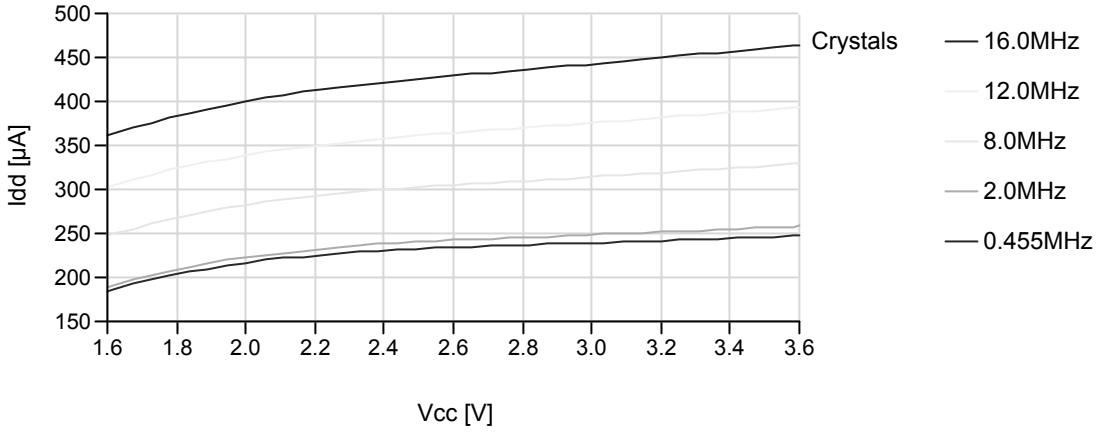
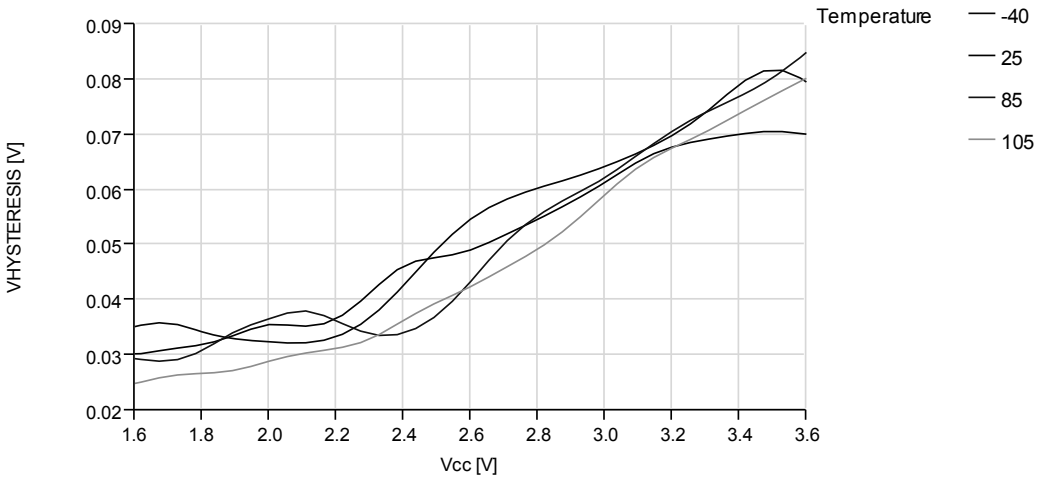


Figure 37-37.I/O Pin Input Hysteresis vs. V_{CC}



37.3 ADC Characteristics

Figure 37-38.ADC INL vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

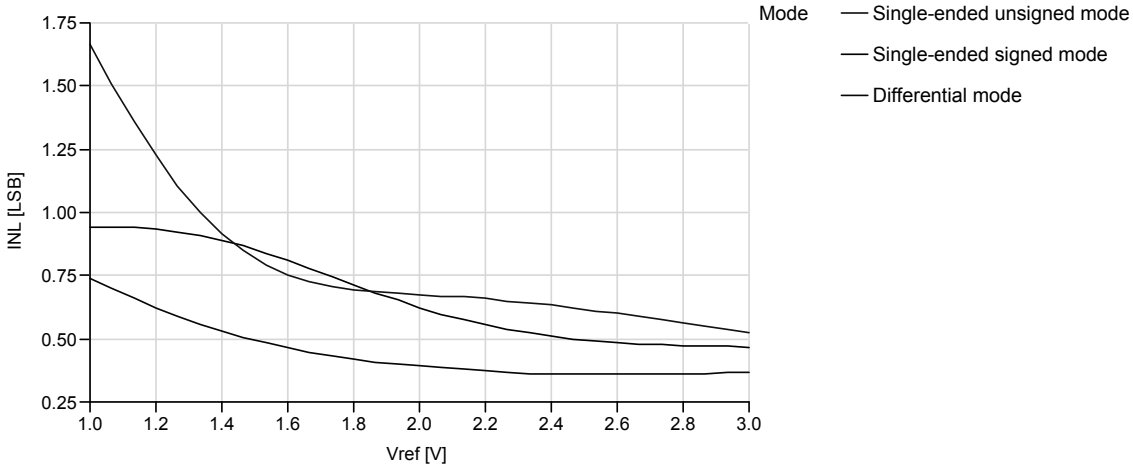


Figure 37-55.Analog Comparator Voltage Scaler vs. SCALEFAC

T = 25°C, V_{CC} = 3.0V

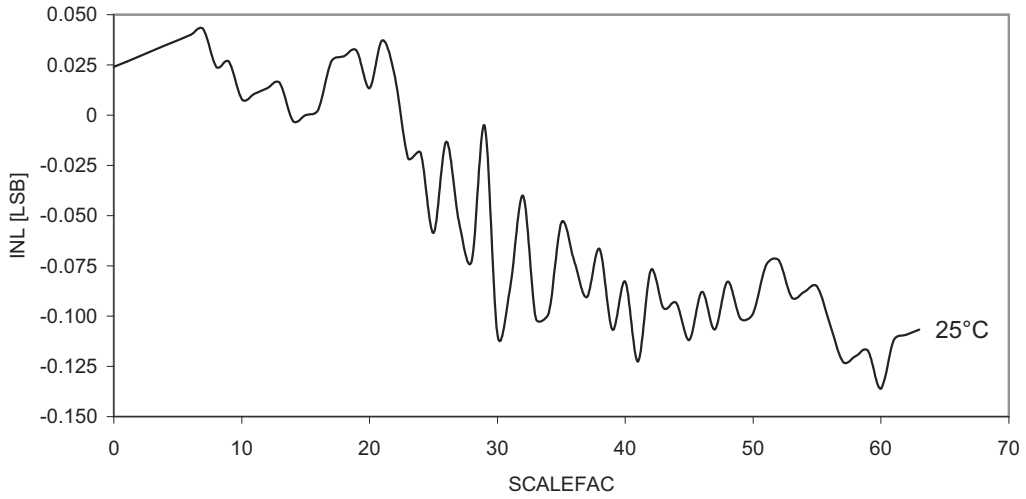
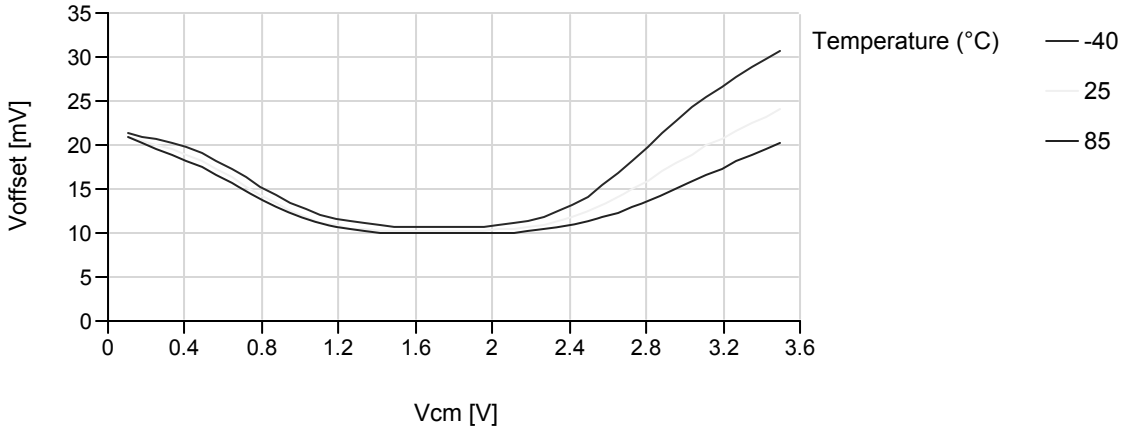
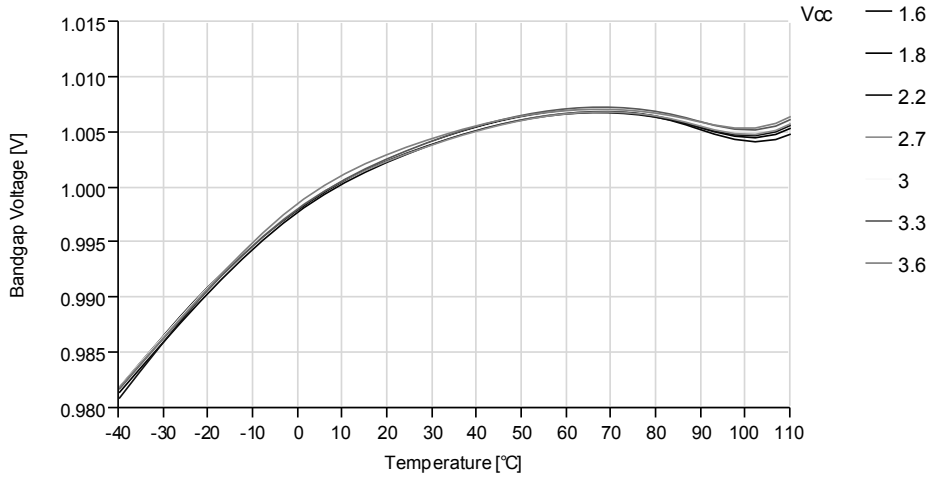


Figure 37-56.Analog Comparator Offset Voltage vs. Common Mode Voltage



37.6 Internal 1.0V Reference Characteristics

Figure 37-59.ADC/DAC Internal 1.0V Reference vs. Temperature



37.7 BOD Characteristics

Figure 37-60.BOD Thresholds vs. Temperature

BOD level = 1.6V

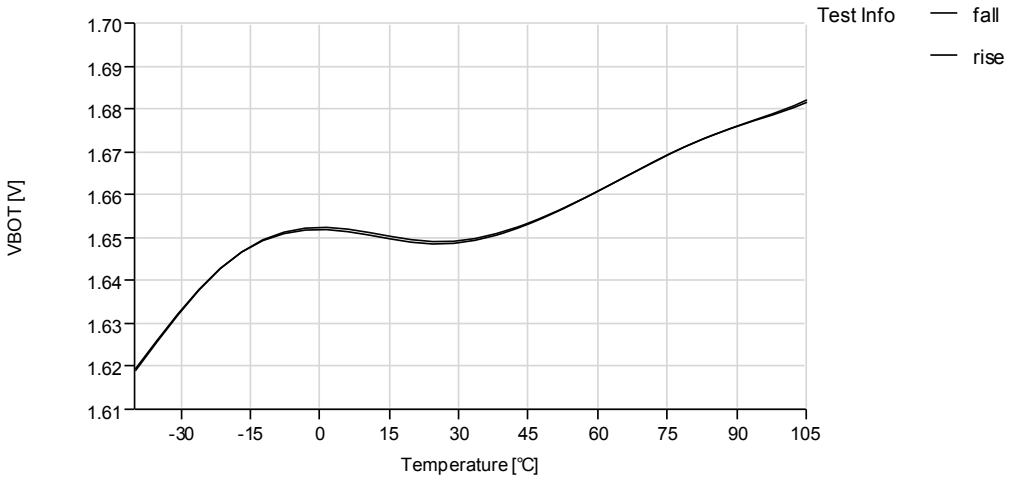
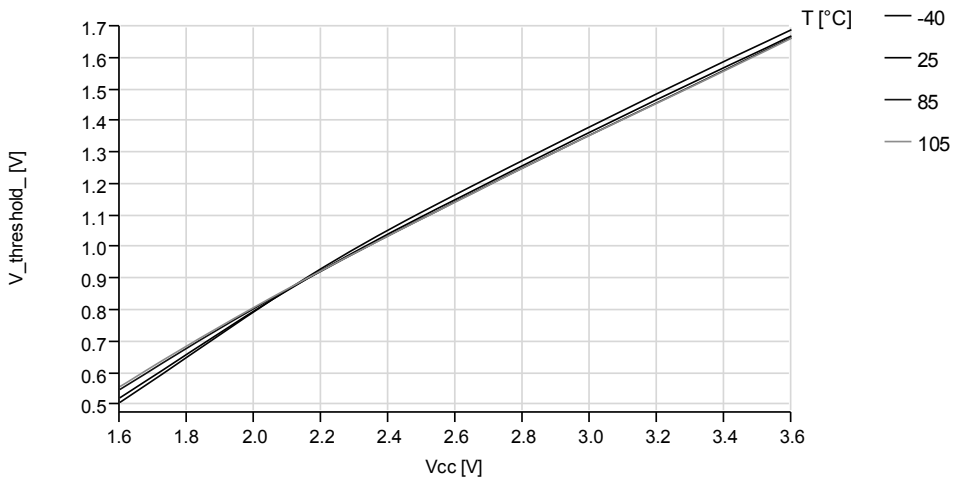


Figure 37-67.Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IL} - Reset pin read as "0"



37.9 Power-on Reset Characteristics

Figure 37-68.Power-on Reset Current Consumption vs. V_{CC}

BOD level = 3.0V, enabled in continuous mode