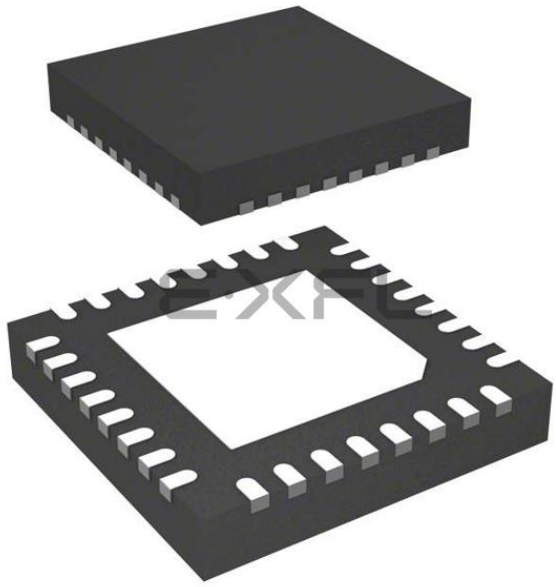

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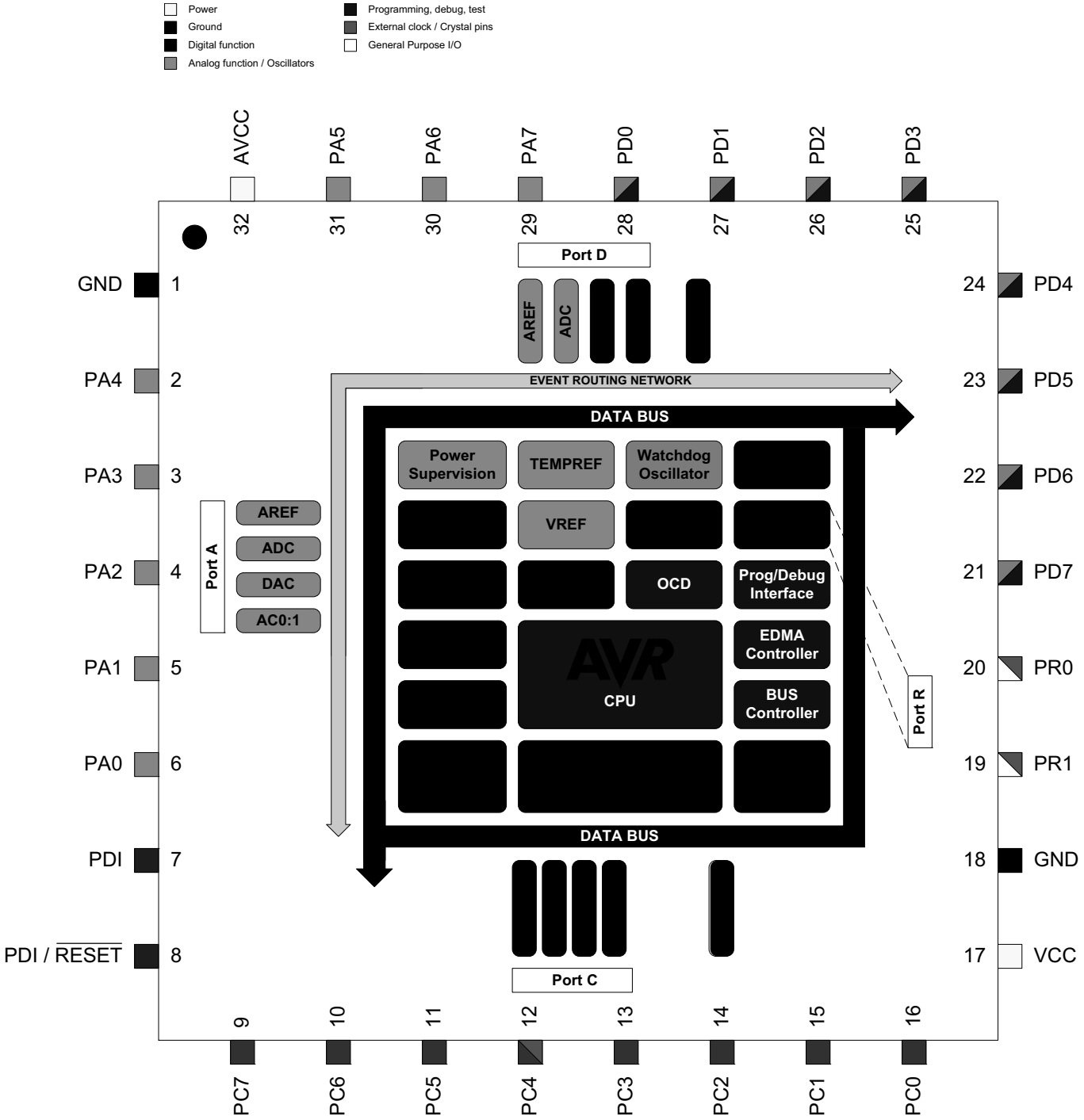
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32e5-m4ur

3. Pinout and Block Diagram



Notes: 1. For full details on pinout and alternate pin functions refer to “Pinout and Pin Functions” on page 57.

4. Overview

The Atmel AVR XMEGA is a family of low power, high performance, and peripheral rich 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the AVR XMEGA devices achieve CPU throughput approaching one million instructions per second (MIPS) per megahertz, allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The AVR XMEGA E5 devices provide the following features: in-system programmable flash with read-while-write capabilities; internal EEPROM and SRAM; four-channel enhanced DMA (EDMA) controller; eight-channel event system with asynchronous event support; programmable multilevel interrupt controller; 26 general purpose I/O lines; CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3) generators; one XMEGA Custom Logic module with timer, counter and logic functions (XCL); 16-bit real-time counter (RTC) with digital correction; three flexible, 16-bit timer/counters with compare and PWM channels; two USARTs; one two-wire serial interface (TWI) allowing simultaneous master and slave; one serial peripheral interface (SPI); one sixteen-channel, 12-bit ADC with programmable gain, offset and gain correction, averaging, over-sampling and decimation; one 2-channel 12-bit DAC; two analog comparators (ACs) with window mode and current sources; programmable watchdog timer with separate internal oscillator; accurate internal oscillators with PLL and prescaler; and programmable brown-out detection.

The program and debug interface (PDI), a fast, two-pin interface for programming and debugging, is available.

The AVR XMEGA E5 devices have five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, EDMA controller, event system, interrupt controller, and all peripherals to continue functioning. The power-down mode saves the SRAM and register contents, but stops the oscillators, disabling all other functions until the next TWI, or pin-change interrupt, or reset. In power-save mode, the asynchronous real-time counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In standby mode, the external crystal oscillator keeps running while the rest of the device is sleeping. This allows very fast startup from the external crystal, combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run. In each power save, standby or extended standby mode, the low power mode of the internal 8MHz oscillator allows very fast startup time combined with very low power consumption.

To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in active mode and idle sleep mode and low power mode of the internal 8MHz oscillator can be enabled.

Atmel offers a free QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The devices are manufactured using Atmel high-density, nonvolatile memory technology. The program flash memory can be reprogrammed in-system through the PDI. A boot loader running in the device can use any interface to download the application program to the flash memory. The boot loader software in the boot flash section can continue to run. By combining an 8/16-bit RISC CPU with in-system, self-programmable flash, the AVR XMEGA is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

All Atmel AVR XMEGA devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

14. WDT – Watchdog Timer

14.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
  - Normal mode
  - Window mode
- Configuration lock to prevent unwanted changes

14.2 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

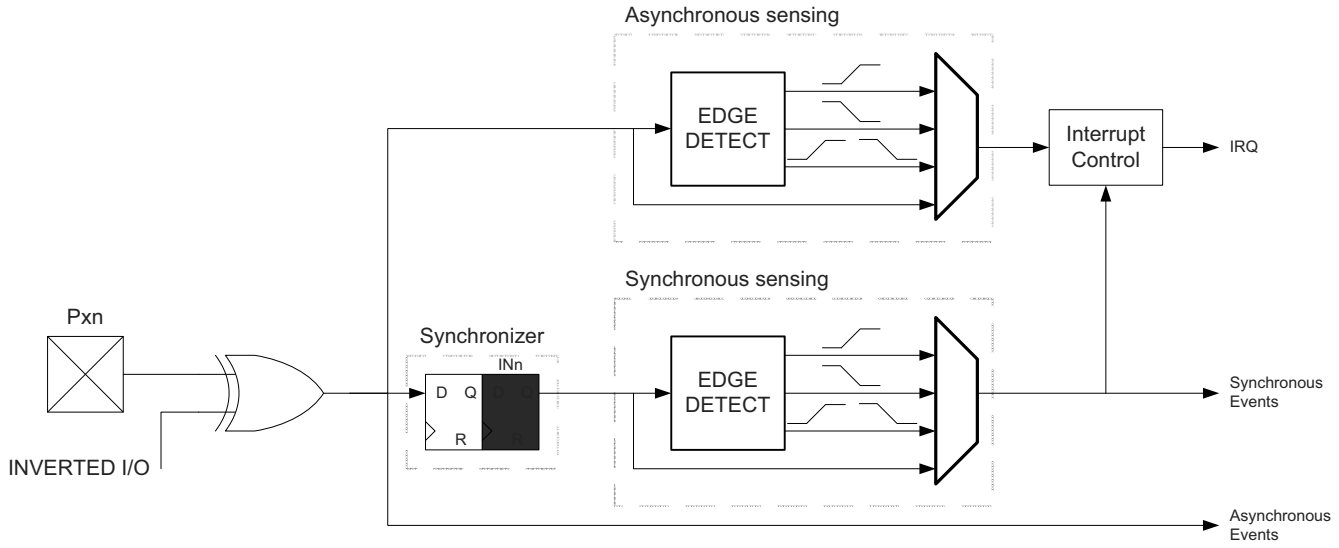
The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

16.4 Input Sensing

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in Figure 16-7.

Figure 16-7. Input Sensing System Overview



When a pin is configured with inverted I/O, the pin value is inverted before the input sensing.

16.5 Alternate Port Functions

Most port pins have alternate pin functions in addition to being a general purpose I/O pin. When an alternate function is enabled, it might override the normal port pin function or pin value. This happens when other peripherals that require pins are enabled or configured to use pins. If and how a peripheral will override and use pins is described in the section for that peripheral. “Pinout and Pin Functions” on page 57 shows which modules on peripherals that enable alternate functions on a pin, and which alternate functions that are available on a pin.

23. SPI – Serial Peripheral Interface

23.1 Features

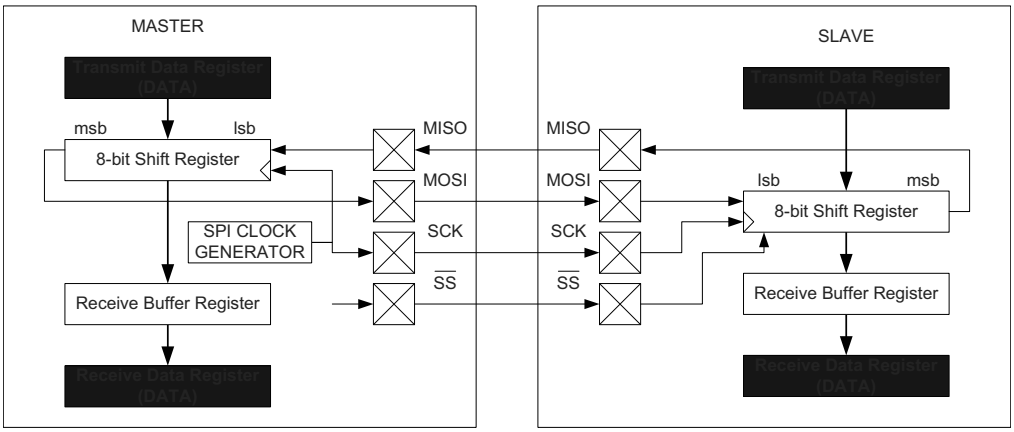
- One SPI peripheral
- Full-duplex, three-wire synchronous data transfer
- Master or slave operation
- lsb first or msb first data transfer
- Eight programmable bit rates
- Interrupt flag at the end of transmission
- Write collision flag to indicate data collision
- Wake up from idle sleep mode
- Double speed master mode

23.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed, full duplex, synchronous data transfer interface using three or four pins. It allows fast communication between an AVR XMEGA device and peripheral devices or between several microcontrollers.

A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions. The interconnection between master and slave devices with SPI is shown in Figure 23-1. The system consists of two shift registers and a clock generator. The SPI master initiates the communication by pulling the slave select (SS) signal low for the desired slave. Master and slave prepare the data to be sent in their respective shift registers, and the master generates the required clock pulses on the SCK line to interchange data. Data are always shifted from master to slave on the master output, slave input (MOSI) line, and from slave to master on the master input, slave output (MISO) line. After each data packet, the master can synchronize the slave by pulling the $\overline{SS}$ line high.

Figure 23-1. SPI Master-slave Interconnection



By default, the SPI module is single buffered and transmit direction and double buffered in the receive direction. A byte written to the transmit data register will be copied to the shift register when a full character has been received. When receiving data, a received character must be read from the transmit data register before the third character has been completely shifted in to avoid losing data. Optionally, buffer modes can be enabled. When used, one buffer is available for transmitter and a double buffer for reception.

PORTC has one SPI. Notation of this is SPIC.

26. XCL – XMEGA Custom Logic Module

26.1 Features

- Two independent 8-bit timer/counter with:
  - Period and compare channel for each timer/counter
  - Input Capture for each timer
  - Serial peripheral data length control for each timer
  - Timeout support for each timer
  - Timer underflow interrupt/event
  - Compare match or input capture interrupt/event for each timer
- One 16-bit timer/counter by cascading two 8-bit timer/counters with:
  - Period and compare channel
  - Input capture
  - Timeout support
  - Timer underflow interrupt/event
  - Compare match or input capture interrupt/event
- Programmable lookup table supporting multiple configurations:
  - Two 2-input units
  - One 3-input unit
  - RS configuration
  - Duplicate input with selectable delay on one input or output
  - Connection to external I/O pins, event system or one selectable USART
- Combinatorial Logic Functions using programmable truth table:
  - AND, NAND, OR, NOR, XOR, XNOR, NOT, MUX
- Sequential Logic Functions:
  - D-Flip-Flop, D Latch, RS Latch
- Input sources:
  - From external pins or the event system
  - One input source includes selectable delay or synchronizing option
  - Can be shared with selectable USART pin locations
- Outputs:
  - Available on external pins or event system
  - Includes selectable delay or synchronizing option
  - Can override selectable USART pin locations
- Operates in active mode and all sleep modes

26.2 Overview

The XMEGA Custom Logic module (XCL) consists of two sub-units, each including 8-bit timer/counter with flexible settings, peripheral counter working with one software selectable USART module, delay elements, glue logic with programmable truth table and a global logic interconnect array.

The timer/counter configuration allows for two 8-bits timer/counters. Each timer/counter supports normal, compare and input capture operation, with common flexible clock selections and event channels for each timer. By cascading the two 8-bit timer/counters, the XCL can be used as a 16-bit timer/counter.

The peripheral counter (PEC) configuration, the XCL is connected to one software selectable USART. This USART controls the counter operation, and the PEC can optionally control the data length within the USART frame.

The glue logic configuration, the XCL implements two programmable lookup tables (LUTs). Each defines the truth table corresponding to the logical condition between two inputs. Any combinatorial function logic is possible. The LUT inputs can be connected to I/O pins or event system channels. If the LUT is connected to the USART0 pin locations, the data lines (TXD/RXD) data encoding/decoding will be possible. Connecting together the LUT units, RS Latch, or any combinatorial logic between two operands or three inputs can be enabled.

34. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	Rd ← Rd + Rr	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	Rd ← Rd + Rr + C	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	Rd ← Rd + 1:Rd + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	Rd ← Rd - Rr	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	Rd ← Rd - K	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	Rd ← Rd - Rr - C	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	Rd ← Rd - K - C	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	Rd + 1:Rd ← Rd + 1:Rd - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	Rd ← Rd • Rr	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	Rd ← Rd • K	Z,N,V,S	1
OR	Rd, Rr	Logical OR	Rd ← Rd v Rr	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	Rd ← Rd v K	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	Rd ← Rd ⊕ Rr	Z,N,V,S	1
COM	Rd	One’s Complement	Rd ← $FF - Rd	Z,C,N,V,S	1
NEG	Rd	Two’s Complement	Rd ← $00 - Rd	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FFh - K)	Z,N,V,S	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V,S	1
DEC	Rd	Decrement	Rd ← Rd - 1	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V,S	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V,S	1
SER	Rd	Set Register	Rd ← $FF	None	1
MUL	Rd,Rr	Multiply Unsigned	R1:R0 ← Rd x Rr (UU)	Z,C	2
MULS	Rd,Rr	Multiply Signed	R1:R0 ← Rd x Rr (SS)	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr (SU)	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	R1:R0 ← Rd x Rr<<1 (UU)	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	R1:R0 ← Rd x Rr<<1 (SS)	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← Rd x Rr<<1 (SU)	Z,C	2
DES	K	Data Encryption	if (H = 0) then R15:R0 ← Encrypt(R15:R0, K) else if (H = 1) then R15:R0 ← Decrypt(R15:R0, K)		1/2
Branch instructions					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2
EIJMP		Extended Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	2
JMP	k	Jump	PC ← k	None	3
RCALL	k	Relative Call Subroutine	PC ← PC + k + 1	None	2 / 3(1)

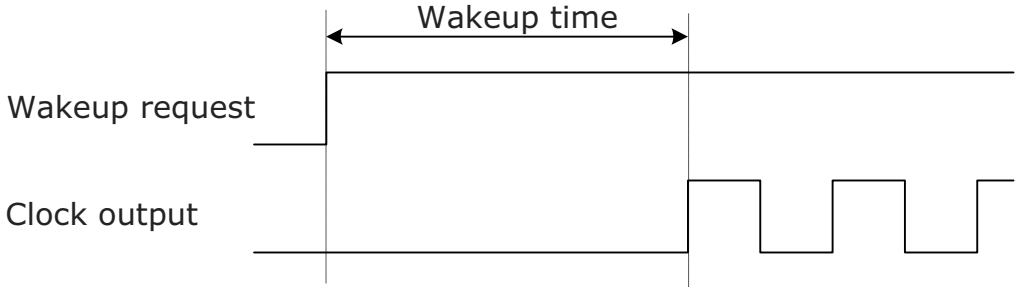
36.4 Wake-up Time from Sleep Modes

Table 36-5. Device Wake-up Time from Sleep Modes with Various System Clock Sources

Symbol	Parameter	Condition		Min.	Typ.(1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock			0.2		µs
		32kHz internal oscillator			120		
		8MHz internal oscillator			0.5		
		32MHz internal oscillator			0.2		
	Wake-up time from power save mode	External 2MHz clock			4.5		
		32kHz internal oscillator			320		
		8MHz internal oscillator	Normal mode		4.5		
			Low power mode		0.5		
		32MHz internal oscillator			5.0		
	Wake-up time from power down mode	External 2MHz clock			4.5		
		32kHz internal oscillator			320		
		8MHz internal oscillator			4.5		
		32MHz internal oscillator			5.0		

Notes: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 36-2. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 36-2. Wake-up Time Definition



36.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 36-24. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC}= 1.6 - 1.8V	20		48	
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

36.13.6 External Clock Characteristics

Figure 36-3. External Clock Drive Waveform

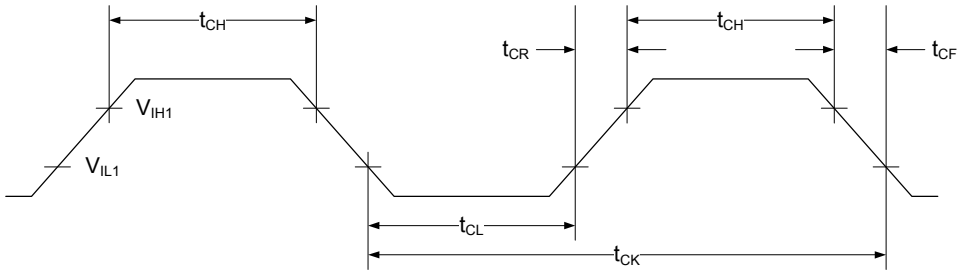


Table 36-25. External Clock used as System Clock without Prescaling

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

37. Typical Characteristics

37.1 Current Consumption

37.1.1 Active Mode Supply Current

Figure 37-1. Active Mode Supply Current vs. Frequency

f_{SYS} = 0 – 1MHz external clock, T = 25°C

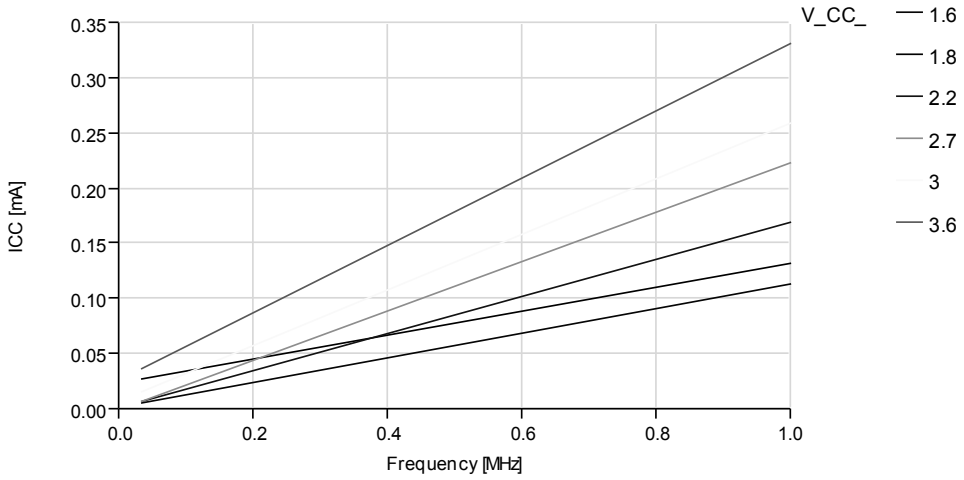


Figure 37-2. Active Mode Supply Current vs. Frequency

f_{SYS} = 0 – 32MHz external clock, T = 25°C

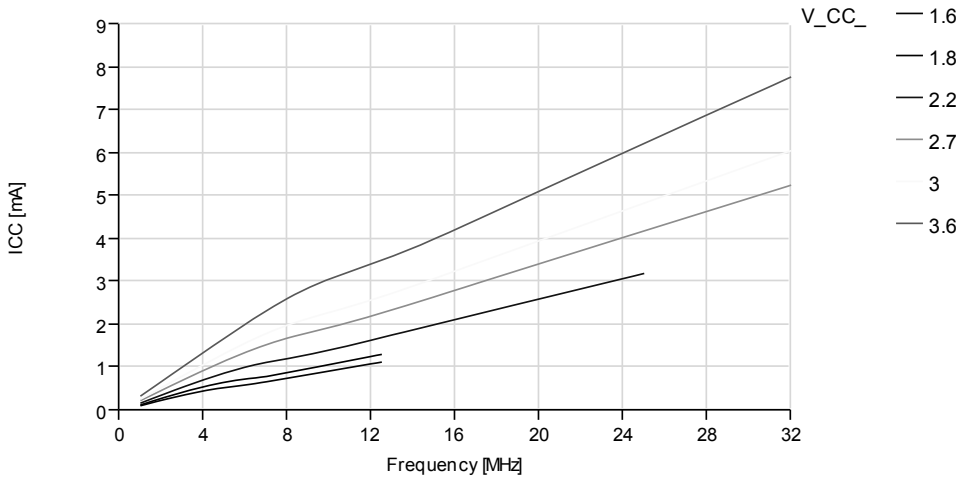


Figure 37-39.ADC INL Error vs. V_{CC}

T = 25°C, V_{REF} = 1.0V

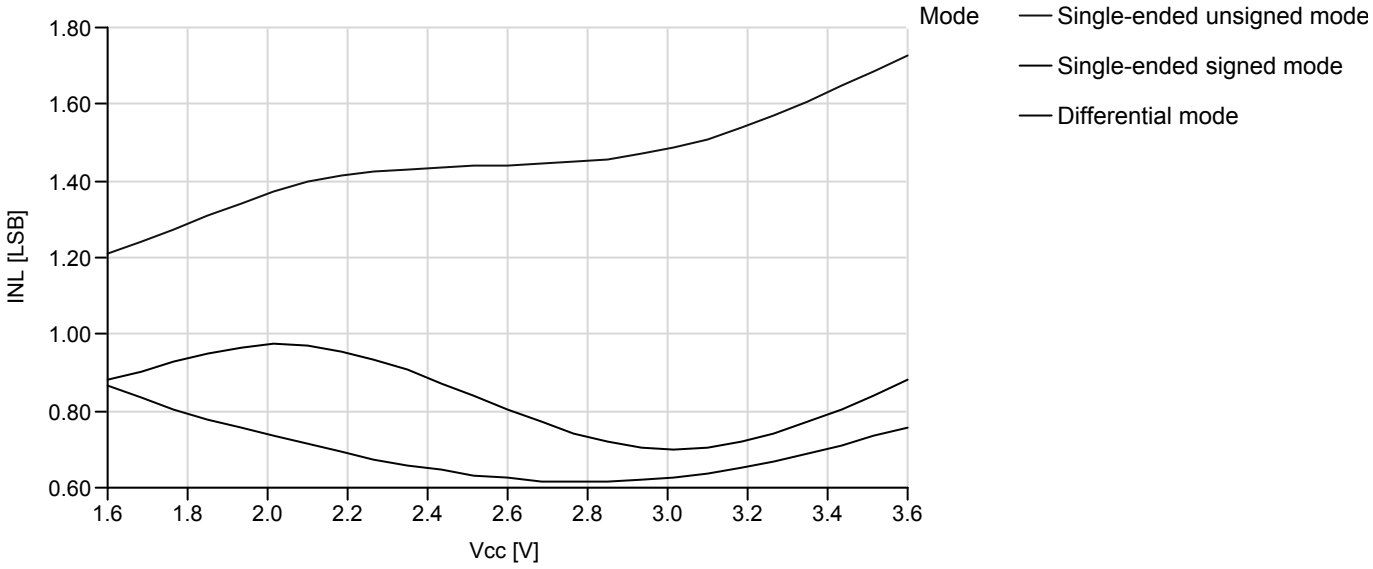


Figure 37-40.ADC DNL Error vs. V_{REF}

SE Unsigned mode, T=25°C, V_{CC} = 3.6V, external reference

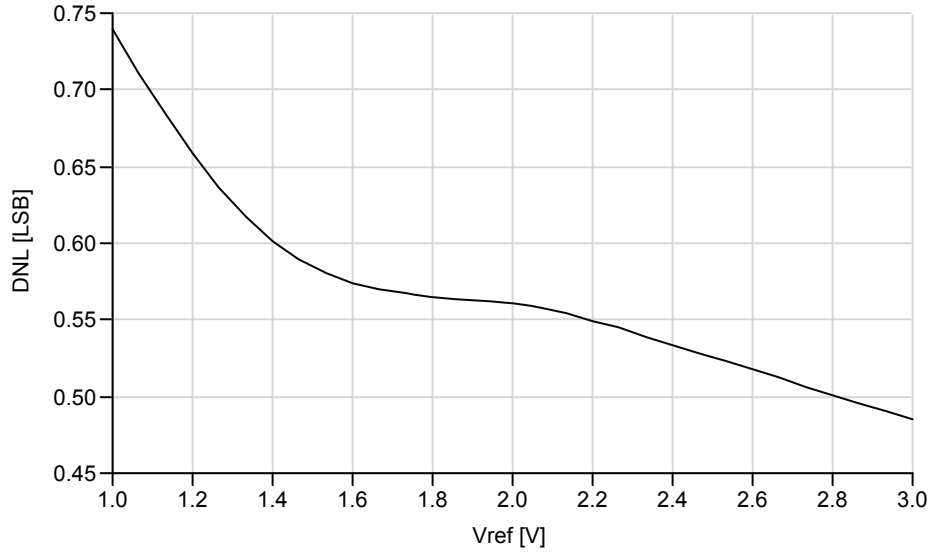


Figure 37-55.Analog Comparator Voltage Scaler vs. SCALEFAC

T = 25°C, V_{CC} = 3.0V

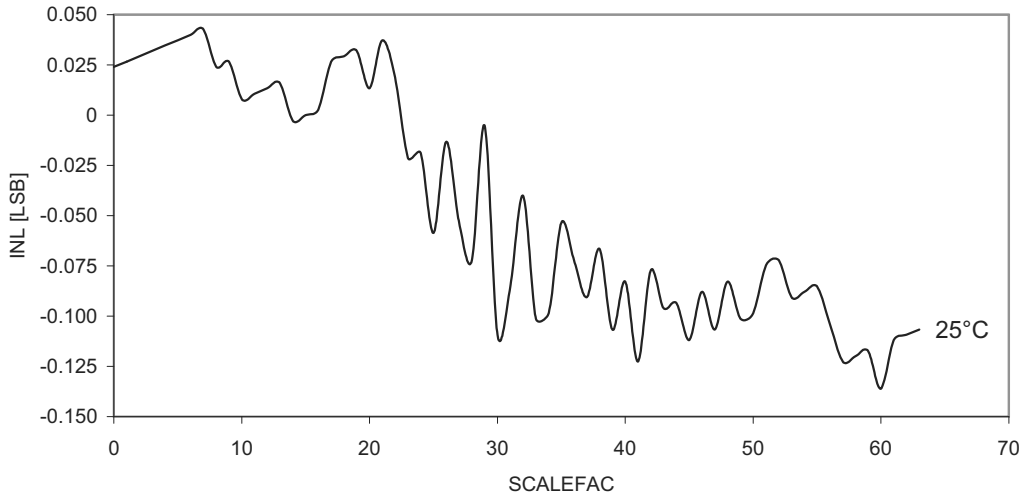
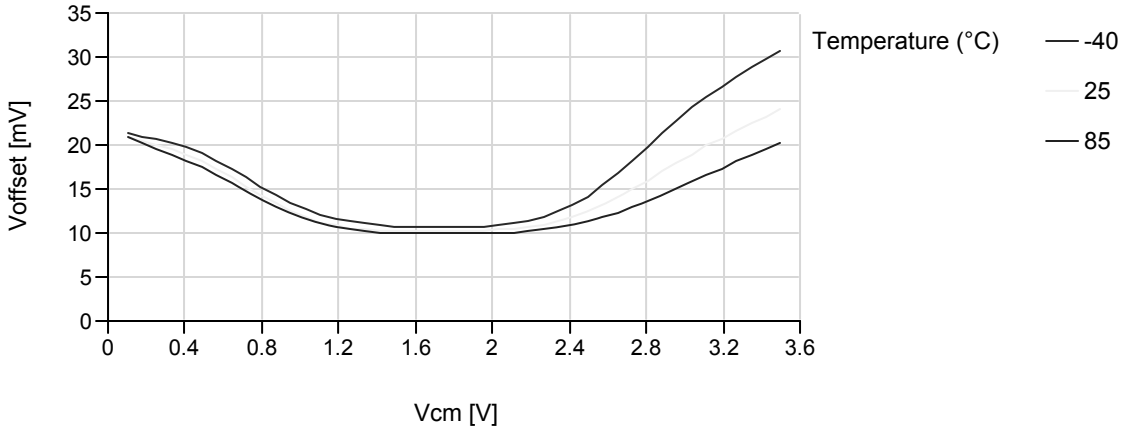
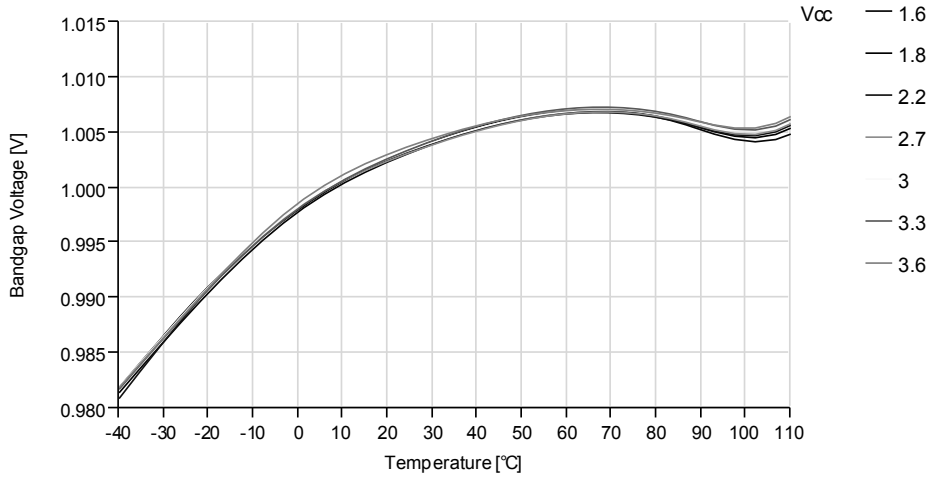


Figure 37-56.Analog Comparator Offset Voltage vs. Common Mode Voltage



37.6 Internal 1.0V Reference Characteristics

Figure 37-59.ADC/DAC Internal 1.0V Reference vs. Temperature



37.7 BOD Characteristics

Figure 37-60.BOD Thresholds vs. Temperature

BOD level = 1.6V

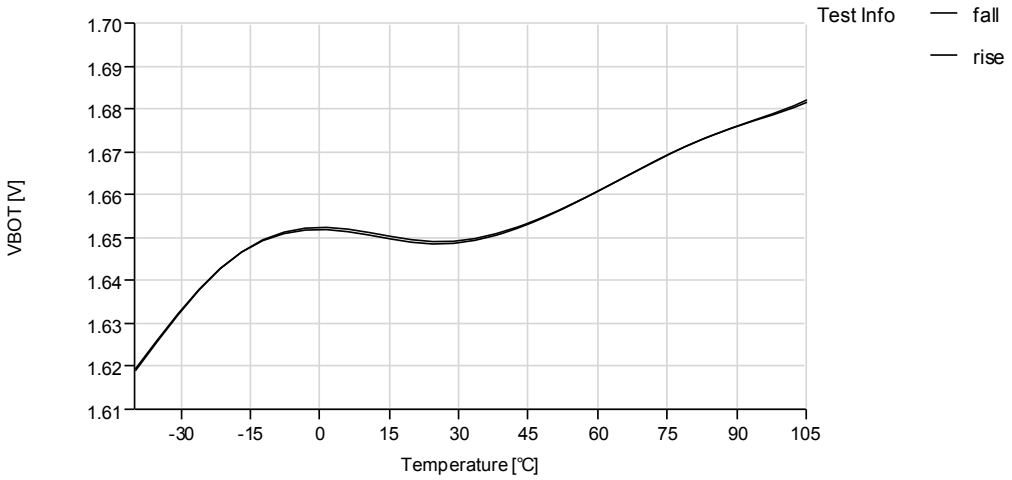
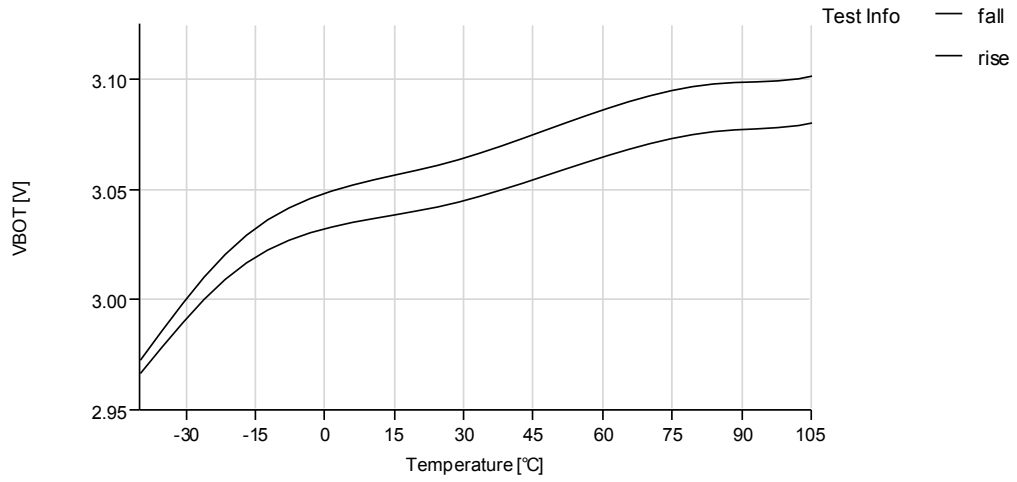


Figure 37-61.BOD Thresholds vs. Temperature

BOD level = 3.0V



37.8 External Reset Characteristics

Figure 37-62.Minimum Reset Pin Pulse Width vs. V_{CC}

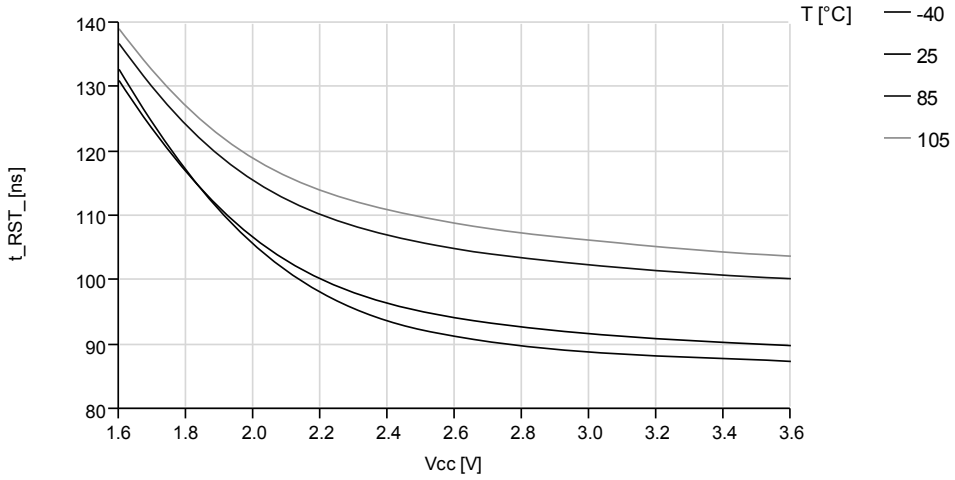


Figure 37-63.Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

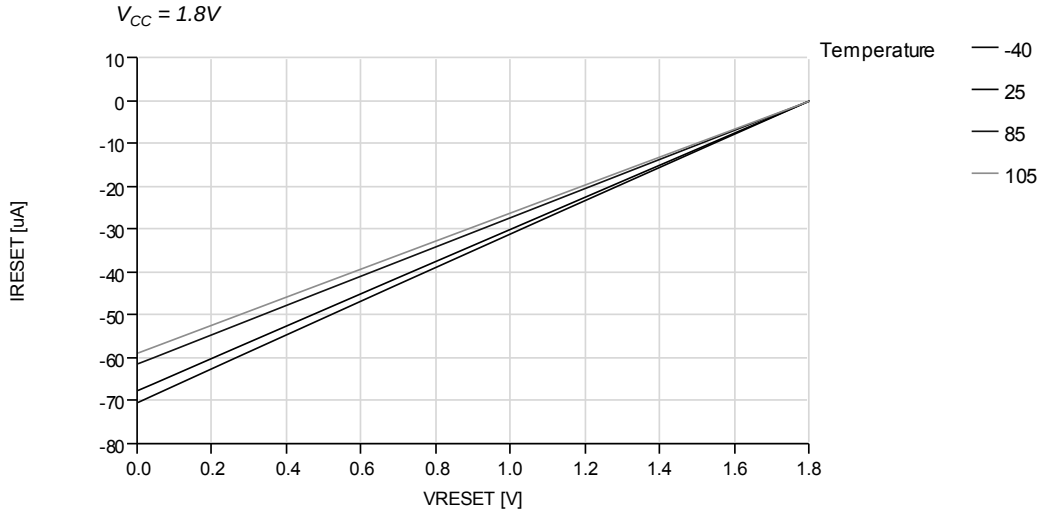
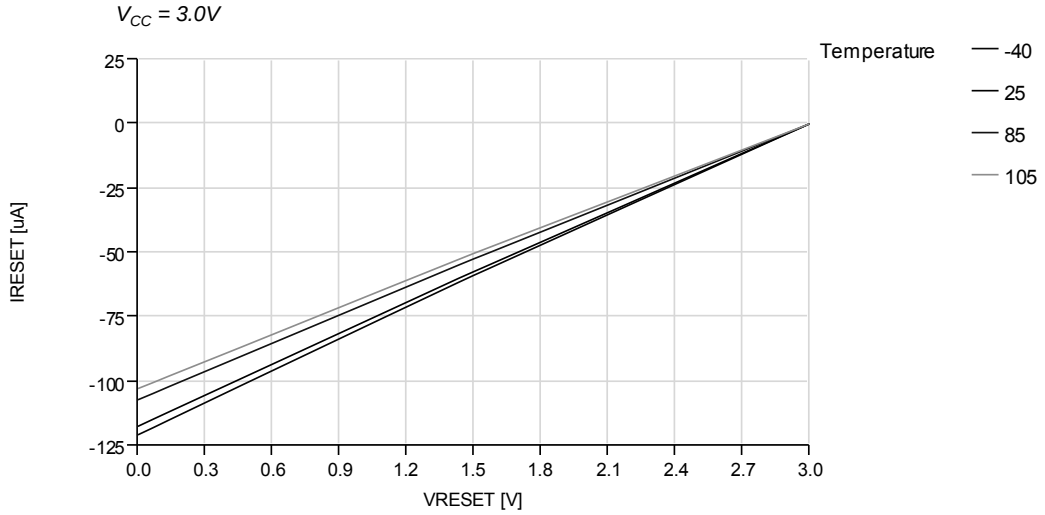


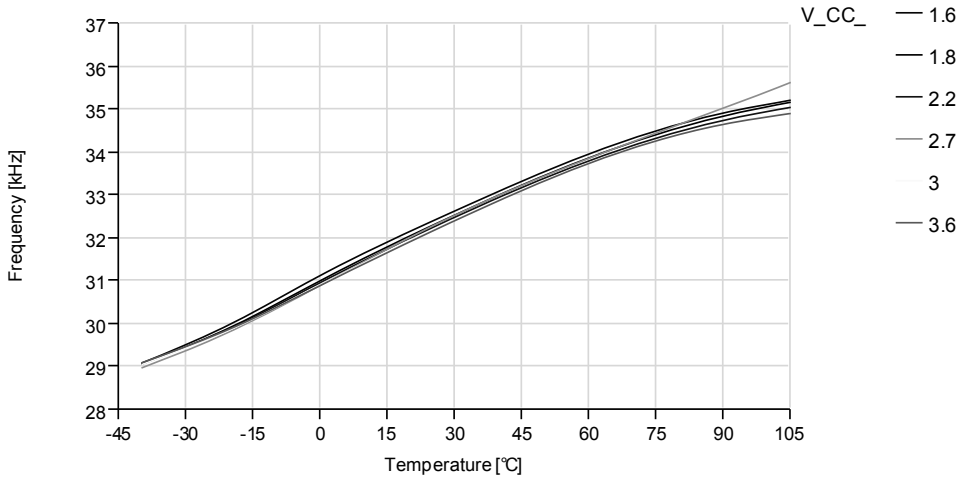
Figure 37-64.Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage



37.10 Oscillator Characteristics

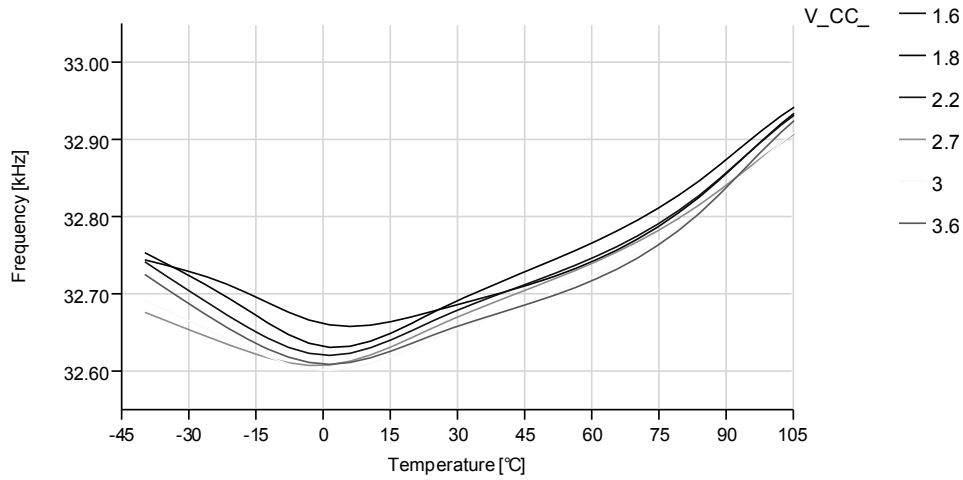
37.10.1 Ultra Low-Power Internal Oscillator

Figure 37-70. Ultra Low-Power Internal Oscillator Frequency vs. Temperature



37.10.2 32.768KHz Internal Oscillator

Figure 37-71. 32.768kHz Internal Oscillator Frequency vs. Temperature



37.10.4 32MHz Internal Oscillator

Figure 37-78. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

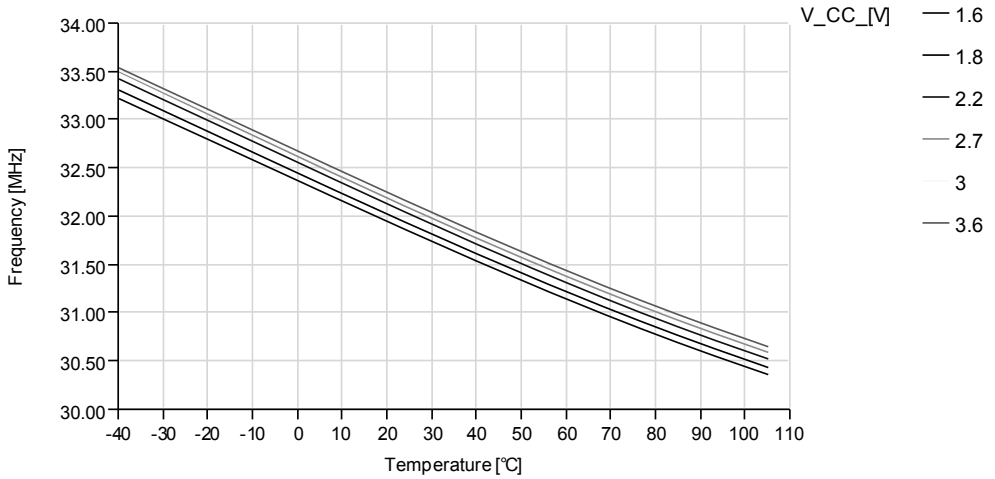
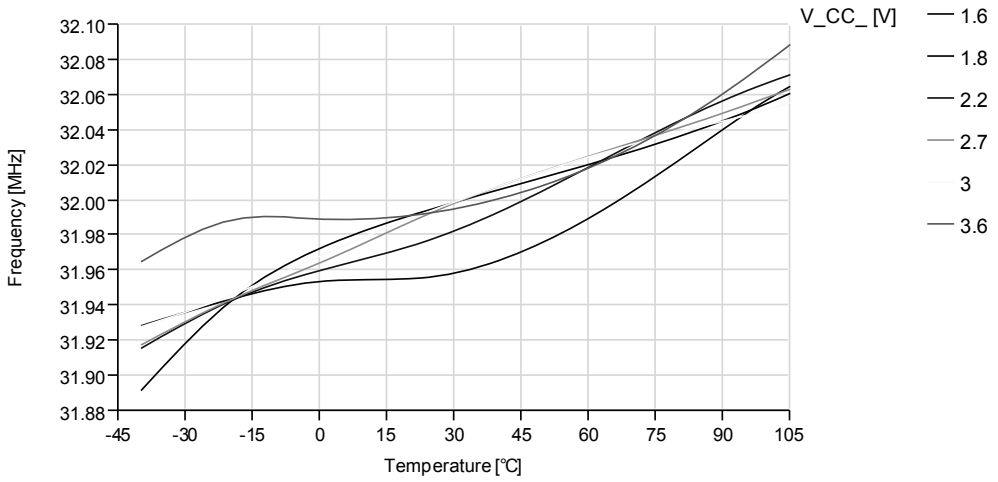


Figure 37-79. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator



39. Revision History

Please note that referring page numbers in this section are referred to this document. The referring revision in this document section are referring to the document revision.

39.1 8153K – 08/2016

1.	“Ordering Information” on page 2: Ordering codes for UQFN packages corrected from M4N/M4NR to M4UN/M4UNR.

39.2 8153J – 11/2014

1.	Changed error for ESR parameter in Table 36-27 on page 86.
2.	Changed the use of capital letters in heading, figure titles, and table headings.

39.3 8153I – 08/2014

1.	Removed preliminary from the front page.
2.	Updated with ESR info in Table 36-27 on page 86.
3.	Added errata on Automatic port override on PORT C in Section 38. “Errata – ATxmega32E5 / ATxmega16E5 / ATxmega8E5” on page 136.
4.	Added errata on Sext timer not implemented in slave mode in Section 38. “Errata – ATxmega32E5 / ATxmega16E5 / ATxmega8E5” on page 136.

39.4 8153H – 07/2014

1.	“Ordering Information” on page 2: Added ordering codes for XMEGA E5 devices @105°C.
2.	Electrical characteristics updates: “Current Consumption” : Added power-down numbers for 105°C and updated values in Table 36-3 on page 73. “ Flash and EEPROM Characteristics” : Added Flash and EEPROM write/erase cycles and data retention for 105°C in Table 36-18 on page 82.
3.	Changed Vcc to AVcc in Section 28. “ADC – 12-bit Analog to Digital Converter” on page 51 and in Section 30.1 “Features” on page 54.
4.	32.768 KHz changed to 32 kHz in the heading in Section 36.13.4 on page 84 and in Table 36-23 on page 84.
5.	Changed back page according to datasheet template 2014-0502.

39.5 8153G – 10/2013

1.	Updated wake-up time from power-save mode for 32MHz internal oscillator from 0.2µs to 5.0µs in Table 36-5 on page 75.

39.6 8153F – 08/2013

1.	TWI characteristics: Units of Data setup time ($t_{SU;DAT}$) changed from µs to ns in Table 36-30 on page 91.

39.7 8153E – 06/2013

1.	Errata “Rev. B” : Updated date code from 1318 to 1324 in “Temperature sensor not calibrated” on page 137.

39.8 8153D – 06/2013

1.	Analog Comparator Characteristics: Updated minimum and maximum values of Input Voltage Range, Table 36-14 on page 80.

39.9 8153C – 05/2013

1.	Electrical Characteristics, Table on page 73: Updated typical value from 7mA to 6mA for Active Current Consumption, 32MHz, V_{CC}=3.0V.
2.	Errata “Rev. A” and “Rev. B” : Added DAC errata: AREF on PORT C0.

39.10 8153B – 04/2013

1.	“Rev. B” on page 136: Removed the “EDMA: Channel transfer never stops when double buffering is enabled on sub-sequent channels” errata.

39.11 8153A – 04/2013

1.	Initial revision.