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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atxmega32e5-mur">https://www.e-xfl.com/product-detail/microchip-technology/atxmega32e5-mur</a>

## 7.4 ALU - Arithmetic Logic Unit

The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed. The ALU operates in direct connection with all 32 general purpose registers. In a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed and the result is stored in the register file. After an arithmetic or logic operation, the status register is updated to reflect information about the result of the operation.

ALU operations are divided into three main categories – arithmetic, logical, and bit functions. Both 8- and 16-bit arithmetic is supported, and the instruction set allows for efficient implementation of 32-bit arithmetic. The hardware multiplier supports signed and unsigned multiplication and fractional format.

### 7.4.1 Hardware Multiplier

The multiplier is capable of multiplying two 8-bit numbers into a 16-bit result. The hardware multiplier supports different variations of signed and unsigned integer and fractional numbers:

- Multiplication of unsigned integers
- Multiplication of signed integers
- Multiplication of a signed integer with an unsigned integer
- Multiplication of unsigned fractional numbers
- Multiplication of signed fractional numbers
- Multiplication of a signed fractional number with an unsigned one

A multiplication takes two CPU clock cycles.

## 7.5 Program Flow

After reset, the CPU starts to execute instructions from the lowest address in the flash program memory '0.' The program counter (PC) addresses the next instruction to be fetched.

Program flow is provided by conditional and unconditional jump and call instructions capable of addressing the whole address space directly. Most AVR instructions use a 16-bit word format, while a limited number use a 32-bit format.

During interrupts and subroutine calls, the return address PC is stored on the stack. The stack is allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. After reset, the stack pointer (SP) points to the highest address in the internal SRAM. The SP is read/write accessible in the I/O memory space, enabling easy implementation of multiple stacks or stack areas. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR CPU.

## 7.6 Status Register

The status register (SREG) contains information about the result of the most recently executed arithmetic or logic instruction. This information can be used for altering program flow in order to perform conditional operations. Note that the status register is updated after all ALU operations, as specified in the instruction set reference. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The status register is not automatically stored when entering an interrupt routine nor restored when returning from an interrupt. This must be handled by software.

The status register is accessible in the I/O memory space.

## 7.7 Stack and Stack Pointer

The stack is used for storing return addresses after interrupts and subroutine calls. It can also be used for storing temporary data. The stack pointer (SP) register always points to the top of the stack. It is implemented as two 8-bit registers that are accessible in the I/O memory space. Data are pushed and popped from the stack using the PUSH and POP instructions. The stack grows from a higher memory location to a lower memory location. This implies that pushing data onto the stack decreases the SP, and popping data off the stack increases the SP. The SP is automatically loaded

the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 71.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 8-1.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

**Table 8-1. Device ID Bytes for Atmel AVR XMEGA E5 Devices**

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega32E5	4C	95	1E
ATxmega16E5	45	94	1E
ATxmega8E5	41	93	1E

### 8.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

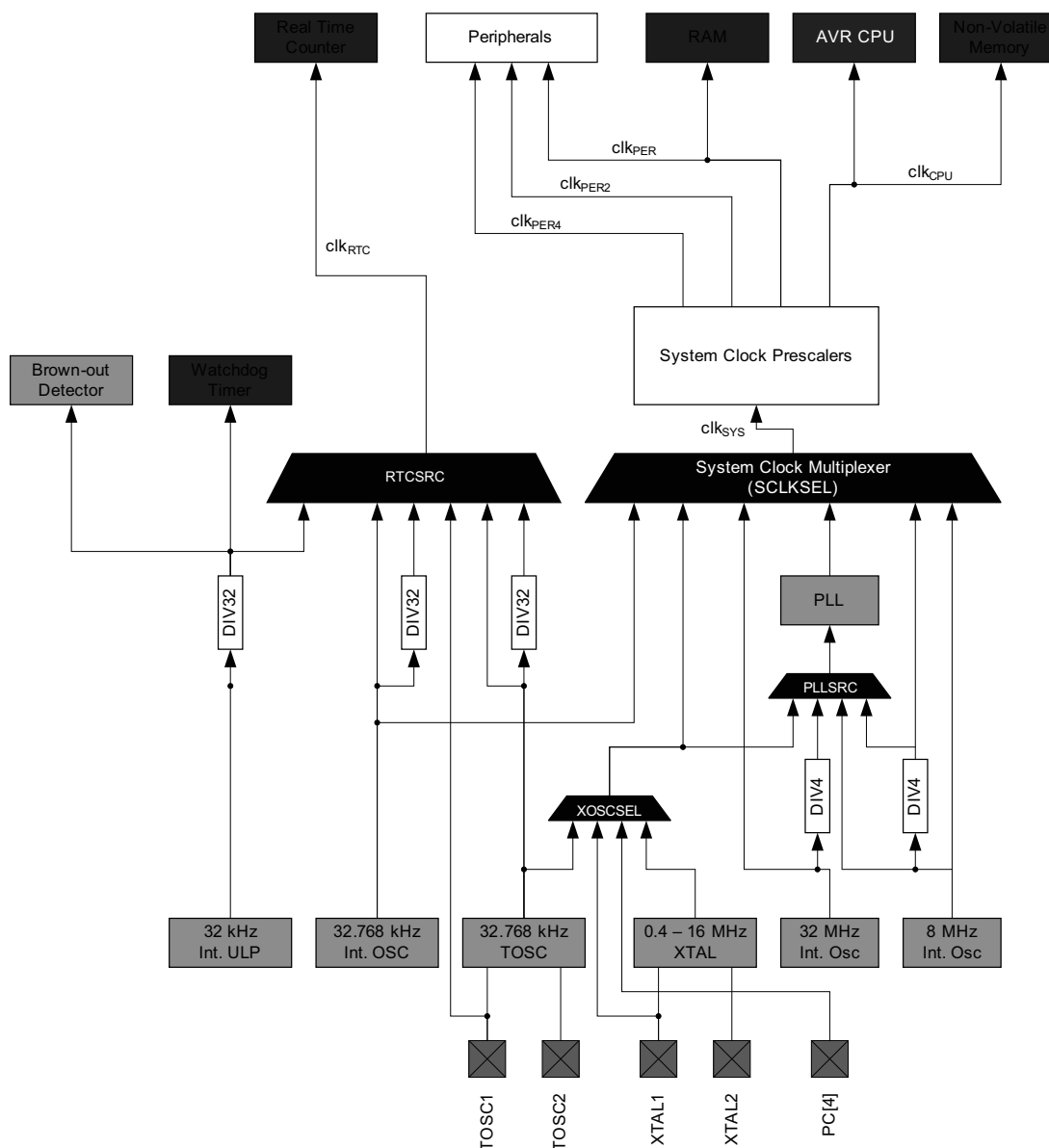
## 8.4 Fuses and Lock Bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, startup configuration, etc.

The lock bits are used to set protection levels for the different flash sections (i.e., if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

An un-programmed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero. Both fuses and lock bits are reprogrammable like the flash program memory.

**Figure 11-1. The Clock System, Clock Sources, and Clock Distribution**



## 11.3 Clock Sources

The clock sources are divided in two main groups: internal oscillators and external clock sources. Most of the clock sources can be directly enabled and disabled from software, while others are automatically enabled or disabled, depending on peripheral settings. After reset, the device starts up running from the 2MHz output of the 8MHz internal oscillator. The other clock sources, DFLL and PLL, are turned off by default.

The internal oscillators do not require any external components to run. For details on characteristics and accuracy of the internal oscillators, refer to the device datasheet.

### 11.3.1 32kHz Ultra Low Power Internal Oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz ultra low power (ULP) internal oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built-in prescaler that provides a 1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device. This oscillator can be selected as the clock source for the RTC.

### 11.3.2 32.768kHz Calibrated Internal Oscillator

This oscillator provides an approximate 32.768kHz clock. It is calibrated during production to provide a default frequency close to its nominal frequency. The calibration register can also be written from software for run-time calibration of the oscillator frequency. The oscillator employs a built-in prescaler, which provides both a 32.768kHz output and a 1.024kHz output.

### 11.3.3 32.768kHz Crystal Oscillator

A 32.768kHz crystal oscillator can be connected between the TOSC1 and TOSC2 pins and enables a dedicated low frequency oscillator input circuit. A low power mode with reduced voltage swing on TOSC2 is available. This oscillator can be used as a clock source for the system clock and RTC, and as the DFLL reference clock.

### 11.3.4 0.4 - 16MHz Crystal Oscillator

This oscillator can operate in four different modes optimized for different frequency ranges, all within 0.4 - 16MHz.

### 11.3.5 8MHz Calibrated Internal Oscillator

The 8MHz calibrated internal oscillator is the default system clock source after reset. It is calibrated during production to provide a default frequency close to its nominal frequency. The calibration register can also be written from software for run-time calibration of the oscillator frequency. The oscillator employs a built-in prescaler, with 2MHz output. The default output frequency at start-up and after reset is 2MHz. A low power mode option can be used to enable fast system wake-up from power-save mode. In all other modes, the low power mode can be enabled to significantly reduce the power consumption of the internal oscillator.

### 11.3.6 32MHz Run-time Calibrated Internal Oscillator

The 32MHz run-time calibrated internal oscillator is a high-frequency oscillator. It is calibrated during production to provide a default frequency close to its nominal frequency. A digital frequency locked loop (DFLL) can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy. This oscillator can also be adjusted and calibrated to any frequency between 30 and 55MHz.

### 11.3.7 External Clock Sources

The XTAL1 and XTAL2 pins can be used to drive an external oscillator, either a quartz crystal or a ceramic resonator. XTAL1 or pin 4 of port C (PC4) can be used as input for an external clock signal. The TOSC1 and TOSC2 pins are dedicated to driving a 32.768kHz crystal oscillator.

### 11.3.8 PLL with 1x-31x Multiplication Factor

The built-in phase locked loop (PLL) can be used to generate a high-frequency system clock. The PLL has a user-selectable multiplication factor of from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

## 15. Interrupts and Programmable Multilevel Interrupt Controller

### 15.1 Features

- Short and predictable interrupt response time
- Separate interrupt configuration and vector address for each interrupt
- Programmable multilevel interrupt controller
  - Interrupt prioritizing according to level and vector address
  - Three selectable interrupt levels for all interrupts: low, medium, and high
  - Selectable, round-robin priority scheme within low-level interrupts
  - Non-maskable interrupts for critical functions
- Interrupt vectors optionally placed in the application section or the boot loader section

### 15.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

### 15.3 Interrupt Vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA E5 devices are shown in Table 15-1. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA AU manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 15-1. The program address is the word address.

**Table 15-1. Peripheral Module Address Map**

Program address (base address)	Source	Interrupt description
0x0000	RESET	
0x0002	OSCF_INT_vect	Crystal oscillator failure and PLL lock failure interrupt vector (NMI)
0x0004	PORTR_INT_vect	Port R Interrupt vector
0x0006	EDMA_INT_base	EDMA Controller Interrupt base
0x000E	RTC_INT_base	Real time counter interrupt base
0x0012	PORTC_INT_vect	Port C interrupt vector
0x0014	TWIC_INT_base	Two-wire interface on Port C interrupt base
0x0018	TCC4_INT_base	Timer/counter 4 on port C interrupt base

The output override disable unit can disable the waveform output on selectable port pins to optimize the pins usage. This is to free the pins for other functional use, when the application does not need the waveform output spread across all the port pins as they can be selected by the OTMX configurations.

The waveform extension is available for TCC4 and TCC5. The notation of this is WEXC.

## 21. RTC – 16-bit Real-Time Counter

### 21.1 Features

- 16-bit resolution
- Selectable clock source
  - 32.768kHz external crystal
  - External clock
  - 32.768kHz internal oscillator
  - 32kHz internal ULP oscillator
- Programmable 10-bit clock prescaling
- One compare register
- One period register
- Clear counter on period overflow
- Optional interrupt/event on overflow and compare match
- Correction for external crystal oscillator frequency error down to  $\pm 0.5$ ppm accuracy

### 21.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5 $\mu$ s, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than 18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.



Base Address	Name	Description
0x07E0	PORTR	Port R
0x0800	TCC4	Timer/Counter 4 on port C
0x0840	TCC5	Timer/Counter 5 on port C
0x0880	FAULTC4	Fault Extension on TCC4
0x0890	FAULTC5	Fault Extensionon TCC5
0x08A0	WEXC	Waveform Extension on port C
0x08B0	HIRES	High Resolution Extension on port C
0x08C0	USARTC0	USART 0 on port C
0x08E0	SPIC	Serial Peripheral Interface on port C
0x08F8	IRCOM	Infrared Communication Module
0x0940	TCD5	Timer/Counter 5 on port D
0x09C0	USARTD0	USART 0 on port D

## 34. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	$Rd \leftarrow Rd + Rr$	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	$Rd \leftarrow Rd + 1:Rd + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	$Rd \leftarrow Rd - Rr$	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	$Rd \leftarrow Rd - K$	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	$Rd \leftarrow Rd - K - C$	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	$Rd + 1:Rd \leftarrow Rd + 1:Rd - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	$Rd \leftarrow Rd \bullet Rr$	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	$Rd \leftarrow Rd \bullet K$	Z,N,V,S	1
OR	Rd, Rr	Logical OR	$Rd \leftarrow Rd \vee Rr$	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	$Rd \leftarrow Rd \oplus Rr$	Z,N,V,S	1
COM	Rd	One's Complement	$Rd \leftarrow \$FF - Rd$	Z,C,N,V,S	1
NEG	Rd	Two's Complement	$Rd \leftarrow \$00 - Rd$	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (\$FFh - K)$	Z,N,V,S	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V,S	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V,S	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V,S	1
SER	Rd	Set Register	$Rd \leftarrow \$FF$	None	1
MUL	Rd,Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr (UU)$	Z,C	2
MULS	Rd,Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr (SS)$	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr (SU)$	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr << 1 (UU)$	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	$R1:R0 \leftarrow Rd \times Rr << 1 (SS)$	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr << 1 (SU)$	Z,C	2
DES	K	Data Encryption	if (H = 0) then R15:R0 $\leftarrow$ Encrypt(R15:R0, K) else if (H = 1) then R15:R0 $\leftarrow$ Decrypt(R15:R0, K)		1/2
Branch instructions					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow 0$	None	2
EIJMP		Extended Indirect Jump to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow EIND$	None	2
JMP	k	Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Call Subroutine	$PC \leftarrow PC + k + 1$	None	2 / 3 <sup>(1)</sup>

35.3 32MA

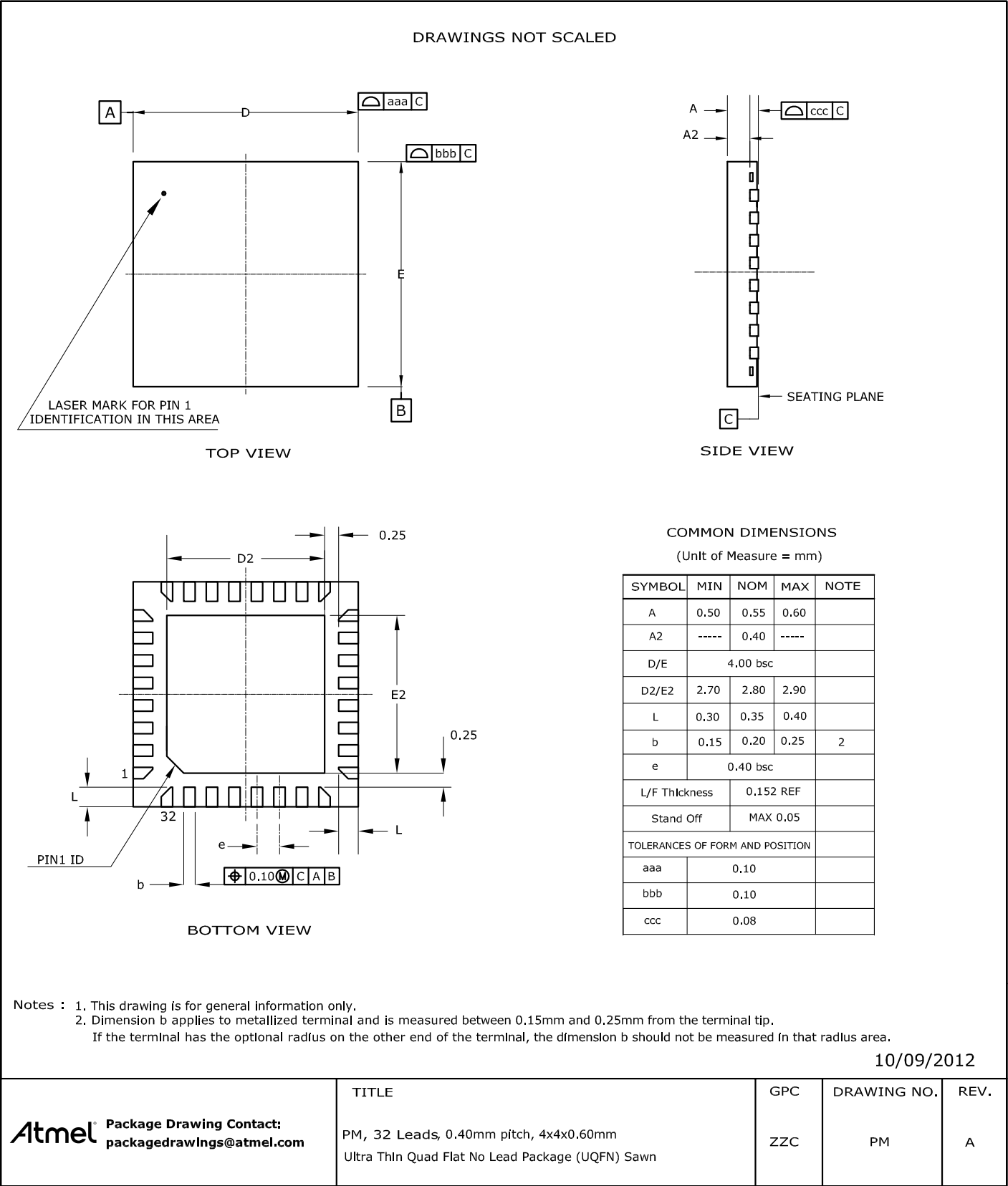


Table 36-13. Accuracy Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
RES	Input Resolution					12	Bits
INL <sup>(1)</sup>	Integral non-linearity	$V_{REF} = \text{Ext } 1.0V$	$V_{CC} = 1.6V$		$\pm 2.0$	$\pm 3$	lsb
			$V_{CC} = 3.6V$		$\pm 1.5$	$\pm 2.5$	
		$V_{REF} = AV_{CC}$	$V_{CC} = 1.6V$		$\pm 2.0$	$\pm 4$	
			$V_{CC} = 3.6V$		$\pm 1.5$	$\pm 4$	
		$V_{REF} = \text{INT}1V$	$V_{CC} = 1.6V$		$\pm 5.0$		
			$V_{CC} = 3.6V$		$\pm 5.0$		
DNL <sup>(1)</sup>	Differential non-linearity	$V_{REF} = \text{Ext } 1.0V$	$V_{CC} = 1.6V$		$\pm 1.5$	3	
			$V_{CC} = 3.6V$		$\pm 0.6$	1.5	
		$V_{REF} = AV_{CC}$	$V_{CC} = 1.6V$		$\pm 1.0$	3.5	
			$V_{CC} = 3.6V$		$\pm 0.6$	1.5	
		$V_{REF} = \text{INT}1V$	$V_{CC} = 1.6V$		$\pm 4.5$		
			$V_{CC} = 3.6V$		$\pm 4.5$		
	Gain error	After calibration			<4		mV/K
	Gain calibration step size				4		
	Gain calibration drift	$V_{REF} = \text{Ext } 1.0V$			<0.2		
	Offset error	After calibration			<1		lsb
	Offset calibration step size				1		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

## 36.8 Analog Comparator Characteristics

Table 36-14. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{off}$	Input offset voltage			10		mV
$I_{lk}$	Input leakage current			<10	50	nA
	Input voltage range		-0.1		$AV_{CC}$	V
	AC startup time			50		$\mu s$
$V_{hys1}$	Hysteresis, none	$V_{CC} = 1.6V - 3.6V$		0		mV
$V_{hys2}$	Hysteresis, small	$V_{CC} = 1.6V - 3.6V$		12		
$V_{hys3}$	Hysteresis, large	$V_{CC} = 1.6V - 3.6V$		28		
$t_{delay}$	Propagation delay	$V_{CC} = 3.0V, T = 85^{\circ}C$		22	30	ns
		$V_{CC} = 1.6V - 3.6V$		21	40	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	64-Level Voltage Scaler Integral non-linearity (INL)			0.3	0.5	lsb
	Current source accuracy after calibration			5		%
	Current source calibration range	Single mode	4		6	$\mu\text{A}$
	Current source calibration range	Double mode	8		12	

## 36.9 Bandgap and Internal 1.0V Reference Characteristics

Table 36-15. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC	1 Clk <sub>PER</sub> + 2.5 $\mu\text{s}$			$\mu\text{s}$
		As input voltage to ADC and AC		1.5		
BANDGAP	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference for ADC and DAC	T= 25°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Calibrated at T= 25°C		$\pm 3$		

### 36.9.1 Brownout Detection Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{\text{BOT}}$	BOD level 0 falling $V_{\text{CC}}$		1.50	1.65	1.75	V
	BOD level 1 falling $V_{\text{CC}}$			1.8		
	BOD level 2 falling $V_{\text{CC}}$			2.0		
	BOD level 3 falling $V_{\text{CC}}$			2.2		
	BOD level 4 falling $V_{\text{CC}}$			2.4		
	BOD level 5 falling $V_{\text{CC}}$			2.6		
	BOD level 6 falling $V_{\text{CC}}$			2.8		
	BOD level 7 falling $V_{\text{CC}}$			3.0		
$T_{\text{BOD}}$	Detection time	Continuous mode		0.4		$\mu\text{s}$
		Sampled mode		1.0		ms
$V_{\text{HYST}}$	Hysteresis	BOD level 0 - 7. Min value measured at BOD level 0		1.0		%

## 36.14 SPI Characteristics

Figure 36-5. SPI Timing Requirements in Master Mode

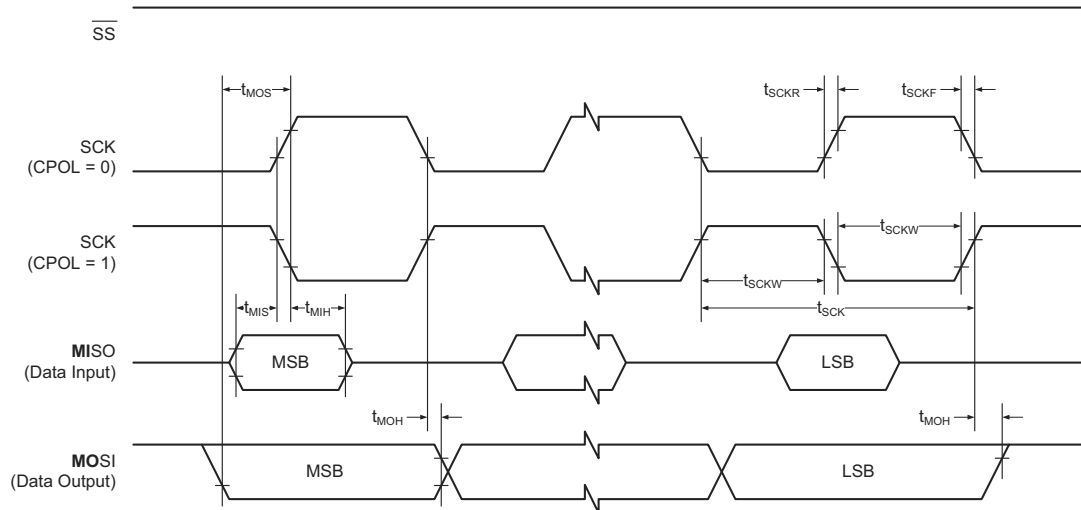
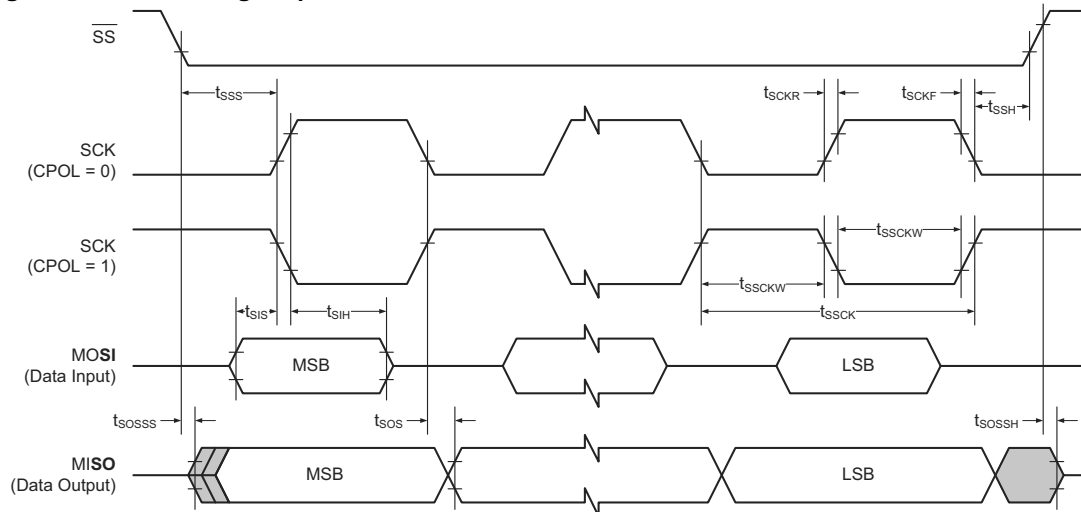
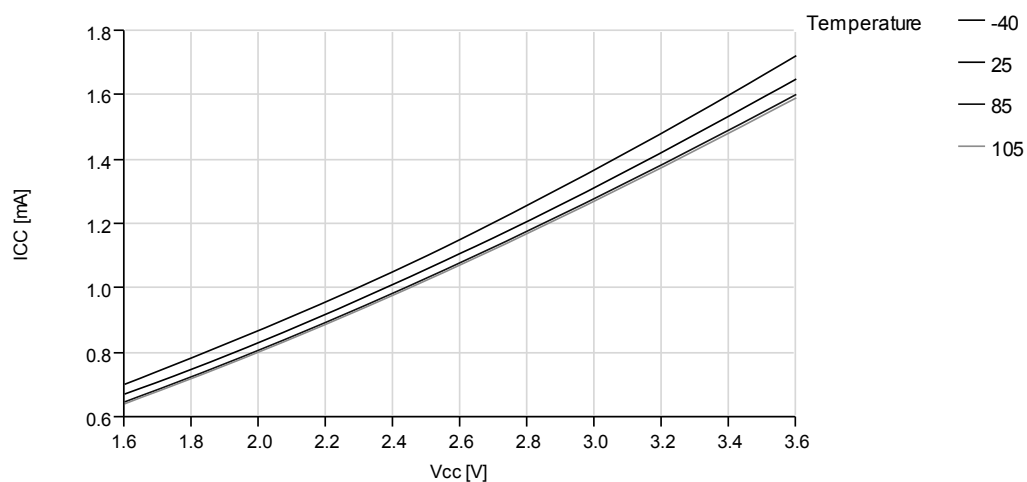


Figure 36-6. SPI Timing Requirements in Slave Mode



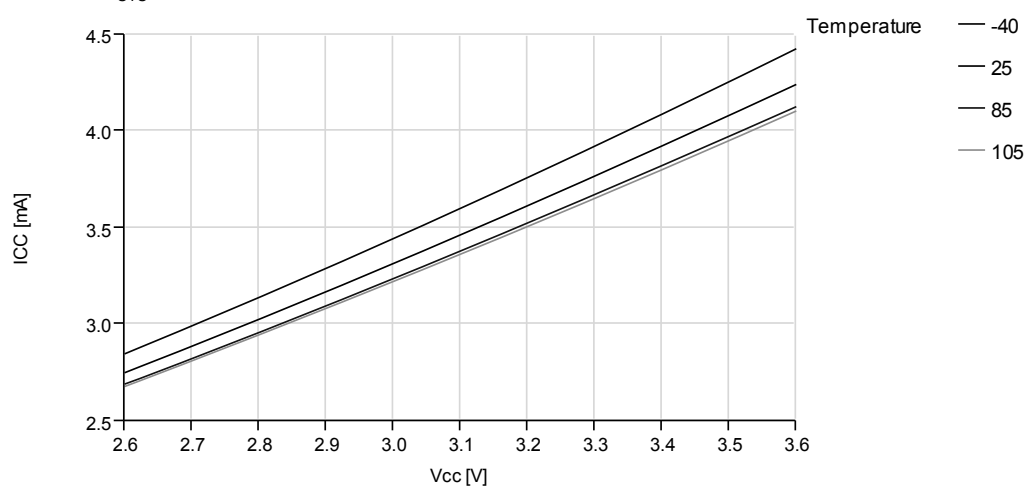
**Figure 37-15. Idle Mode Supply Current vs.  $V_{CC}$**

$f_{SYS} = 32\text{MHz}$  internal oscillator prescaled to 8MHz

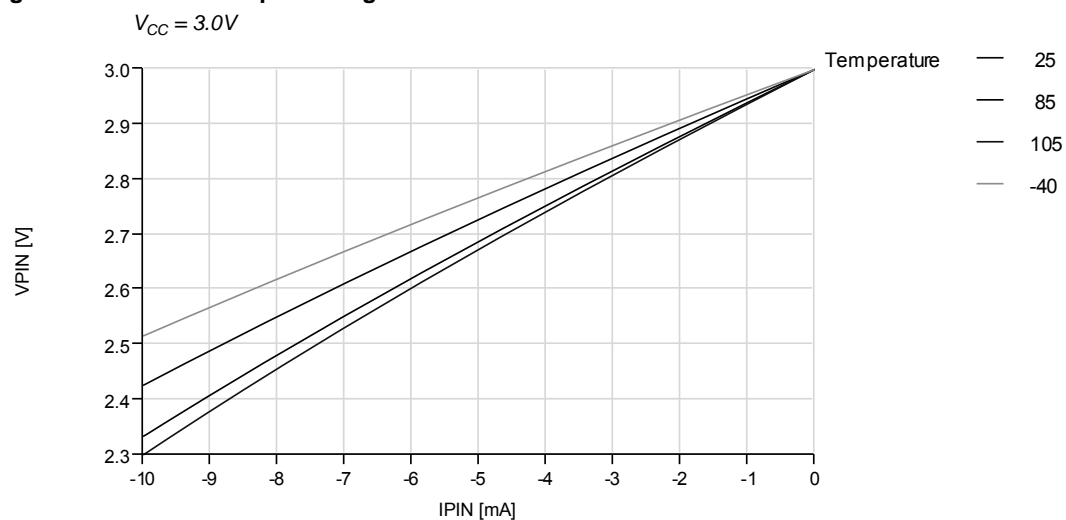


**Figure 37-16. Idle Mode Supply Current vs.  $V_{CC}$**

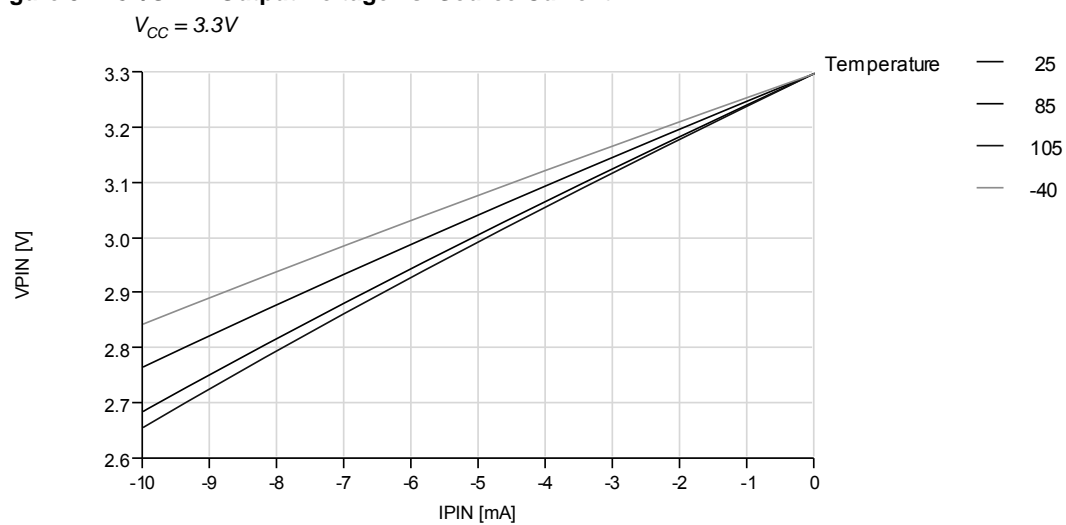
$f_{SYS} = 32\text{MHz}$  internal oscillator



**Figure 37-27. I/O Pin Output Voltage vs. Source Current**

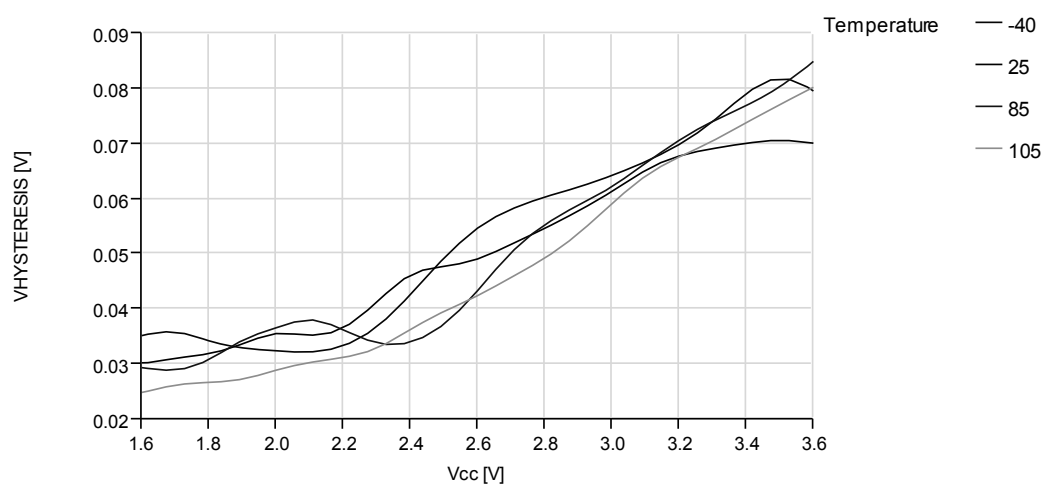


**Figure 37-28. I/O Pin Output Voltage vs. Source Current**





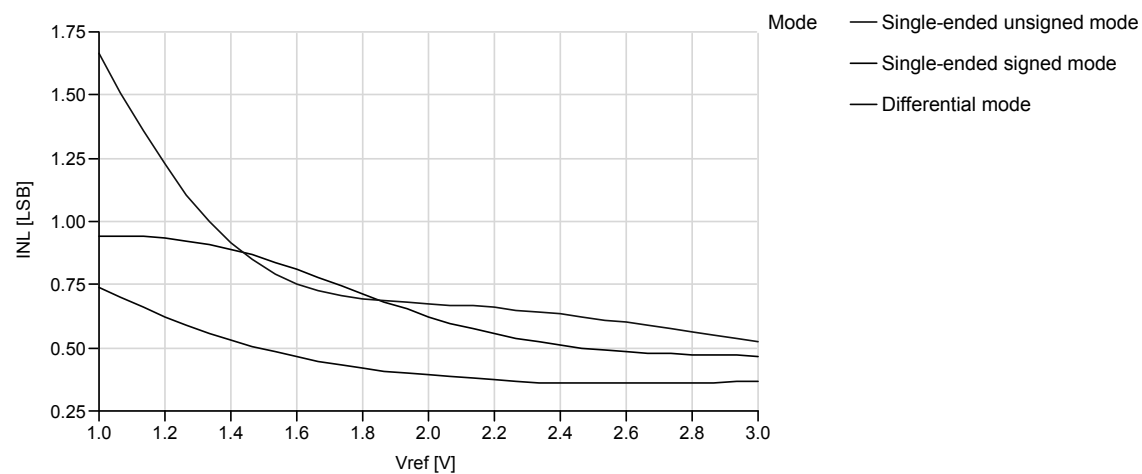
**Figure 37-37. I/O Pin Input Hysteresis vs.  $V_{CC}$**



### 37.3 ADC Characteristics

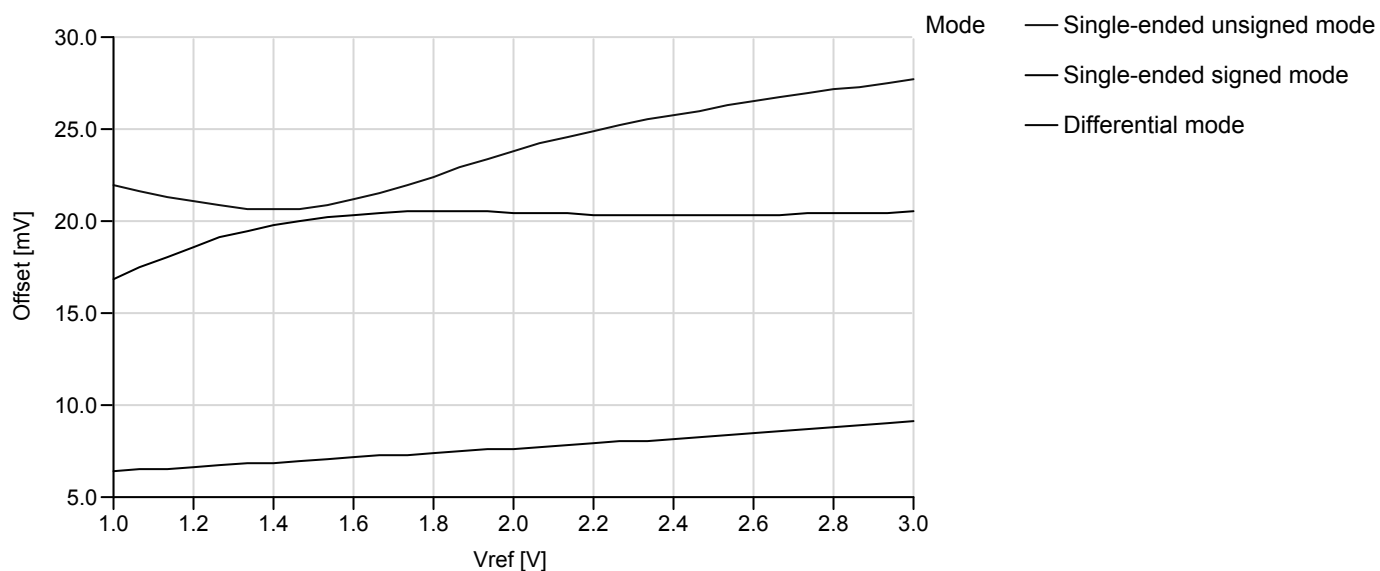
**Figure 37-38. ADC INL vs.  $V_{REF}$**

$T = 25^{\circ}\text{C}$ ,  $V_{CC} = 3.6\text{V}$ , external reference



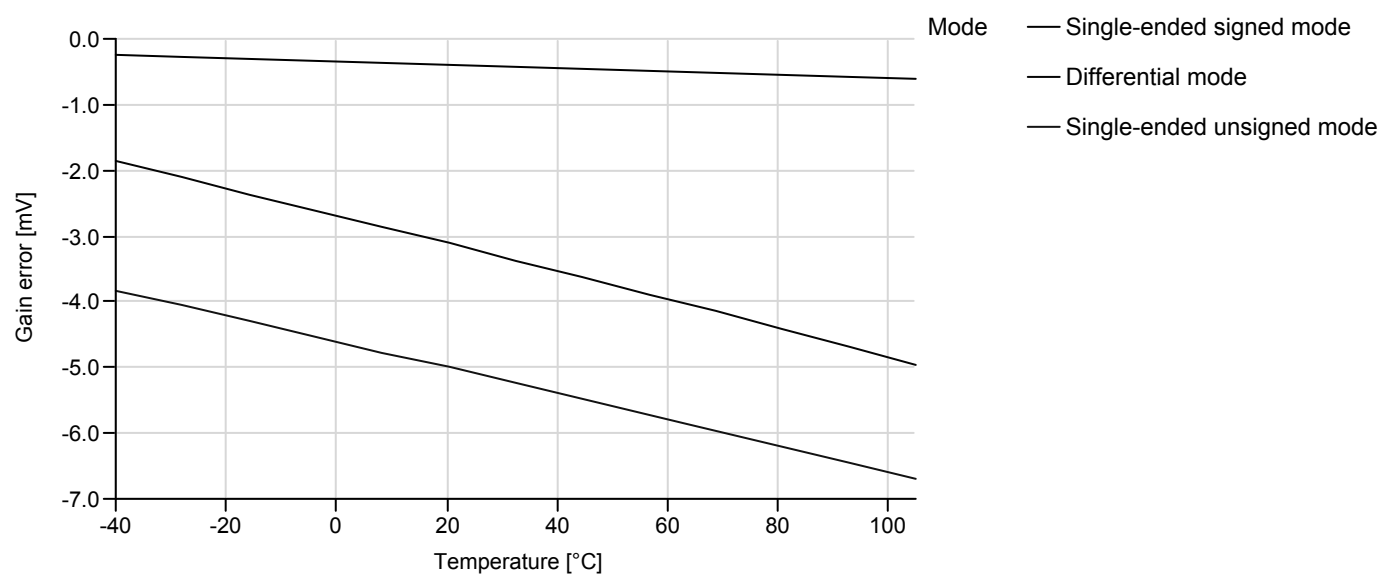
**Figure 37-45. ADC Offset Error vs.  $V_{REF}$**

$T = 25^{\circ}\text{C}$ ,  $V_{CC} = 3.6\text{V}$ , ADC sample rate = 300kps

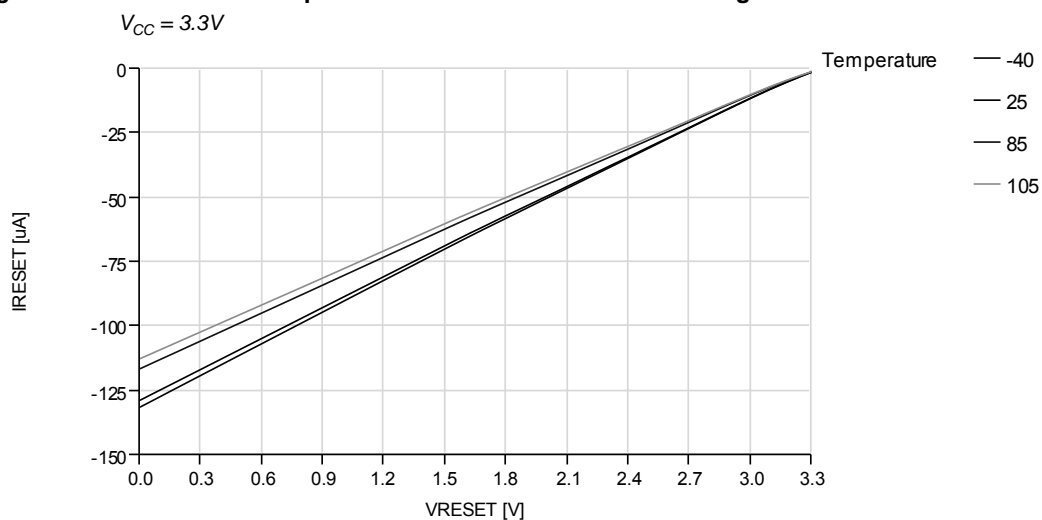


**Figure 37-46. ADC Gain Error vs. Temperature**

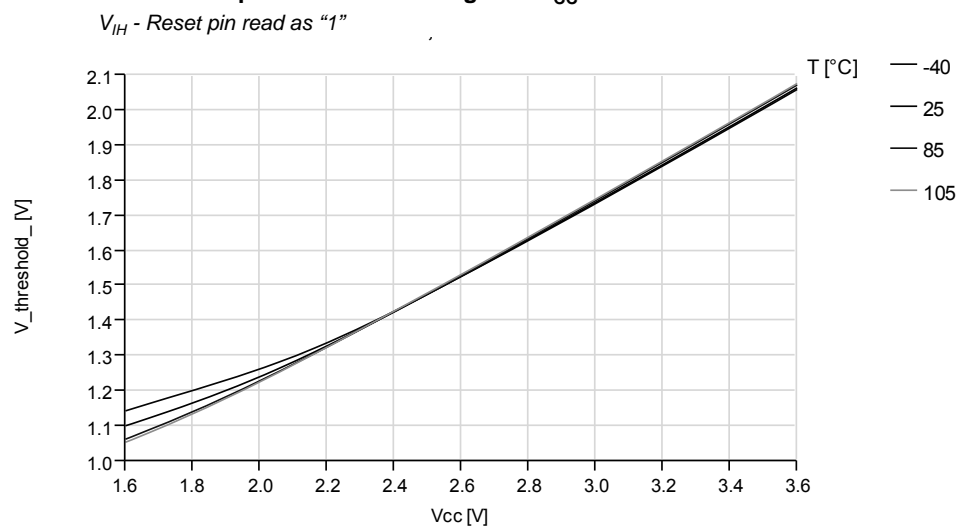
$V_{CC} = 3.6\text{V}$ ,  $V_{REF} = \text{external } 1.0\text{V}$ , sample rate = 300kps



**Figure 37-65. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage**



**Figure 37-66. Reset Pin Input Threshold Voltage vs.  $V_{CC}$**



37.10.4 32MHz Internal Oscillator

Figure 37-78. 32MHz Internal Oscillator Frequency vs. Temperature

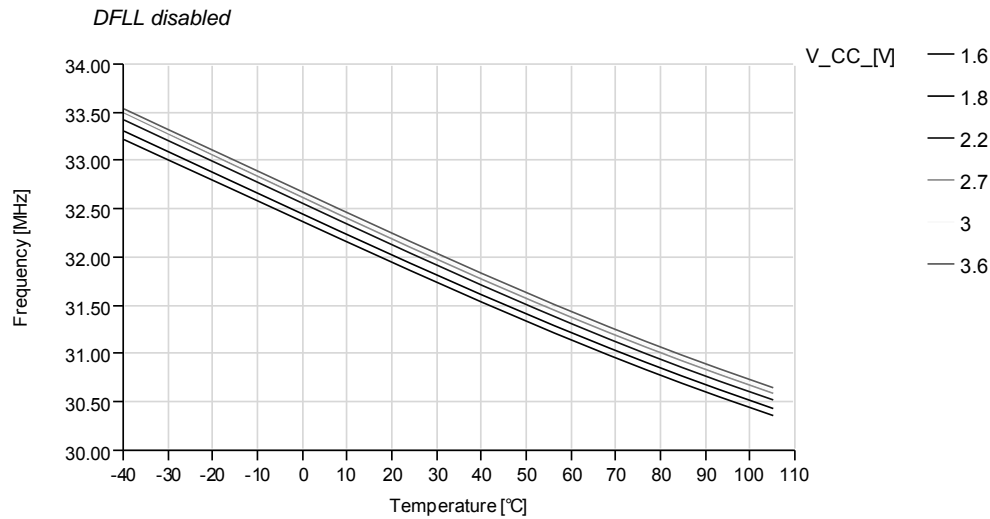
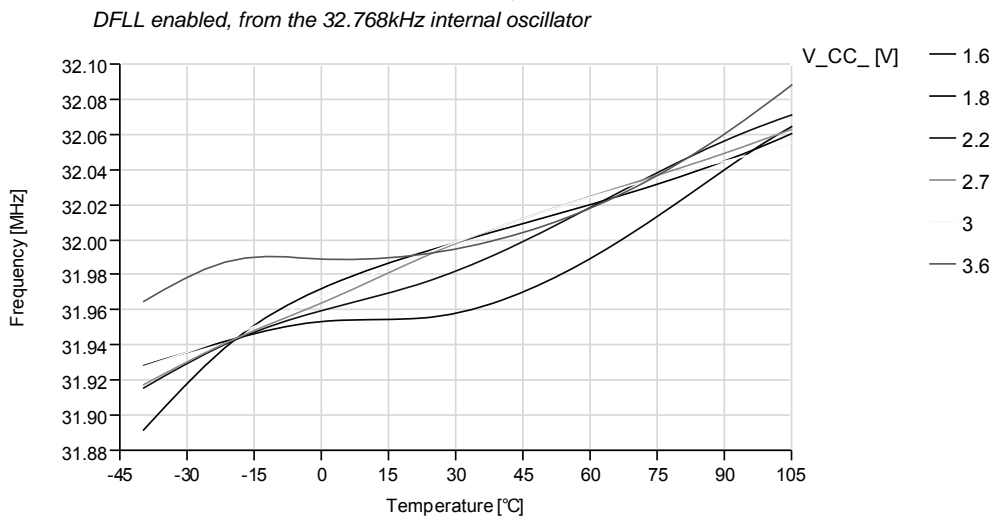
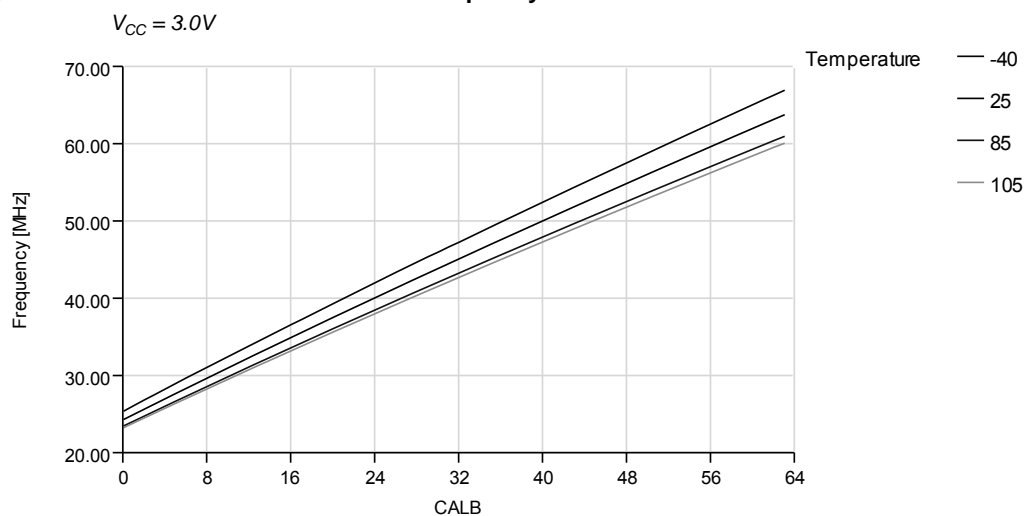


Figure 37-79. 32MHz Internal Oscillator Frequency vs. Temperature



**Figure 37-82. 32MHz internal Oscillator Frequency vs. CALB Calibration Value**



### 37.11 Two-wire Interface Characteristics

**Figure 37-83. SDA Fall Time vs. Temperature**

