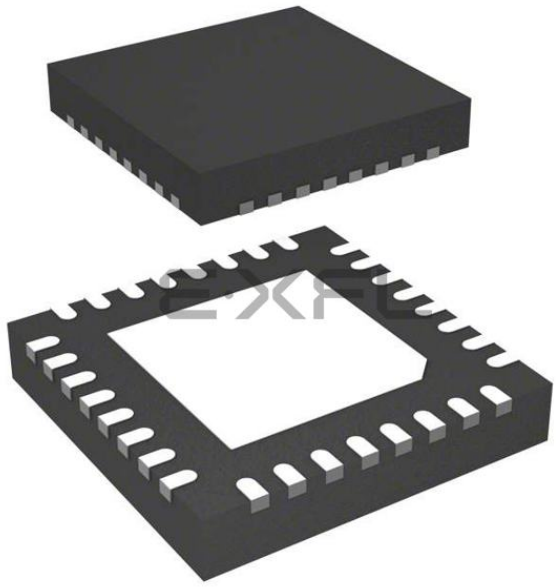


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

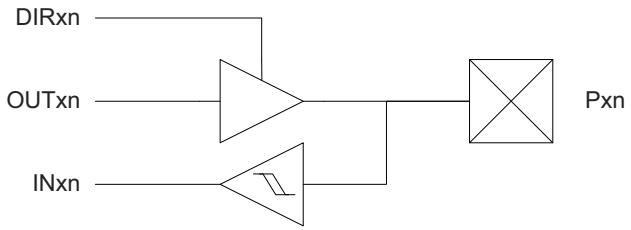
Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega8e5-m4n

16.3 Output Driver

All port pins (Pxn) have programmable output configuration. The port pins also have configurable slew rate limitation to reduce electromagnetic emission.

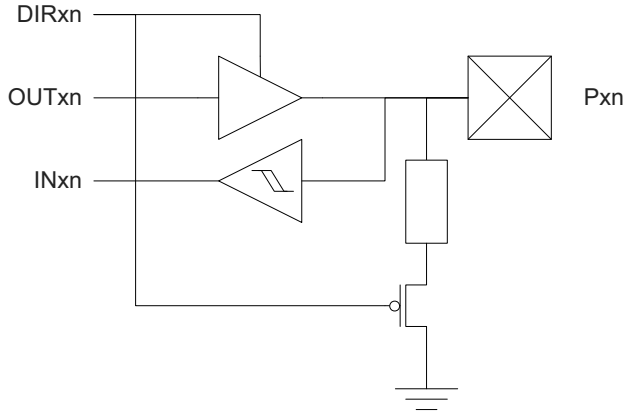
16.3.1 Push-pull

Figure 16-1. I/O Configuration - Totem-pole



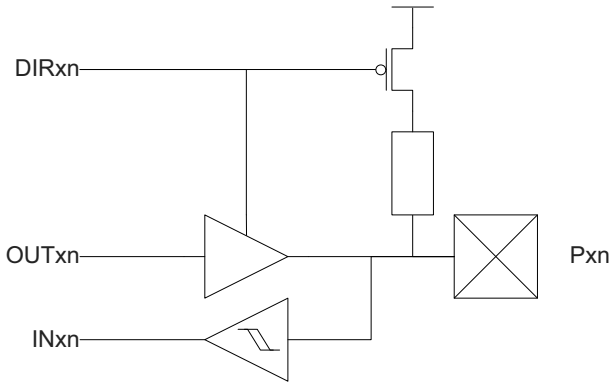
16.3.2 Pull-down

Figure 16-2. I/O Configuration - Totem-pole with Pull-down (on input)



16.3.3 Pull-up

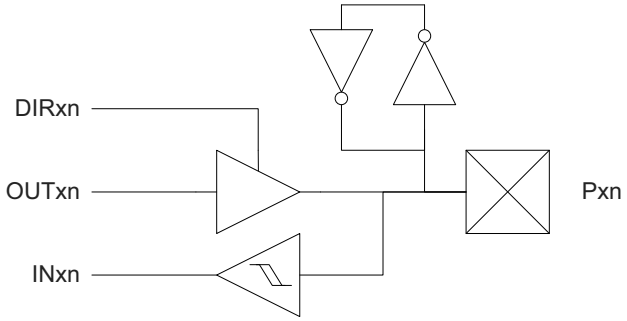
Figure 16-3. I/O Configuration - Totem-pole with Pull-up (on input)



16.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 16-4. I/O Configuration - Totem-pole with Bus-keeper



16.3.5 Others

Figure 16-5. Output Configuration - Wired-OR with Optional Pull-down

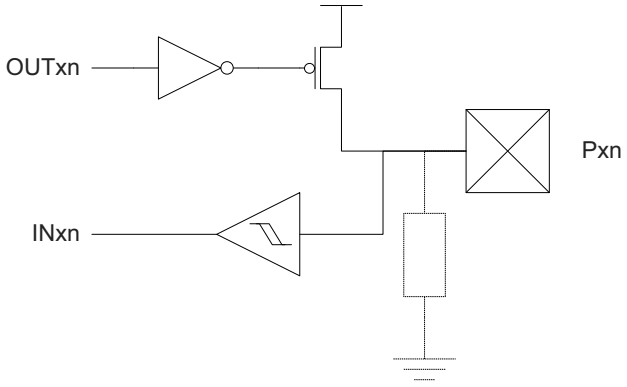


Figure 16-6. I/O Configuration - Wired-AND with Optional Pull-up

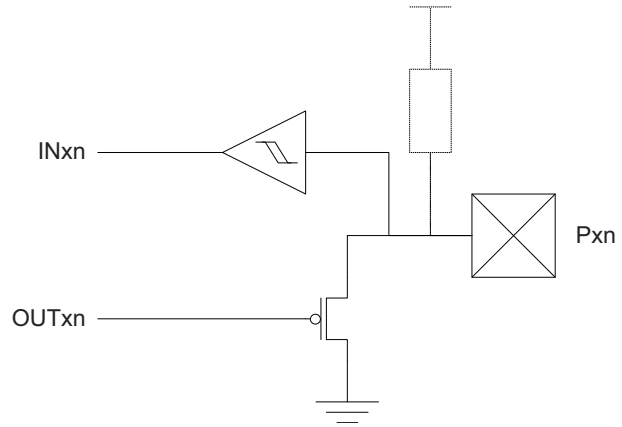
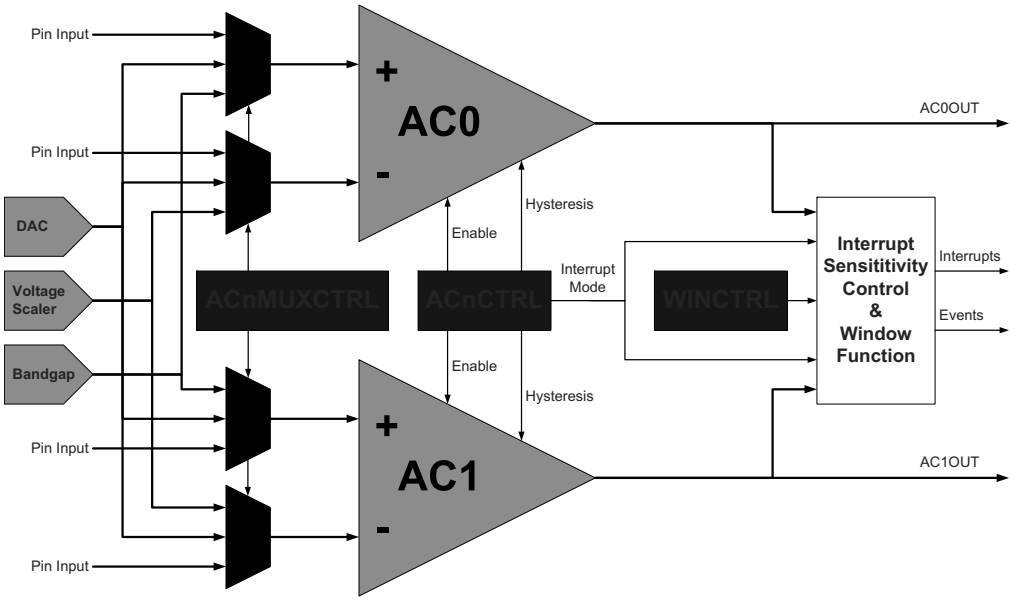
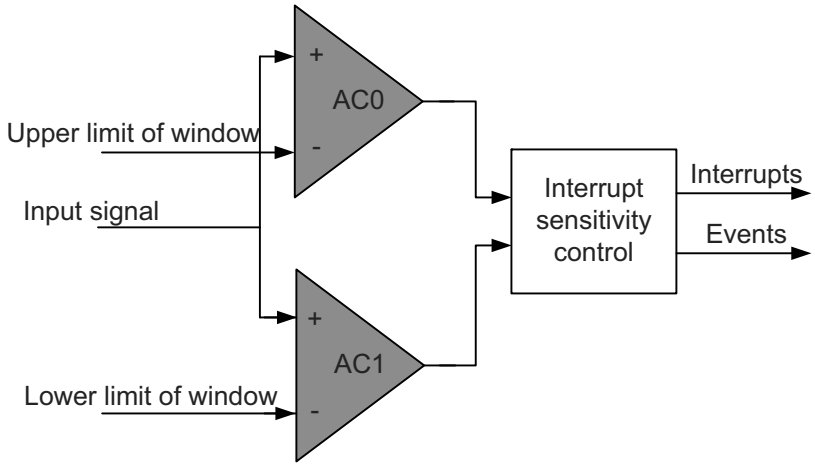


Figure 30-1. Analog Comparator Overview



The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 30-2.

Figure 30-2. Analog Comparator Window Function



31. Programming and Debugging

31.1 Features

- Programming
  - External programming through PDI interface
    - Minimal protocol overhead for fast operation
    - Built-in error detection and handling for reliable operation
  - Boot loader support for programming through any communication interface
- Debugging
  - Nonintrusive, real-time, on-chip debug system
  - No software or hardware resources required from device except pin connection
  - Program flow control
  - Go, Stop, Reset, Step Into, Step Over, Step Out, Run-to-Cursor
  - Unlimited number of user program breakpoints
  - Unlimited number of user data breakpoints, break on:
    - Data location read, write, or both read and write
    - Data location content equal or not equal to a value
    - Data location content is greater or smaller than a value
    - Data location content is within or outside a range
  - No limitation on device clock frequency
- Program and Debug Interface (PDI)
  - Two-pin interface for external programming and debugging
  - Uses the Reset pin and a dedicated pin
  - No I/O pins required during programming or debugging

31.2 Overview

The Program and Debug Interface (PDI) is an Atmel proprietary interface for external programming and on-chip debugging of a device. The PDI supports fast programming of nonvolatile memory (NVM) spaces; flash, EEPOM, fuses, lock bits, and the user signature row.

Debug is supported through an on-chip debug system that offers nonintrusive, real-time debug. It does not require any software or hardware resources except for the device pin connection. Using the Atmel tool chain, it offers complete program flow control and support for an unlimited number of program and complex data breakpoints. Application debug can be done from a C or other high-level language source code level, as well as from an assembler and disassemble level.

Programming and debugging can be done through the PDI physical layer. This is a two-pin interface that uses the Reset pin for the clock input (PDI_CLK) and one other dedicated pin for data input and output (PDI_DATA). Any external programmer or on-chip debugger/emulator can be directly connected to this interface.

XCKn	Transfer Clock for USART n
RXDn	Receiver Data for USART n
TXDn	Transmitter Data for USART n
SS	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI

32.1.6 Oscillators, Clock, and Event

TOSCn	Timer Oscillator pin n
XTALn	Input/Output for Oscillator pin n
CLKOUT	Peripheral Clock Output
EVOUT	Event Channel Output
RTCOUT	RTC Clock Source Output

32.1.7 Debug/System Functions

RESET	Reset pin
PDI_CLK	Program and Debug Interface Clock pin
PDI_DATA	Program and Debug Interface Data pin

Base Address	Name	Description
0x07E0	PORTR	Port R
0x0800	TCC4	Timer/Counter 4 on port C
0x0840	TCC5	Timer/Counter 5 on port C
0x0880	FAULTC4	Fault Extension on TCC4
0x0890	FAULTC5	Fault Extensionon TCC5
0x08A0	WEXC	Waveform Extension on port C
0x08B0	HIRESC	High Resolution Extension on port C
0x08C0	USARTC0	USART 0 on port C
0x08E0	SPIC	Serial Peripheral Interface on port C
0x08F8	IRCOM	Infrared Communication Module
0x0940	TCD5	Timer/Counter 5 on port D
0x09C0	USARTD0	USART 0 on port D

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2 / 3[1]
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	3[1]
CALL	k	call Subroutine	PC ← k	None	3 / 4[1]
RET		Subroutine Return	PC ← STACK	None	4 / 5[1]
RETI		Interrupt Return	PC ← STACK	I	4 / 5[1]
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) =1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data transfer instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1

37.1.2 Idle Mode Supply Current

Figure 37-9. Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

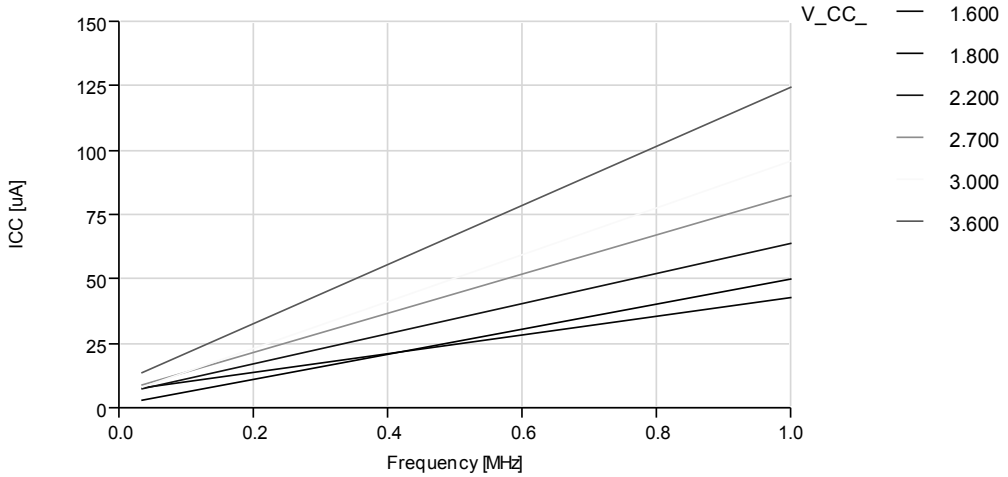
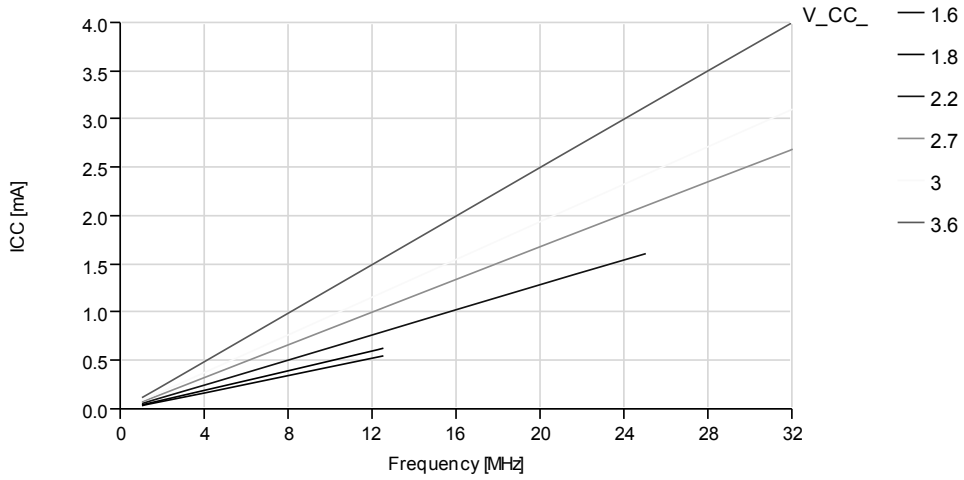


Figure 37-10.Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C



37.1.3 Power-down Mode Supply Current

Figure 37-17.Power-down Mode Supply Current vs. Temperature

All functions disabled

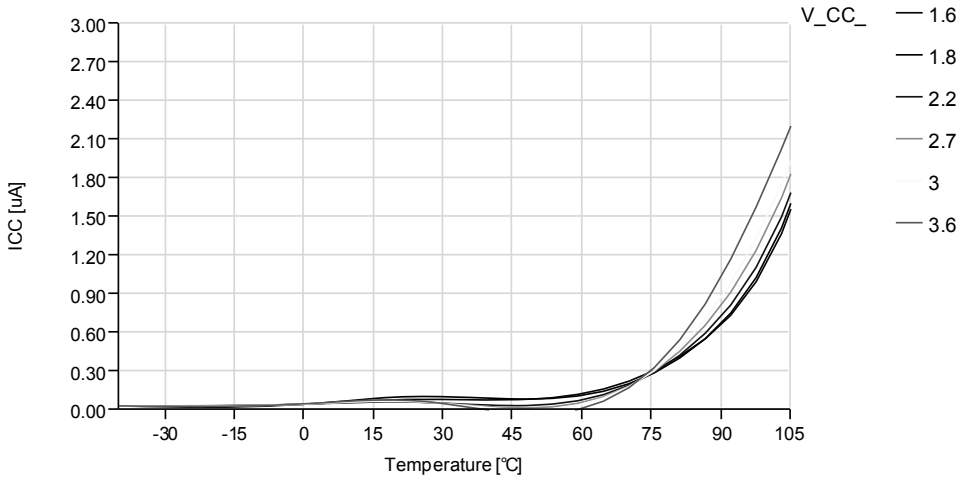


Figure 37-18.Power-down Mode supply Current vs. V_{CC}

All functions disabled

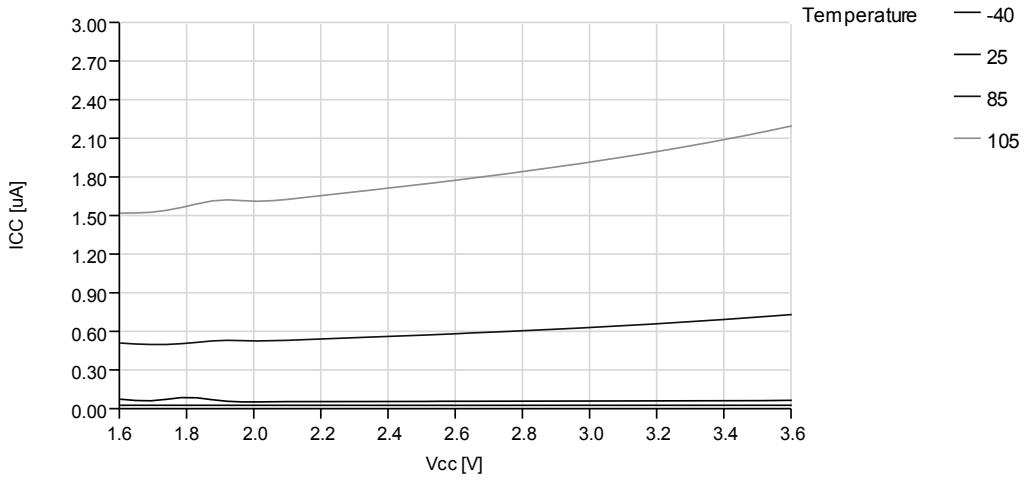
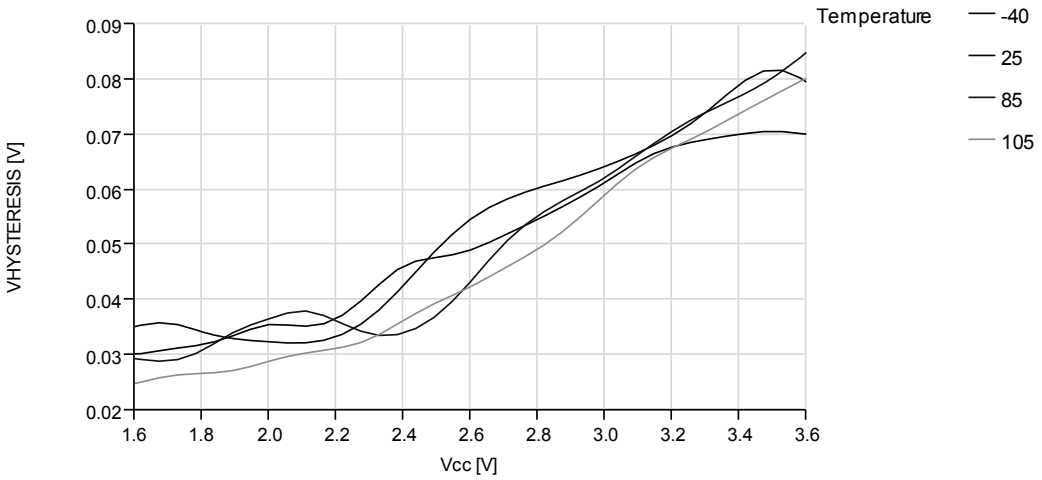


Figure 37-37.I/O Pin Input Hysteresis vs. V_{CC}



37.3 ADC Characteristics

Figure 37-38.ADC INL vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

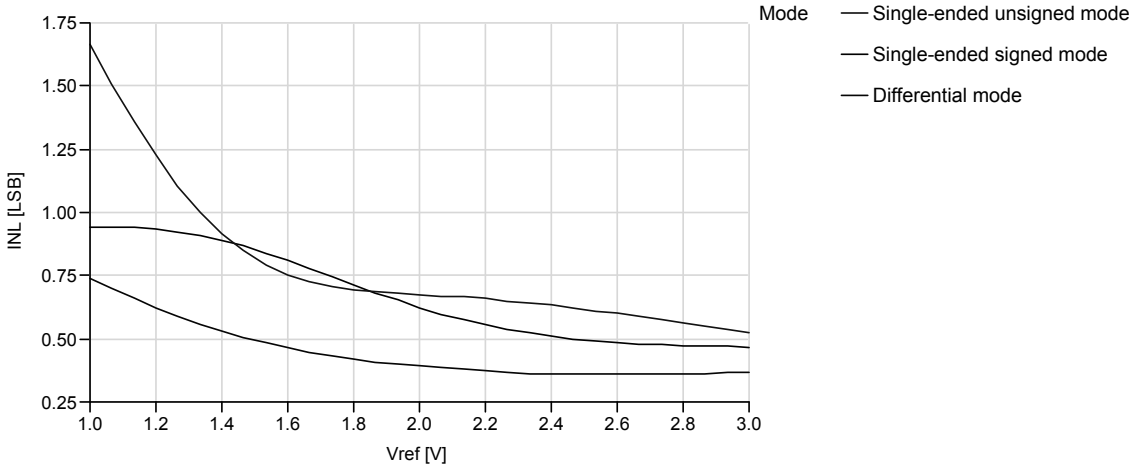


Figure 37-41. ADC Gain Error vs. V_{CC}

T = 25°C, V_{REF} = 1.0V, ADC sample rate = 300ksps

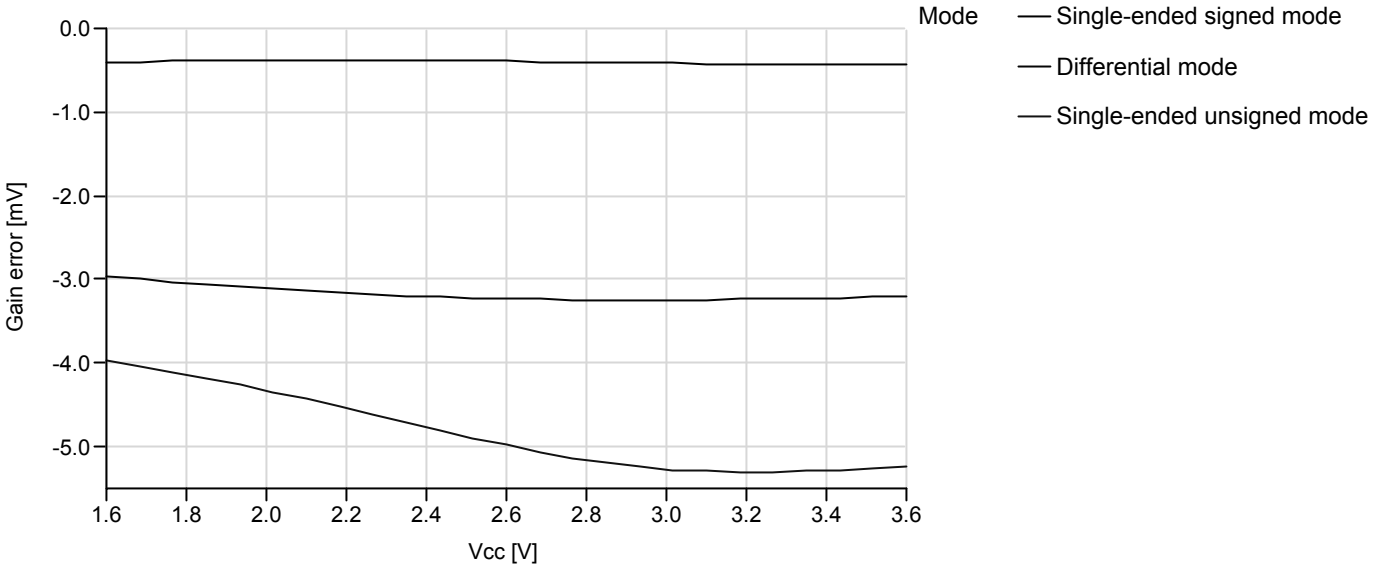


Figure 37-42. ADC Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

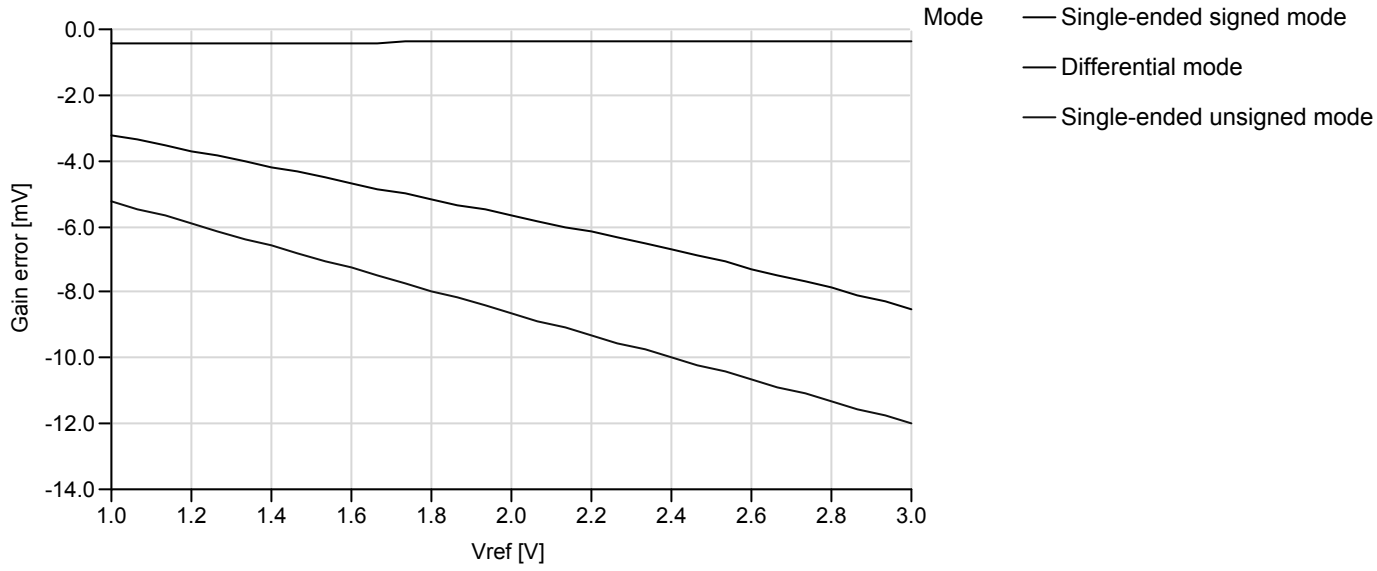


Figure 37-45. ADC Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

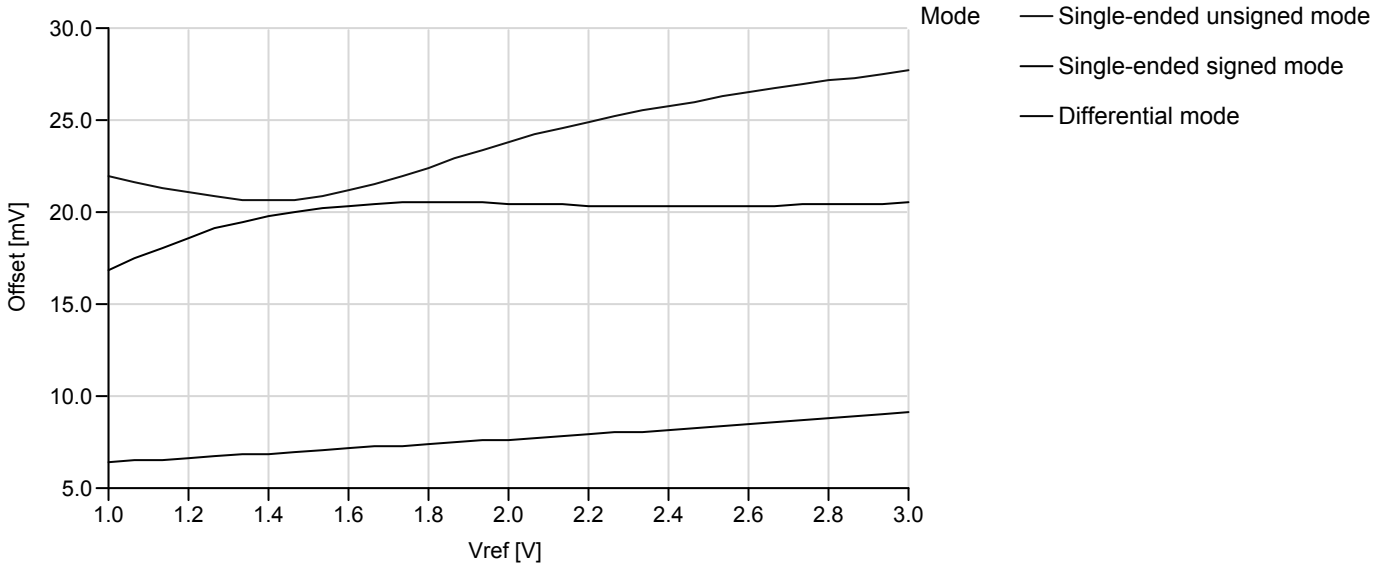
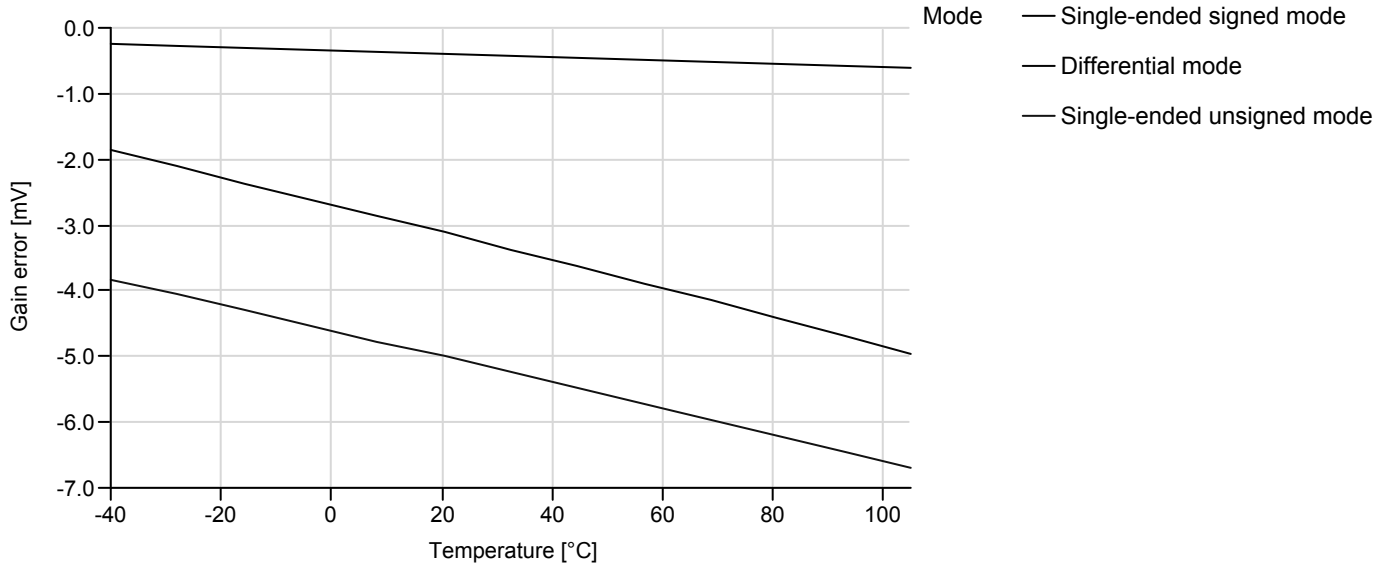


Figure 37-46.ADC Gain Error vs. Temperature

V_{CC} = 3.6V, V_{REF} = external 1.0V, sample rate = 300ksps



37.4 DAC Characteristics

Figure 37-47.DAC INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V

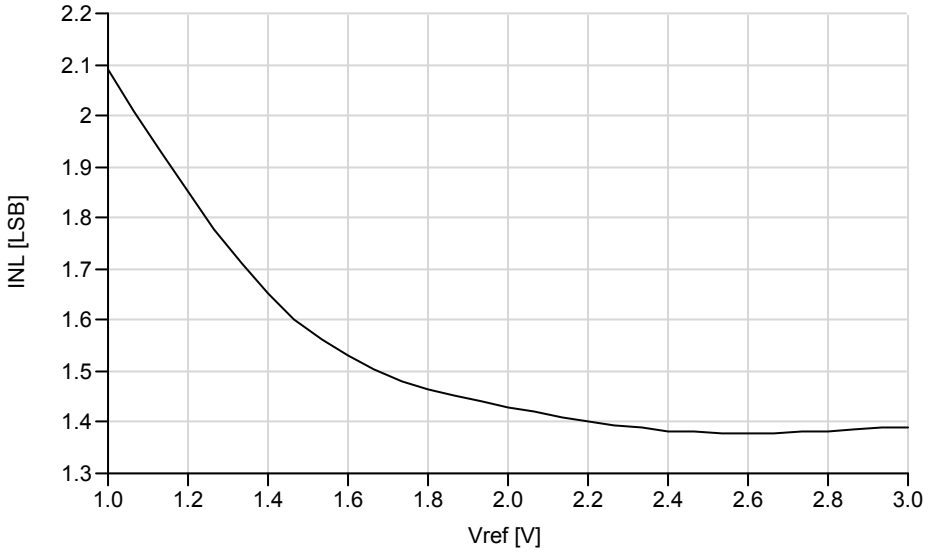


Figure 37-48.DNL Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V

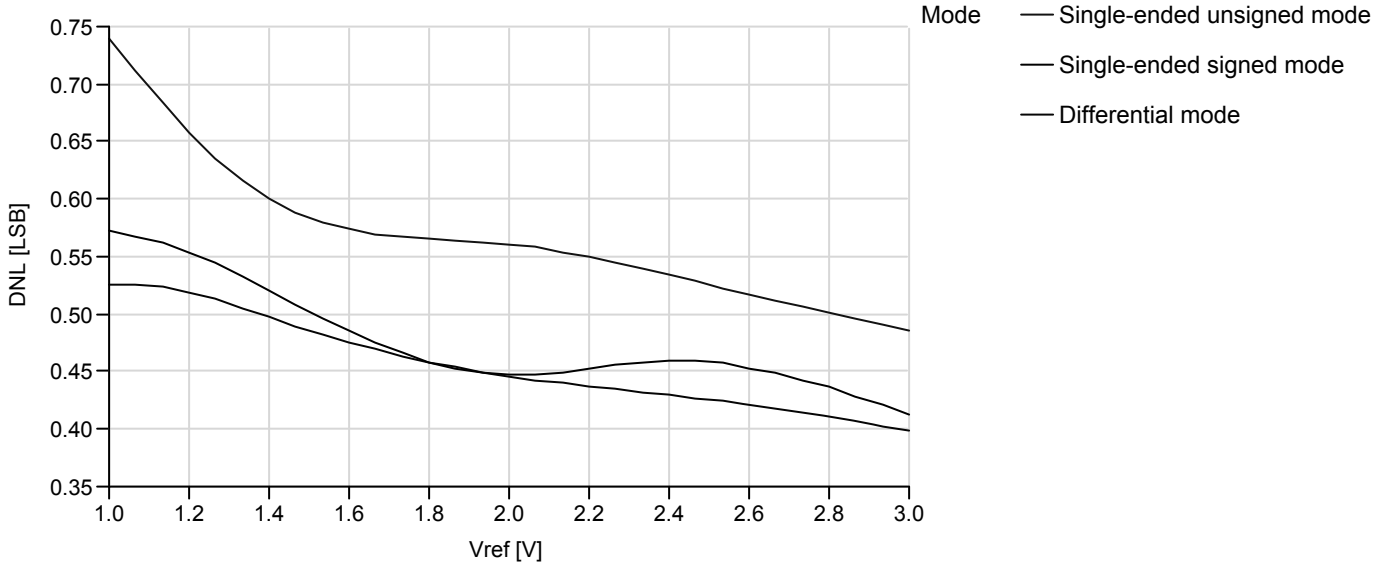
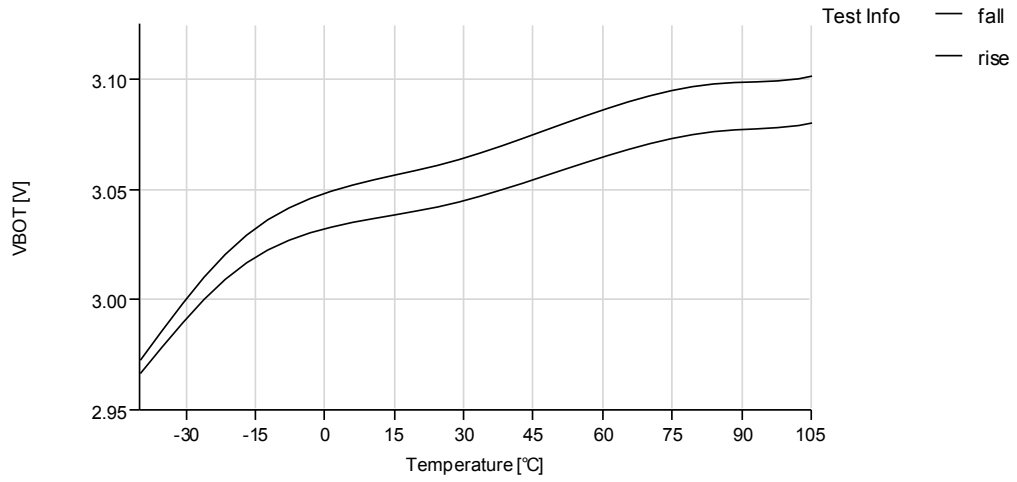


Figure 37-61.BOD Thresholds vs. Temperature

BOD level = 3.0V



37.8 External Reset Characteristics

Figure 37-62.Minimum Reset Pin Pulse Width vs. V_{CC}

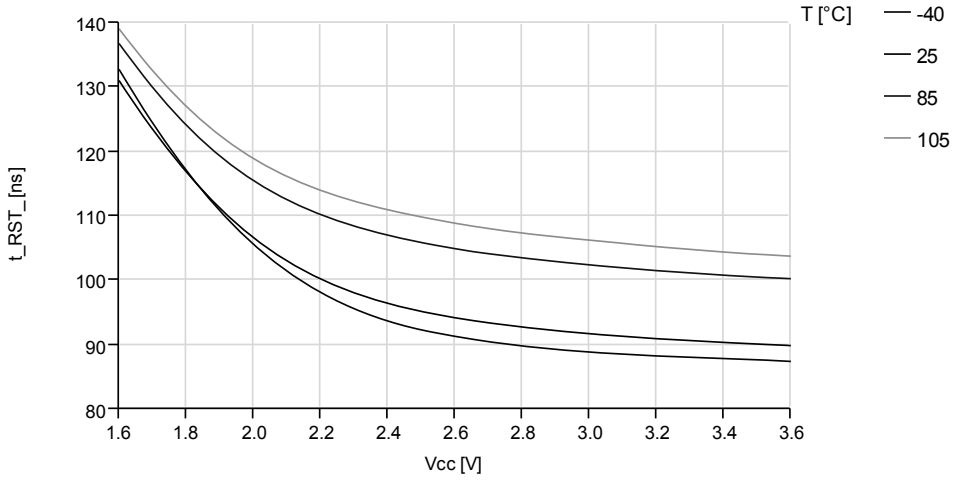


Figure 37-63.Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

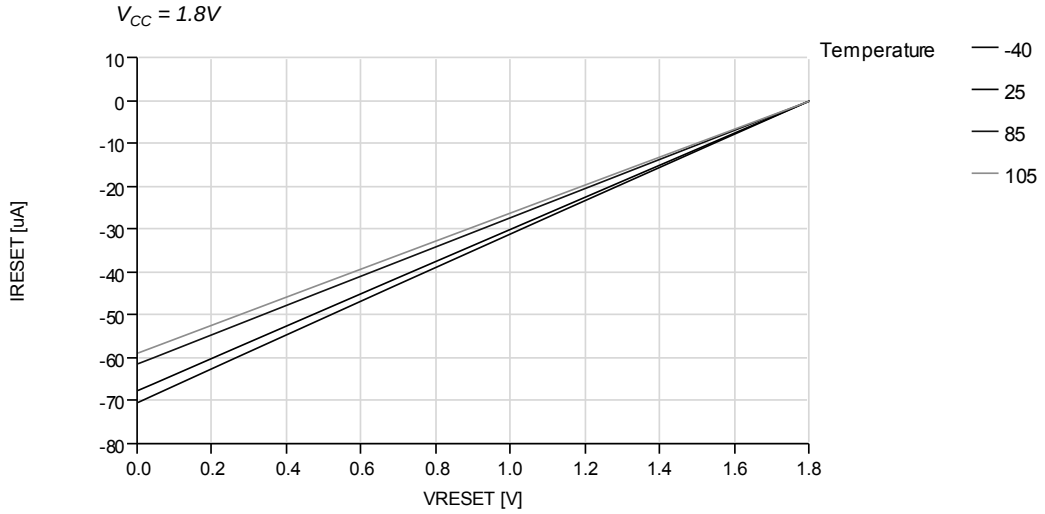


Figure 37-64.Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

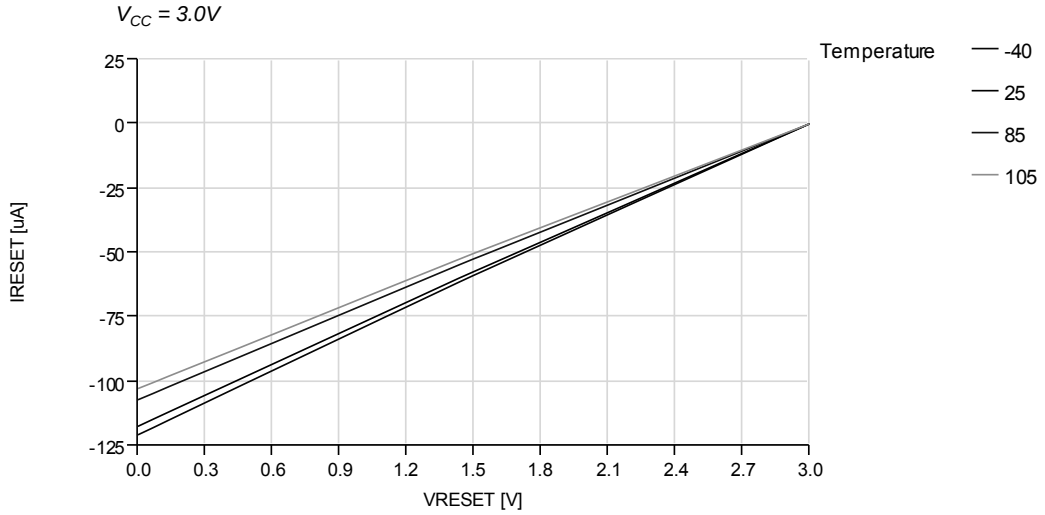


Figure 37-65.Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

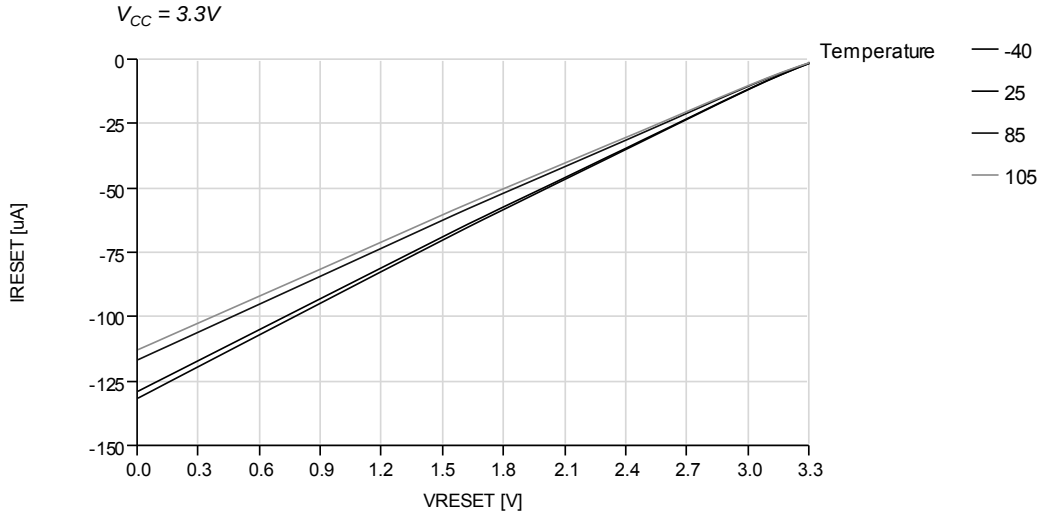


Figure 37-66.Reset Pin Input Threshold Voltage vs. V_{CC}

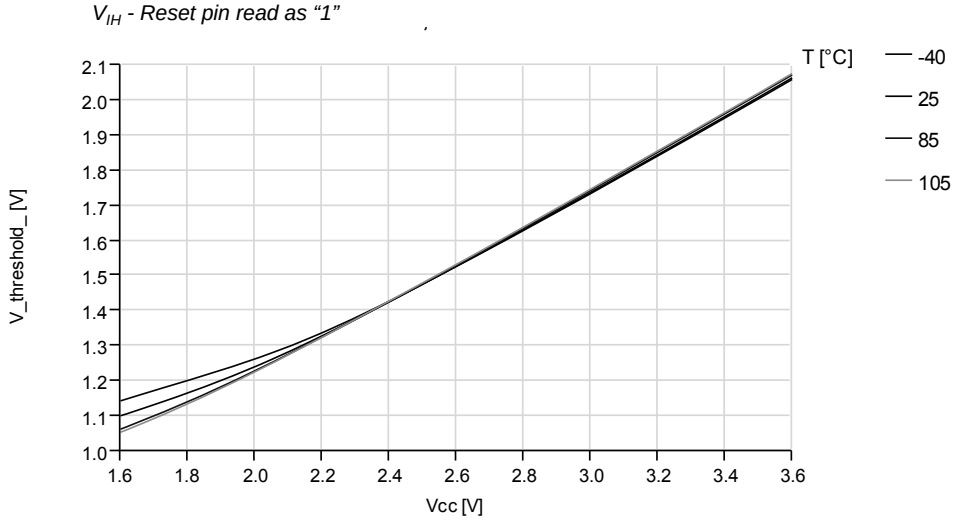


Figure 37-80. 32MHz Internal Oscillator CALA Calibration Step Size

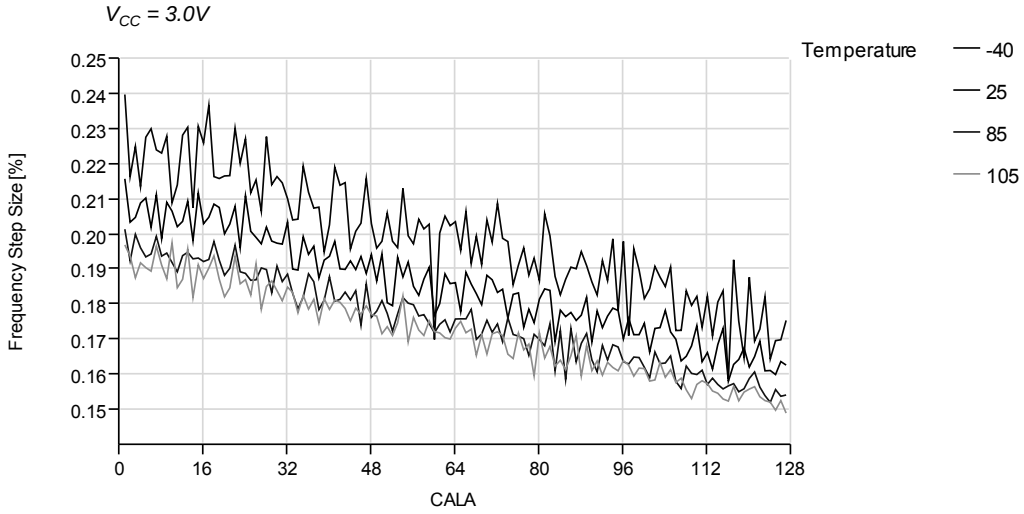
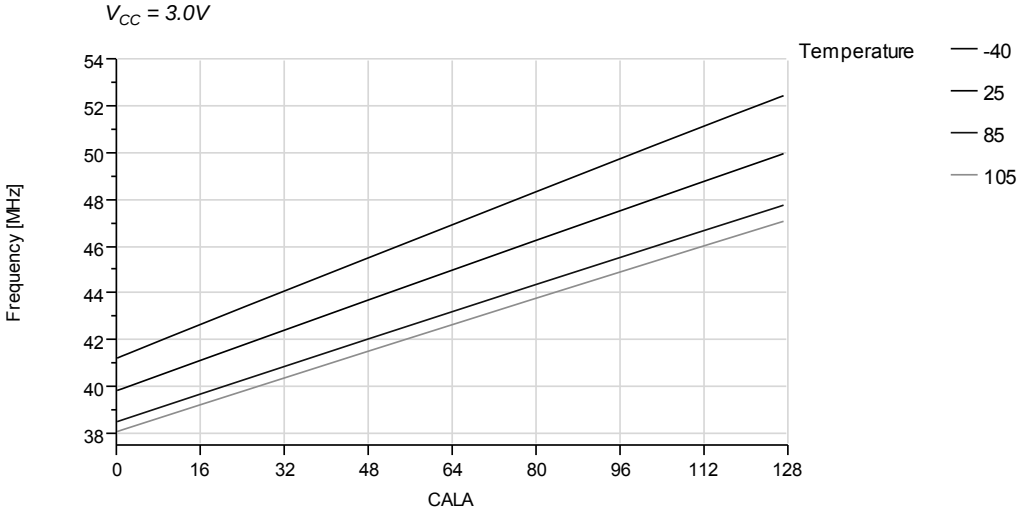


Figure 37-81. 32MHz Internal Oscillator Frequency vs. CALA Calibration Value



38.2 Rev. A

- DAC: AREF on PD0 is not available for the DAC
- EDMA: Channel transfer never stops when double buffering is enabled on sub-sequent channels
- ADC: Offset correction fails in unsigned mode
- ADC: Averaging is failing when channel scan is enabled
- ADC: Averaging in single conversion requires multiple conversion triggers
- ADC accumulator sign extends the result in unsigned mode averaging
- ADC: Free running average mode issue
- ADC: Event triggered conversion in averaging mode
- AC: Flag can not be cleared if the module is not enabled
- USART: Receiver not functional when variable data length and start frame detector are enabled
- T/C: Counter does not start when CLKSEL is written
- EEPROM write and Flash write operations fails under 2.0V
- TWI master or slave remembering data
- Temperature Sensor not calibrated

Issue: DAC: AREF on PD0 is not available for the DAC

The AREF external reference input on pin PD0 is not available for the DAC.

Workaround:

No workaround. Only AREF on pin PA0 can be used as external reference input for the DAC.

Issue: EDMA: Channel transfer never stops when double buffering is enabled on sub-sequent channels

When the double buffering is enabled on two channels, the channels which are not set in double buffering mode are never disabled at the end of the transfer. A new transfer can start if the channel is not disabled by software.

Workaround:

- CHMODE = 00

  Enable double buffering on all channels or do not use channels which are not set the double buffering mode.
- CHMODE = 01 or 10

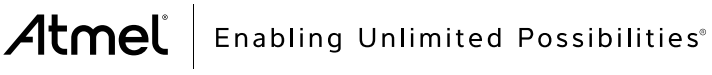
  Do not use the channel which is not supporting the double buffering mode.

Issue: ADC: Offset correction fails in unsigned mode

In single ended, unsigned mode, a problem appears in low saturation (zero) when the offset correction is activated. The offset is removed from result and when a negative result appears, the result is not correct.

Workaround:

No workaround, but avoid using this correction method to cancel ΔV effect.



Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA**T:** (+1)(408) 441.0311**F:** (+1)(408) 436.4200 **|www.atmel.com**