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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, SPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf52211cae80

1.2 Features

1.2.1 Feature Overview

The MCF52211 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
 - Static operation
 - 32-bit address and data paths on-chip
 - Up to 80 MHz processor core frequency
 - 40 MHz and 33 MHz off-platform bus frequency
 - Sixteen general-purpose, 32-bit data and address registers
 - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
 - Multiply-Accumulate (MAC) unit with 32-bit accumulator to support $16 \times 16 \rightarrow 32$ or $32 \times 32 \rightarrow 32$ operations
- System debug support
 - Real-time trace for determining dynamic execution path
 - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
 - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
 - Up to 16-Kbyte dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support
 - Up to 128 Kbytes of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
 - Fully static operation with processor sleep and whole chip stop modes
 - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
 - Clock enable/disable for each peripheral when not used (except backup watchdog timer)
 - Software controlled disable of external clock output for low-power consumption
- Universal Serial Bus On-The-Go (USB OTG) dual-mode host and device controller
 - Full-speed / low-speed host controller
 - USB 1.1 and 2.0 compliant full-speed / low speed device controller
 - 16 bidirectional end points
 - DMA or FIFO data stream interfaces
 - Low power consumption
 - OTG protocol logic
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
 - 16-bit divider for clock generation
 - Interrupt control logic with maskable interrupts
 - DMA support
 - Data formats can be 5, 6, 7 or 8 bits with even, odd, or no parity
 - Up to two stop bits in 1/16 increments
 - Error-detection capabilities
 - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
 - Transmit and receive FIFO buffers
- Two I²C modules

- Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
- Fully compatible with industry-standard I²C bus
- Master and slave modes support multiple masters
- Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
 - Full-duplex, three-wire synchronous transfers
 - Up to four chip selects available
 - Master mode operation only
 - Programmable bit rates up to half the CPU clock frequency
 - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
 - Eight analog input channels
 - 12-bit resolution
 - Minimum 1.125 μ s conversion time
 - Simultaneous sampling of two channels for motor control applications
 - Single-scan or continuous operation
 - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit
 - Unused analog channels can be used as digital I/O
- Four 32-bit timers with DMA support
 - 12.5 ns resolution at 80 MHz
 - Programmable sources for clock input, including an external clock option
 - Programmable prescaler
 - Input capture capability with programmable trigger edge on input pin
 - Output compare with programmable mode for the output pin
 - Free run and restart modes
 - Maskable interrupts on input capture or output compare
 - DMA trigger capability on input capture or output compare
- Four-channel general purpose timer
 - 16-bit architecture
 - Programmable prescaler
 - Output pulse-widths variable from microseconds to seconds
 - Single 16-bit input pulse accumulator
 - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
 - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
 - Support for PCM mode (resulting in superior signal quality compared to conventional PWM)
 - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
 - Programmable period and duty cycle
 - Programmable enable/disable for each channel
 - Software selectable polarity for each channel
 - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
 - Programmable center or left aligned outputs on individual channels
 - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
 - Emergency shutdown

Family Configurations

- Two periodic interrupt timers (PITs)
 - 16-bit counter
 - Selectable as free running or count down
- Real-Time Clock (RTC)
 - Maintains system time-of-day clock
 - Provides stopwatch and alarm interrupt functions
- Software watchdog timer
 - 32-bit counter
 - Low-power mode support
- Backup watchdog timer (BWT)
 - Independent timer that can be used to help software recover from runaway code
 - 16-bit counter
 - Low-power mode support
- Clock generation features
 - Crystal, on-chip trimmed relaxation oscillator, or external oscillator reference options
 - Trimmed relaxation oscillator
 - Pre-divider capable of dividing the clock source frequency into the PLL reference frequency range
 - System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
 - Low power modes supported
 - 2^n ($0 \leq n \leq 15$) low-power divider for extremely low frequency operation
- Interrupt controller
 - Uniquely programmable vectors for all interrupt sources
 - Fully programmable level and priority for all peripheral interrupt sources
 - Seven external interrupt signals with fixed level and priority
 - Unique vector number for each interrupt source
 - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
 - Support for hardware and software interrupt acknowledge (IACK) cycles
 - Combinatorial path to provide wake-up from low-power modes
- DMA controller
 - Four fully programmable channels
 - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
 - Source/destination address pointers that can increment or remain constant
 - 24-bit byte transfer counter per channel
 - Auto-alignment transfers supported for efficient block movement
 - Bursting and cycle-steal support
 - Software-programmable DMA requests for the UARTs (3) and 32-bit timers (4)
- Reset
 - Separate reset in and reset out signals
 - Seven sources of reset:
 - Power-on reset (POR)
 - External
 - Software
 - Watchdog
 - Loss of clock / loss of lock

Family Configurations

The full debug/trace interface is available only on the 100-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The processor supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The device implementation can:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.5 On-Chip Memories

1.2.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 8- or 16-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 8- or 16-Kbyte boundary within the 4-Gbyte address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.5.2 Flash Memory

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with up to four banks of 16-Kbyte×16-bit flash memory arrays to generate up to 128 Kbytes of 32-bit flash memory. These electrically erasable and programmable arrays serve as non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller that supports interleaved accesses from the 2-cycle flash memory arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash memory programming interface that allows the flash memory to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips.

1.2.6 Power Management

The device incorporates several low-power modes of operation entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage to the chip falls below the standby battery voltage.

Table 2 shows the pinout configuration for the 100 LQFP.

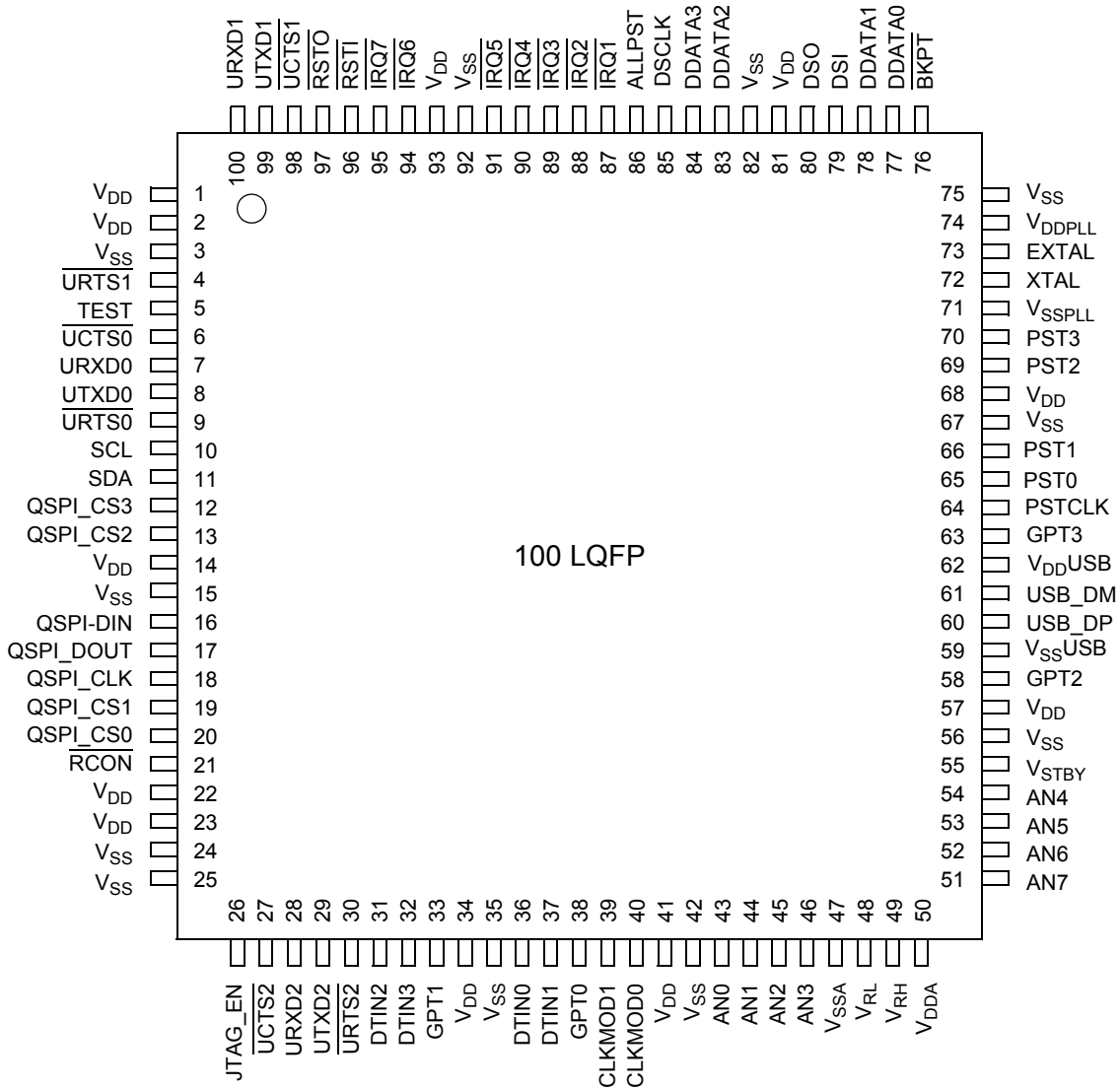


Figure 2. 100 LQFP Pin Assignments

Table 3 shows the pin functions by primary and alternate purpose, and illustrates which packages contain each pin.

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control ¹	Slew Rate / Control ¹	Pull-up / Pull-down ²	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
ADC	AN7	—	—	GPIO	Low	FAST	—	51	H9	33
	AN6	—	—	GPIO	Low	FAST	—	52	G9	34
	AN5	—	—	GPIO	Low	FAST	—	53	G8	35
	AN4	—	—	GPIO	Low	FAST	—	54	F9	36
	AN3	—	—	GPIO	Low	FAST	—	46	G7	28
	AN2	—	—	GPIO	Low	FAST	—	45	G6	27
	AN1	—	—	GPIO	Low	FAST	—	44	H6	26
	AN0	—	—	GPIO	Low	FAST	—	43	J6	25
	SYNCA ³	—	—	—	N/A	N/A	—	—	—	—
	SYNCB ³	—	—	—	N/A	N/A	—	—	—	—
	VDDA	—	—	—	N/A	N/A	—	50	H8	32
	VSSA	—	—	—	N/A	N/A	—	47	H7, J9	29
	VRH	—	—	—	N/A	N/A	—	49	J8	31
	VRL	—	—	—	N/A	N/A	—	48	J7	30
Clock Generation	EXTAL	—	—	—	N/A	N/A	—	73	B9	47
	XTAL	—	—	—	N/A	N/A	—	72	C9	46
	VDDPLL	—	—	—	N/A	N/A	—	74	B8	48
	VSSPLL	—	—	—	N/A	N/A	—	71	C8	45
Debug Data	ALLPST	—	—	—	High	FAST	—	86	A6	55
	DDATA[3:0]	—	—	GPIO	High	FAST	—	84,83,78,77	—	—
	PST[3:0]	—	—	GPIO	High	FAST	—	70,69,66,65	—	—
I ² C	SCL	USB_DMI	UTXD2	GPIO	PDSR[0]	PSRR[0]	pull-up ⁴	10	E1	8
	SDA	USB_DPI	URXD2	GPIO	PDSR[0]	PSRR[0]	pull-up ⁴	11	E2	9

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control ¹	Slew Rate / Control ¹	Pull-up / Pull-down ²	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
QSPI	QSPI_DIN/ EZPD	—	URXD1	GPIO	PDSR[2]	PSRR[2]	—	16	F3	12
	QSPI_DOUT/ EZPQ	—	UTXD1	GPIO	PDSR[1]	PSRR[1]	—	17	G1	13
	QSPI_CLK/ EZPCK	SCL	$\overline{\text{URTS1}}$	GPIO	PDSR[3]	PSRR[3]	pull-up ⁸	18	G2	14
	QSPI_CS3	SYNCA	—	GPIO	PDSR[7]	PSRR[7]	pull-up/pull-down ⁷	12	F1	—
	QSPI_CS2	—	—	GPIO	PDSR[6]	PSRR[6]	pull-up/pull-down ⁷	13	F2	—
	QSPI_CS1	—	—	GPIO	PDSR[5]	PSRR[5]	—	19	H2	—
	QSPI_CS0	SDA	$\overline{\text{UCTS1}}$	GPIO	PDSR[4]	PSRR[4]	pull-up ⁸	20	H1	15
Reset ⁹	$\overline{\text{RSTI}}$	—	—	—	N/A	N/A	pull-up ⁹	96	A3	59
	$\overline{\text{RSTO}}$	—	—	—	high	FAST	—	97	B3	60
Test	TEST	—	—	—	N/A	N/A	pull-down	5	C2	3
Timers, 16-bit	GPT3	—	PWM7	GPIO	PDSR[23]	PSRR[23]	pull-up ¹⁰	63	D7	—
	GPT2	—	PWM5	GPIO	PDSR[22]	PSRR[22]	pull-up ¹⁰	58	E8	—
	GPT1	—	PWM3	GPIO	PDSR[21]	PSRR[21]	pull-up ¹⁰	33	J4	—
	GPT0	—	PWM1	GPIO	PDSR[20]	PSRR[20]	pull-up ¹⁰	38	J5	—
Timers, 32-bit	DTIN3	DTOUT3	PWM6	GPIO	PDSR[19]	PSRR[19]	—	32	H3	19
	DTIN2	DTOUT2	PWM4	GPIO	PDSR[18]	PSRR[18]	—	31	J3	18
	DTIN1	DTOUT1	PWM2	GPIO	PDSR[17]	PSRR[17]	—	37	G4	23
	DTIN0	DTOUT0	PWM0	GPIO	PDSR[16]	PSRR[16]	—	36	H4	22
UART 0	$\overline{\text{UCTS0}}$	—	—	GPIO	PDSR[11]	PSRR[11]	—	6	C1	4
	$\overline{\text{URTS0}}$	—	—	GPIO	PDSR[10]	PSRR[10]	—	9	D3	7
	URXD0	RTC_EXTAL	—	GPIO	PDSR[9]	PSRR[9]	—	7	D1	5
	UTXD0	RTC_XTAL	—	GPIO	PDSR[8]	PSRR[8]	—	8	D2	6

Table 16. Debug Support Signals (continued)

Signal Name	Abbreviation	Function	I/O
Test Data Output	TDO	Serial output for test instructions and data. TDO is tri-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.	O
Development Serial Clock	DSCLK	Development Serial Clock - Internally synchronized input. (The logic level on DSCLK is validated if it has the same value on two consecutive rising bus clock edges.) Clocks the serial communication port to the debug module during packet transfers. Maximum frequency is PSTCLK/5. At the synchronized rising edge of DSCLK, the data input on DSI is sampled and DSO changes state.	I
Breakpoint	$\overline{\text{BKPT}}$	Breakpoint - Input used to request a manual breakpoint. Assertion of $\overline{\text{BKPT}}$ puts the processor into a halted state after the current instruction completes. Halt status is reflected on processor status/debug data signals (PST[3:0] and PSTDDATA[7:0]) as the value 0xF. If CSR[BKD] is set (disabling normal $\overline{\text{BKPT}}$ functionality), asserting $\overline{\text{BKPT}}$ generates a debug interrupt exception in the processor.	I
Development Serial Input	DSI	Development Serial Input - Internally synchronized input that provides data input for the serial communication port to the debug module, after the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output - Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock - Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, and PST and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be reenabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical AND of PST[3:0]. The CLKOUT signal can be used by the development system to know when to sample ALLPST.	O

1.16 EzPort Signal Descriptions

Table 17 contains a list of EzPort external signals.

2.3 Thermal Characteristics

Table 22 lists thermal resistance values.

Table 22. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	42 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	25 ⁴	°C/W
	Junction to case	—	θ_{JC}	9 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
81 MAPBGA	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	61 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	35 ^{2,3}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50 ^{2,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	31 ^{2,3}	°C/W
	Junction to board	—	θ_{JB}	20 ⁴	°C/W
	Junction to case	—	θ_{JC}	12 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
64 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	62 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	43 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	36 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	26 ⁴	°C/W
	Junction to case	—	θ_{JC}	9 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
64 QFN	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	68 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	24 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	55 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	19 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	8 ⁴	°C/W
	Junction to case (bottom)	—	θ_{JC}	0.6 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	3 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

Table 24. SGFM Flash Module Life Characteristics

($V_{DD} = 3.0$ to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles ¹ before failure	P/E	10,000 ²	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

¹ A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

² Reprogramming of a flash memory array block prior to erase is not required.

2.5 EzPort Electrical Specifications

Table 25. EzPort Electrical Specifications

Name	Characteristic	Min	Max	Unit
EP1	EPCK frequency of operation (all commands except READ)	—	$f_{sys} / 2$	MHz
EP1a	EPCK frequency of operation (READ command)	—	$f_{sys} / 8$	MHz
EP2	EPCS_b negation to next EPCS_b assertion	$2 \times T_{cyc}$	—	ns
EP3	EPCS_B input valid to EPCK high (setup)	5	—	ns
EP4	EPCK high to EPCS_B input invalid (hold)	5	—	ns
EP5	EPD input valid to EPCK high (setup)	2	—	ns
EP6	EPCK high to EPD input invalid (hold)	5	—	ns
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

Table 30. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

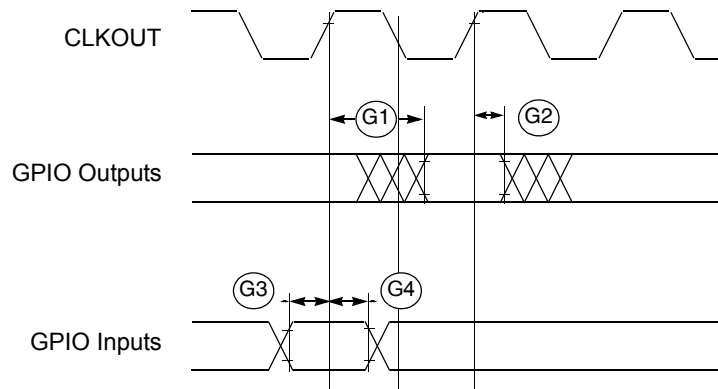


Figure 5. GPIO Timing

2.11 Reset Timing

Table 31. Reset and Configuration Override Timing

($V_{DD} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, $T_A = T_L$ to T_H)¹

NUM	Characteristic	Symbol	Min	Max	Unit
R1	\overline{RSTI} input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to \overline{RSTI} Input invalid	t_{CHRI}	1.5	—	ns
R3	\overline{RSTI} input valid time ²	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to \overline{RSTO} Valid	t_{CHROV}	—	10	ns

¹ All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

² During low power STOP, the synchronizers for the \overline{RSTI} input are bypassed and \overline{RSTI} is asserted asynchronously to the system. Thus, \overline{RSTI} must be held a minimum of 100 ns.

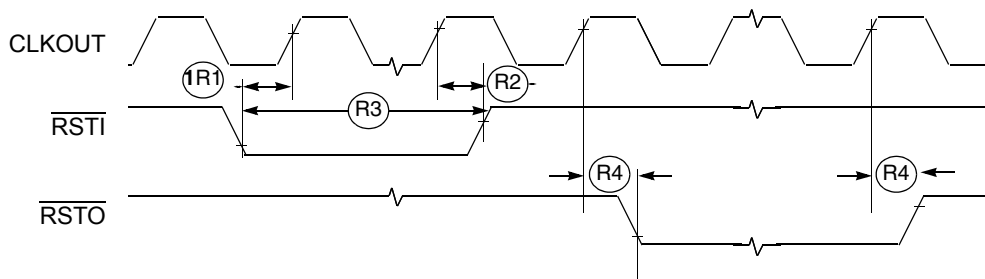


Figure 6. \overline{RSTI} and Configuration Override Timing

2.15 DMA Timers Timing Specifications

Table 35 lists timer module AC timings.

Table 35. Timer Module AC Timing Specifications

Name	Characteristic ¹	Min	Max	Unit
T1	DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time	$3 \times t_{CYC}$	—	ns
T2	DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width	$1 \times t_{CYC}$	—	ns

¹ All timing references to CLKOUT are given to its rising edge.

2.16 QSPI Electrical Specifications

Table 36 lists QSPI timings.

Table 36. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 36 correspond to Figure 9.

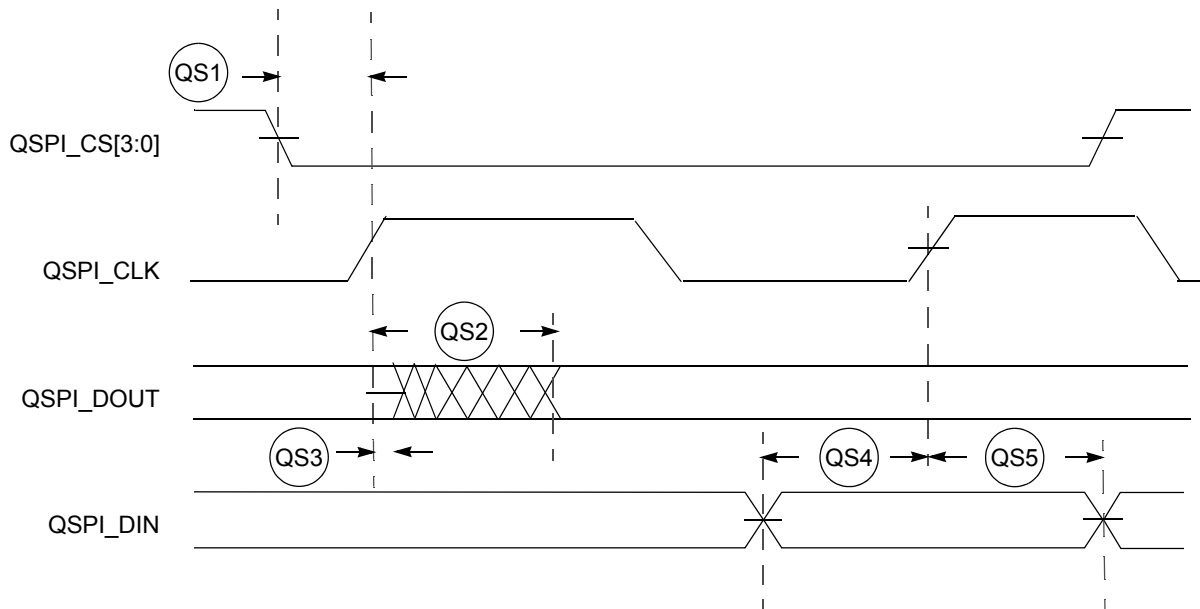


Figure 9. QSPI Timing

2.17 JTAG and Boundary Scan Timing

Table 37. JTAG and Boundary Scan Timing

Num	Characteristics ¹	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	\overline{TRST} assert time	t_{TRSTAT}	100	—	ns
J14	\overline{TRST} setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

¹ JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

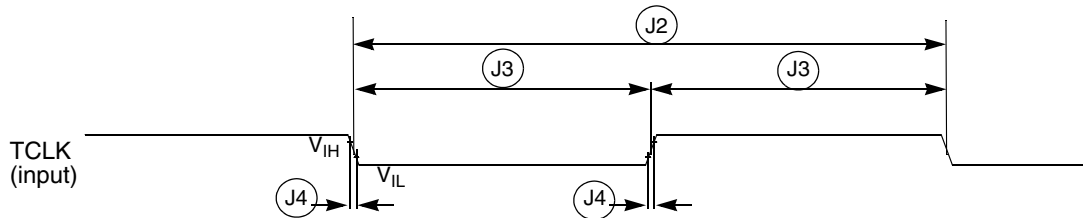


Figure 10. Test Clock Input Timing

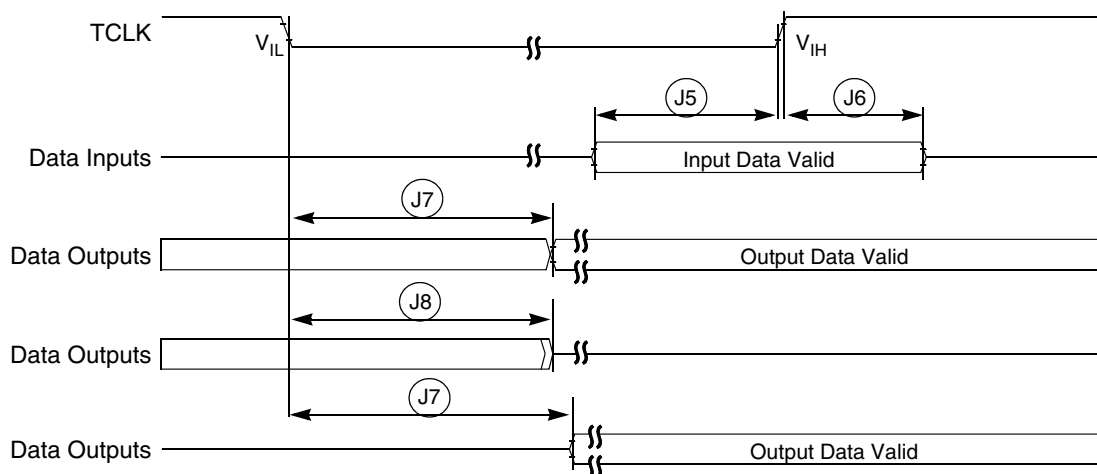


Figure 11. Boundary Scan (JTAG) Timing

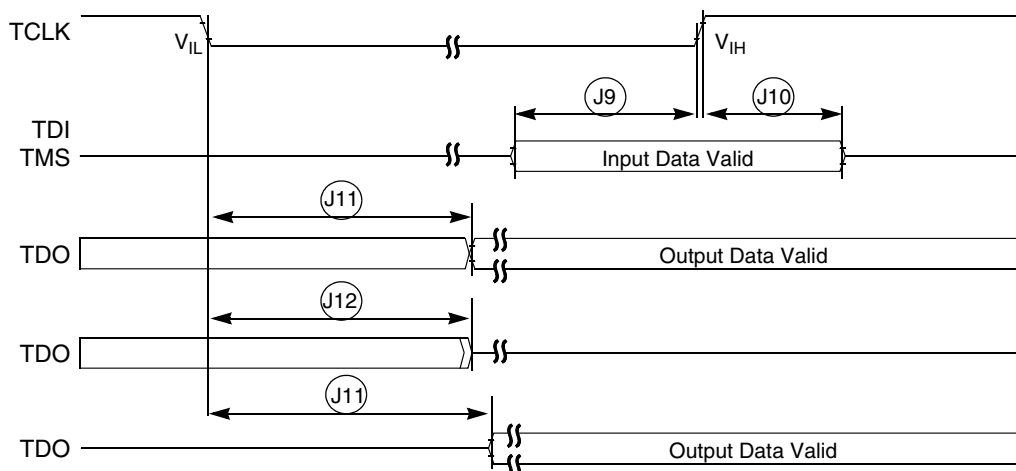


Figure 12. Test Access Port Timing

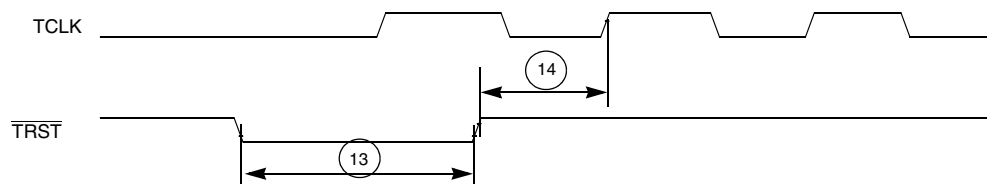


Figure 13. TRST Timing

2.18 Debug AC Timing Specifications

Table 38 lists specifications for the debug AC timing parameters shown in Figure 14.

Table 38. Debug AC Timing Specification

Num	Characteristic	66/80 MHz		Units
		Min	Max	
D1	PST, DDATA to CLKOUT setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.5	—	ns
D3	DSI-to-DSCLK setup	$1 \times t_{CYC}$	—	ns
D4 ¹	DSCLK-to-DSO hold	$4 \times t_{CYC}$	—	ns
D5	DSCLK cycle time	$5 \times t_{CYC}$	—	ns
D6	\overline{BKPT} input data setup time to CLKOUT rise	4	—	ns
D7	\overline{BKPT} input data hold time to CLKOUT rise	1.5	—	ns
D8	CLKOUT high to \overline{BKPT} high Z	0.0	10.0	ns

¹ DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 14 shows real-time trace timing for the values in Table 38.

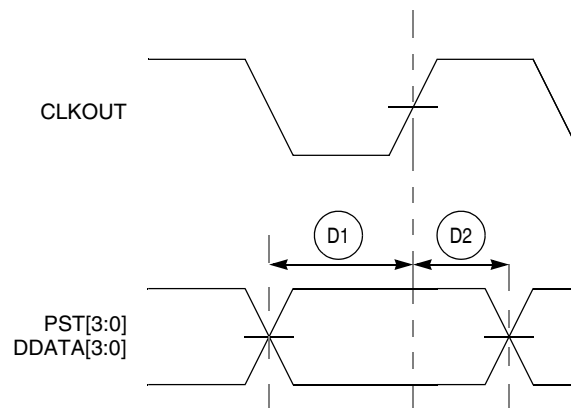


Figure 14. Real-Time Trace AC Timing

Mechanical Outline Drawings

Figure 15 shows BDM serial port AC timing for the values in Table 38.

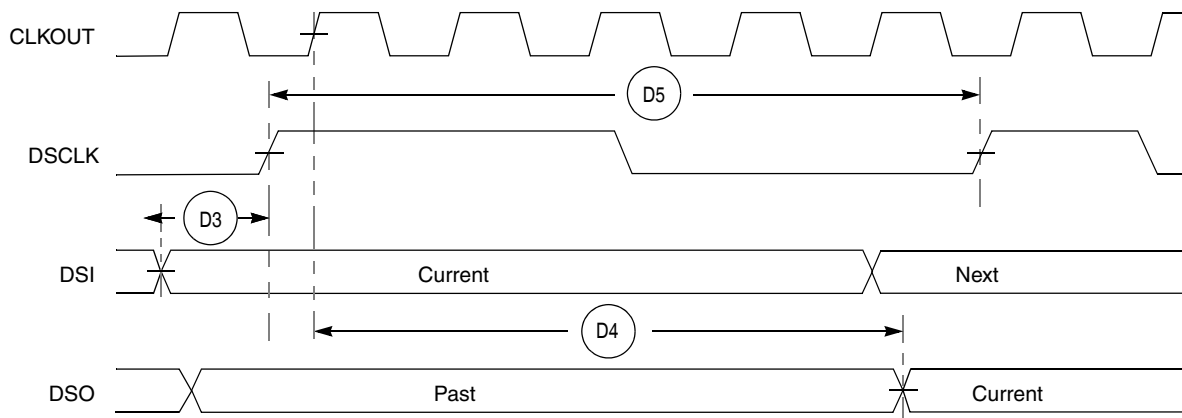
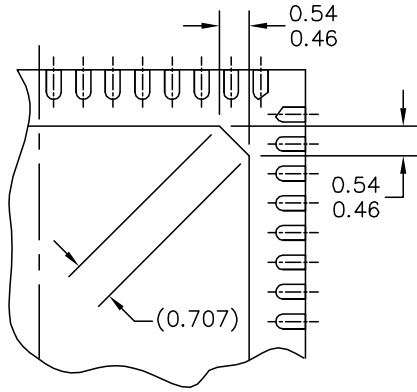


Figure 15. BDM Serial Port AC Timing

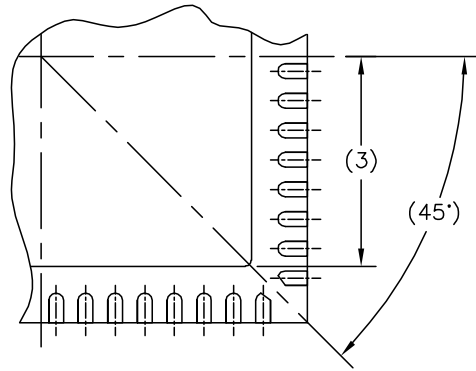
3 Mechanical Outline Drawings

This section describes the physical properties of the device and its derivatives.

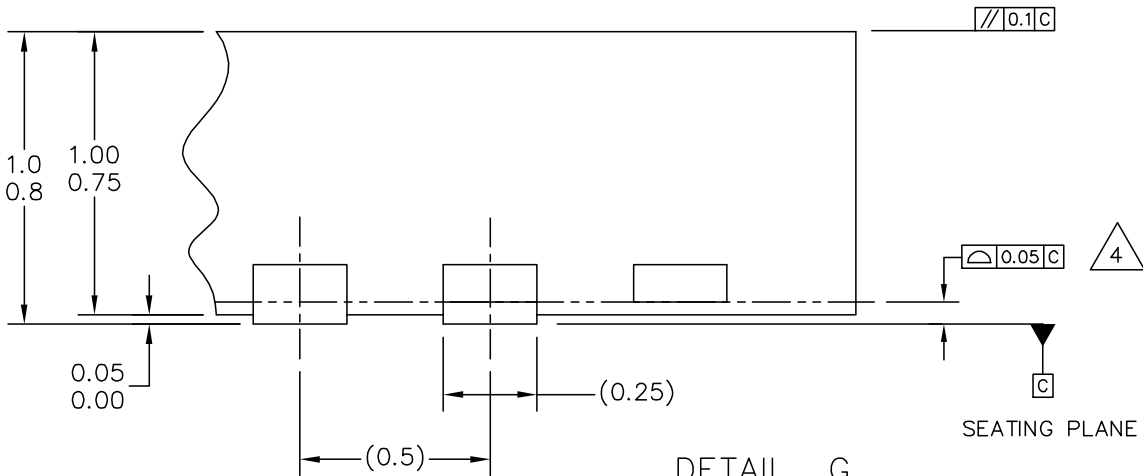
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		PAGE: 1740
	DO NOT SCALE THIS DRAWING	REV: 0



DETAIL M
PREFERRED PIN1 BACKSIDE IDENTIFIER



DETAIL N
PREFERRED CORNER CONFIGURATION



DETAIL G
VIEW ROTATED 90° CW

<p>TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)</p>	CASE NUMBER: 1740-01	
	STANDARD: JEDEC MO-220 VMMD-3	
	PACKAGE CODE: 6200	SHEET: 2 OF 4

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
- 4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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TITLE: PBGA, LOW PROFILE, 81 I/O, 10 X 10 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ASA10670D	REV: 0	
	CASE NUMBER: 1662-01	04 FEB 2005	
	STANDARD: NON-JEDEC		

4 Revision History

Table 39. Revision History

Revision	Description
0	Initial public release.
1	<ul style="list-style-type: none"> • Formatting, layout, spelling, and grammar corrections. • Added information about the MCF52212 and MCF52213 devices. • Synchronized the “Pin Functions by Primary and Alternate Purpose” table in this document and the reference manual. • Added a specification for V_{DDUSB} to the “Absolute maximum ratings” table. • Added specifications for V_{LVD} and V_{LVDHYS} to the “DC electrical specifications” table. • Added the “USB Operation” section. • Changed the maximum value for $f_{sys(P/E)}$ in the “SGFM Flash Program and Erase Characteristics” table (was “66.67 or 80”, is “102.4”). • Changed the maximum value for $f_{sys(R)}$ in the “SGFM Flash Program and Erase Characteristics” table (was “66.67 or 80”, is “50–80”). • Changed the crystal start-up time in the “PLL Electrical Specifications” table (was 10 ms, is 0.1 ms). • Updated the current consumption specifications. • Updated the maximum temperature and added clarifying footnote. • Changed the absolute maximum rating for V_{STBY} (was “-0.3 to 4.0”, is “+1.8 to 3.5”). • Changed the maximum value for f_{sys} in the “PLL Electrical Specifications” table (was “66.67 or 80”, is “50–80”).
2	<ul style="list-style-type: none"> • Updated Clock generation features • Updated Table: Clocking Modes and added appropriate footnote • In Table: CLock Source Electrical Specifications, updated the following values: $f_{crystal}$, f_{ext}, f_{ref_pll}, EXTAL input high voltage (External reference)