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1 Family Configurations

Table 1. MCF52211 Family Configurations

Module	52210	52211	52212	52213
Version 2 ColdFire Core with MAC (Multiply-Accumulate Unit)	•	•	•	•
System Clock	66, 80 MHz		50 MHz	
Performance (Dhrystone 2.1 MIPS)	up to 76		up to 46	
Flash / Static RAM (SRAM)	64/16 Kbytes	128/16 Kbytes	64/8 Kbytes	128/8 Kbytes
Interrupt Controller (INTC)	•	•	•	•
Fast Analog-to-Digital Converter (ADC)	•	•	•	•
USB On-The-Go (USB OTG)	•	•	•	•
Four-channel Direct-Memory Access (DMA)	•	•	•	•
Software Watchdog Timer (WDT)	•	•	•	•
Secondary Watchdog Timer	•	•	•	•
Two-channel Periodic Interrupt Timer (PIT)	2	2	2	2
Four-Channel General Purpose Timer (GPT)	•	•	•	•
32-bit DMA Timers	4	4	4	4
QSPI	•	•	•	•
UART(s)	2	2 (64 LQFP/QFN and 81 MAPBGA) 3 (100 LQFP)	2	2
I ² C	2	2	2	2
Eight/Four-channel 8/16-bit PWM Timer	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•
Chip Configuration and Reset Controller Module	•	•	•	•
Background Debug Mode (BDM)	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port ¹	•	•	•	•
Package	64 LQFP/QFN 81 MAPBGA	64 LQFP/QFN 81 MAPBGA 100 LQFP	64 LQFP	64 LQFP

¹ The full debug/trace interface is available only on the 100-pin packages. A reduced debug interface is bonded on smaller packages.

1.1 Block Diagram

Figure 1 shows a top-level block diagram of the device. Package options for this family are described later in this document.

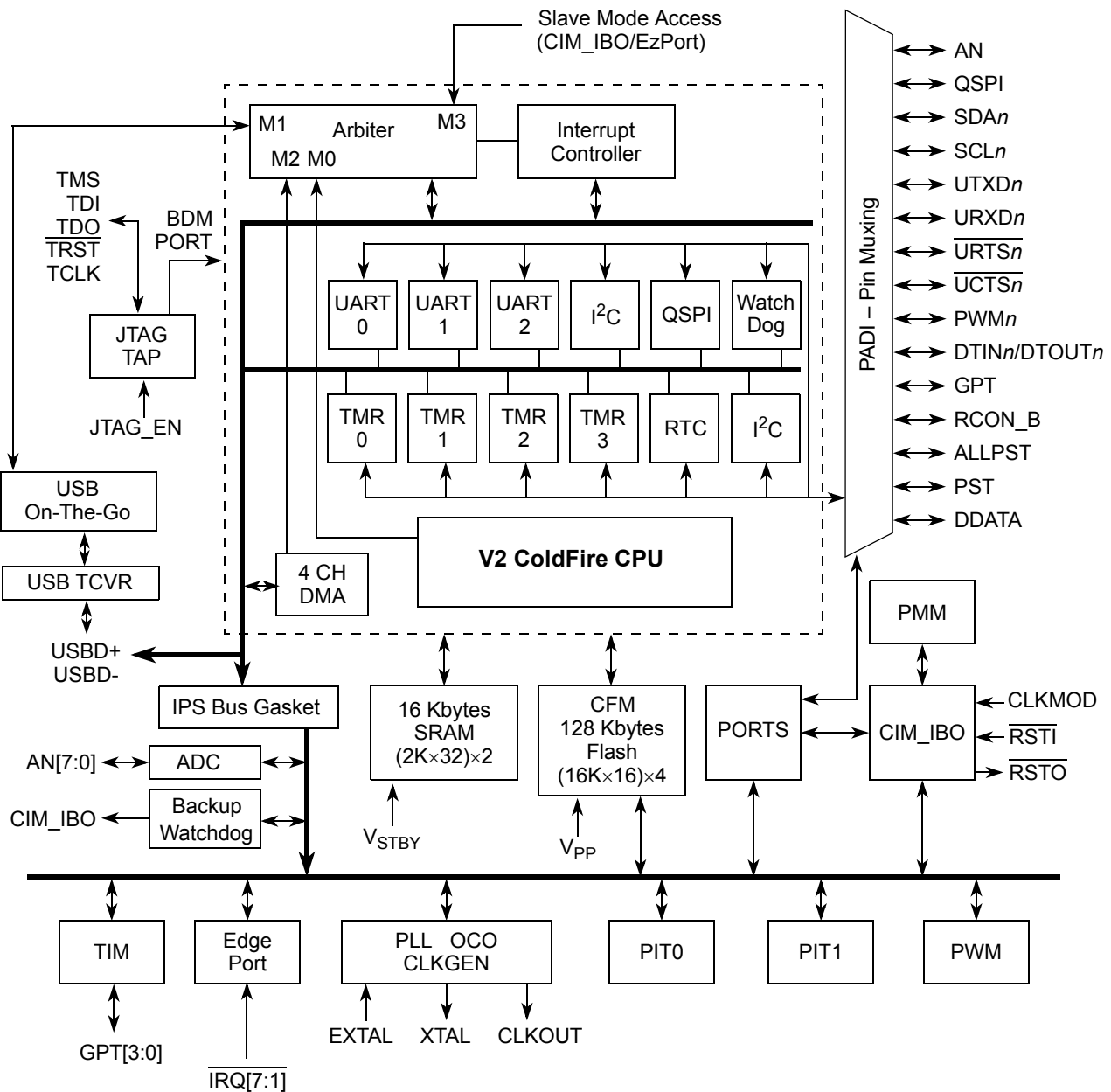


Figure 1. Block Diagram

Family Configurations

The full debug/trace interface is available only on the 100-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The processor supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The device implementation can:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.5 On-Chip Memories

1.2.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 8- or 16-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 8- or 16-Kbyte boundary within the 4-Gbyte address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.5.2 Flash Memory

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with up to four banks of 16-Kbyte×16-bit flash memory arrays to generate up to 128 Kbytes of 32-bit flash memory. These electrically erasable and programmable arrays serve as non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller that supports interleaved accesses from the 2-cycle flash memory arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash memory programming interface that allows the flash memory to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips.

1.2.6 Power Management

The device incorporates several low-power modes of operation entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage to the chip falls below the standby battery voltage.

1.2.7 USB On-The-Go Controller

The device includes a Universal Serial Bus On-The-Go (USB OTG) dual-mode controller. USB is a popular standard for connecting peripherals and portable consumer electronic devices such as digital cameras and handheld computers to host PCs. The OTG supplement to the USB specification extends USB to peer-to-peer application, enabling devices to connect directly to each other without the need for a PC. The dual-mode controller on the device can act as a USB OTG host and as a USB device. It also supports full-speed and low-speed modes.

1.2.8 UARTs

The device has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions.

1.2.9 I²C Bus

The processor includes two I²C modules. The I²C bus is an industry-standard, two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange and minimizes the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

1.2.10 QSPI

The queued serial peripheral interface (QSPI) provides a synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, minimizing the need for CPU intervention between transfers.

1.2.11 Fast ADC

The fast ADC consists of an eight-channel input select multiplexer and two independent sample and hold (S/H) circuits feeding separate 12-bit ADCs. The two separate converters store their results in accessible buffers for further processing.

The ADC can be configured to perform a single scan and halt, a scan when triggered, or a programmed scan sequence repeatedly until manually stopped.

The ADC can be configured for sequential or simultaneous conversion. When configured for sequential conversions, up to eight channels can be sampled and stored in any order specified by the channel list register. Both ADCs may be required during a scan, depending on the inputs to be sampled.

During a simultaneous conversion, both S/H circuits are used to capture two different channels at the same time. This configuration requires that a single channel may not be sampled by both S/H circuits simultaneously.

Optional interrupts can be generated at the end of the scan sequence if a channel is out of range (measures below the low threshold limit or above the high threshold limit set in the limit registers) or at several different zero crossing conditions.

1.2.12 DMA Timers (DTIM0–DTIM3)

There are four independent, DMA transfer capable 32-bit timers (DTIM0, DTIM1, DTIM2, and DTIM3) on the device. Each module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTIN_{*n*} signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler that clocks the actual timer counter register (TCR_{*n*}). Each of these timers can be configured for input capture or reference (output) compare mode. Timer events may optionally cause interrupt requests or DMA transfers.

1.2.13 General Purpose Timer (GPT)

The general purpose timer (GPT) is a four-channel timer module consisting of a 16-bit programmable counter driven by a seven-stage programmable prescaler. Each of the four channels can be configured for input capture or output compare. Additionally, channel three, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator.

1.2.14 Periodic Interrupt Timers (PIT0 and PIT1)

The two periodic interrupt timers (PIT0 and PIT1) are 16-bit timers that provide interrupts at regular intervals with minimal processor intervention. Each timer can count down from the value written in its PIT modulus register or it can be a free-running down-counter.

1.2.15 Real-Time Clock (RTC)

The Real-Time Clock (RTC) module maintains the system (time-of-day) clock and provides stopwatch, alarm, and interrupt functions. It includes full clock features: seconds, minutes, hours, days and supports a host of time-of-day interrupt functions along with an alarm interrupt.

1.2.16 Pulse-Width Modulation (PWM) Timers

The device has an 8-channel, 8-bit PWM timer. Each channel has a programmable period and duty cycle as well as a dedicated counter. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The timer supports PCM mode, which results in superior signal quality when compared to that of a conventional PWM. The PWM outputs have programmable polarity, and can be programmed as left aligned outputs or center aligned outputs. For higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.17 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.18 Backup Watchdog Timer

The backup watchdog timer is an independent 16-bit timer that, like the software watchdog timer, facilitates recovery from runaway code. This timer is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown. The backup watchdog timer can be clocked by either the relaxation oscillator or the system clock.

1.2.19 Phase-Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

Table 2 shows the pinout configuration for the 100 LQFP.

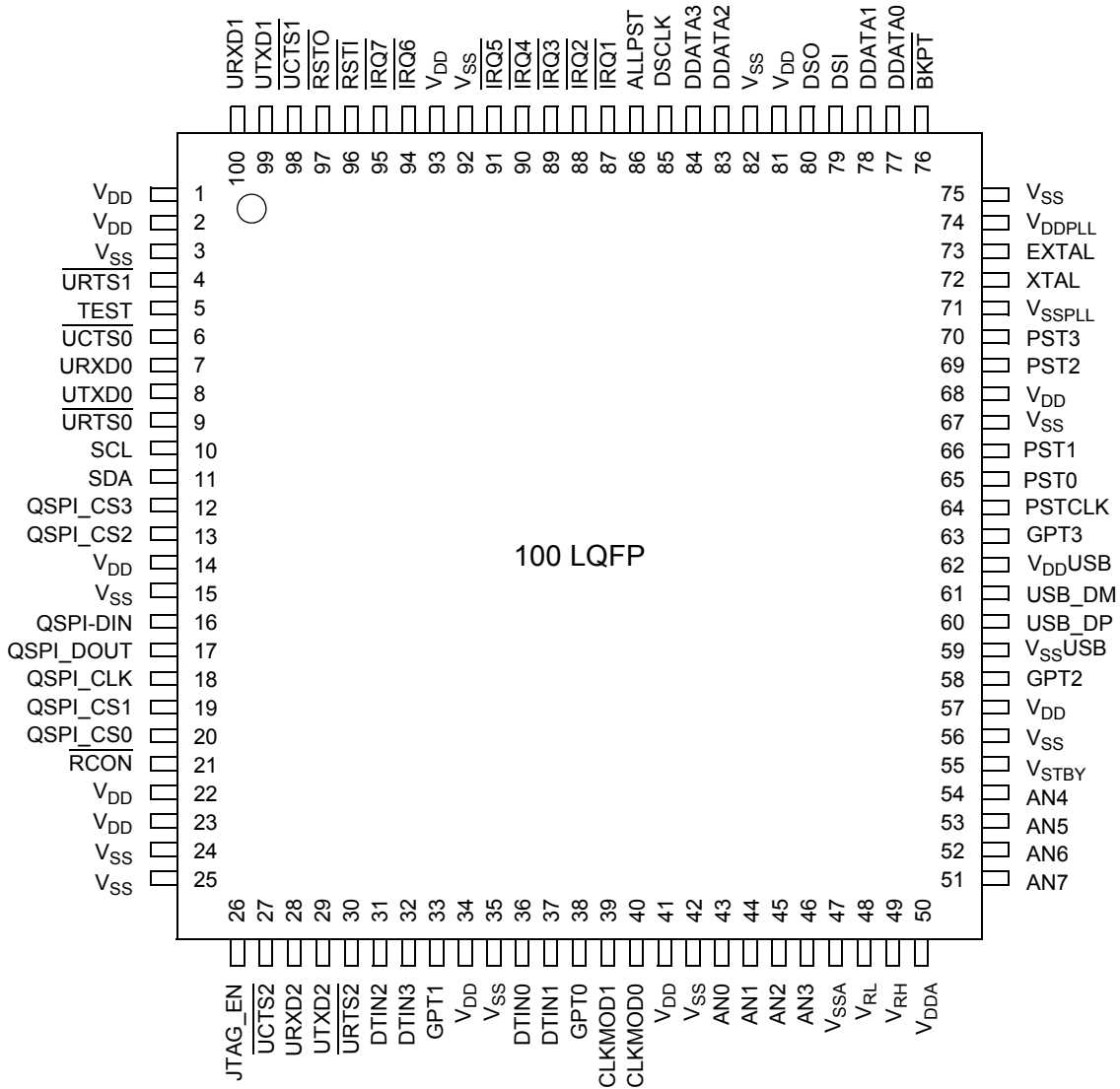


Figure 2. 100 LQFP Pin Assignments

Figure 4 shows the pinout configuration for the 64 LQFP and 64 QFN.

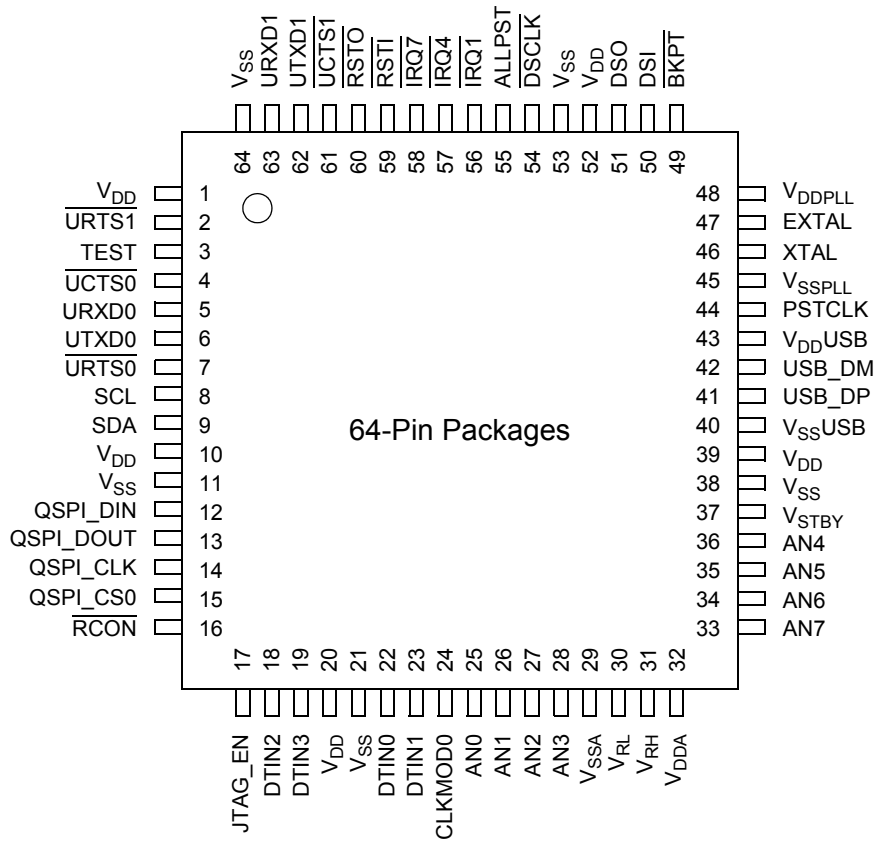


Figure 4. 64 LQFP and 64 QFN Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control ¹	Slew Rate / Control ¹	Pull-up / Pull-down ²	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
UART 1	$\overline{UCTS1}$	SYNCA	URXD2	GPIO	PDSR[15]	PSRR[15]	—	98	C3	61
	$\overline{URTS1}$	SYNCB	UTXD2	GPIO	PDSR[14]	PSRR[14]	—	4	B1	2
	URXD1	—	—	GPIO	PDSR[13]	PSRR[13]	—	100	B2	63
	UTXD1	—	—	GPIO	PDSR[12]	PSRR[12]	—	99	A2	62
UART 2	$\overline{UCTS2}$	—	—	GPIO	PDSR[27]	PSRR[27]	—	27	—	—
	$\overline{URTS2}$	—	—	GPIO	PDSR[26]	PSRR[26]	—	30	—	—
	URXD2	—	—	GPIO	PDSR[25]	PSRR[25]	—	28	—	—
	UTXD2	—	—	GPIO	PDSR[24]	PSRR[24]	—	29	—	—
VSTBY	VSTBY	—	—	—	N/A	N/A	—	55	F8	37
USB	VDDUSB	—	—	—	N/A	N/A	—	62	D8	43
	VSSUSB	—	—	—	N/A	N/A	—	59	F7	40
	USB_DM	—	—	—	N/A	N/A	—	61	D9	42
	USB_DP	—	—	—	N/A	N/A	—	60	E9	41
VDD	VDD	—	—	—	N/A	N/A	—	1,2,14,22,23,34,41,57,68,81,93	D5,E3–E7, F5	1,10,20,39,52
VSS	VSS	—	—	—	N/A	N/A	—	3,15,24,25,35,42,56,67,75,82,92	A1,A9,D4,D6,F4,F6,J1	11,21,38,53,64

¹ The PDSR and PSSR registers are described in the General Purpose I/O chapter. All programmable signals default to 2 mA drive and FAST slew rate in normal (single-chip) mode.

² All signals have a pull-up in GPIO mode.

³ These signals are multiplexed on other pins.

⁴ For primary and GPIO functions only.

⁵ Only when JTAG mode is enabled.

⁶ CLKMOD0 and CLKMOD1 have internal pull-down resistors; however, the use of external resistors is very strongly recommended.

⁷ When these pins are configured for USB signals, they should use the USB transceiver's internal pull-up/pull-down resistors (see the description of the OTG_CTRL register). If these pins are not configured for USB signals, each pin should be pulled down externally using a 10 kΩ resistor.

⁸ For secondary and GPIO functions only.

⁹ RSTI has an internal pull-up resistor; however, the use of an external resistor is very strongly recommended.

¹⁰ For GPIO function. Primary Function has pull-up control within the GPT module.

Table 16. Debug Support Signals (continued)

Signal Name	Abbreviation	Function	I/O
Test Data Output	TDO	Serial output for test instructions and data. TDO is tri-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.	O
Development Serial Clock	DSCLK	Development Serial Clock - Internally synchronized input. (The logic level on DSCLK is validated if it has the same value on two consecutive rising bus clock edges.) Clocks the serial communication port to the debug module during packet transfers. Maximum frequency is PSTCLK/5. At the synchronized rising edge of DSCLK, the data input on DSI is sampled and DSO changes state.	I
Breakpoint	$\overline{\text{BKPT}}$	Breakpoint - Input used to request a manual breakpoint. Assertion of $\overline{\text{BKPT}}$ puts the processor into a halted state after the current instruction completes. Halt status is reflected on processor status/debug data signals (PST[3:0] and PSTDDATA[7:0]) as the value 0xF. If CSR[BKD] is set (disabling normal $\overline{\text{BKPT}}$ functionality), asserting $\overline{\text{BKPT}}$ generates a debug interrupt exception in the processor.	I
Development Serial Input	DSI	Development Serial Input - Internally synchronized input that provides data input for the serial communication port to the debug module, after the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output - Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock - Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, and PST and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be reenabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical AND of PST[3:0]. The CLKOUT signal can be used by the development system to know when to sample ALLPST.	O

1.16 EzPort Signal Descriptions

Table 17 contains a list of EzPort external signals.

2.3 Thermal Characteristics

Table 22 lists thermal resistance values.

Table 22. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	42 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	25 ⁴	°C/W
	Junction to case	—	θ_{JC}	9 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
81 MAPBGA	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	61 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	35 ^{2,3}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50 ^{2,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	31 ^{2,3}	°C/W
	Junction to board	—	θ_{JB}	20 ⁴	°C/W
	Junction to case	—	θ_{JC}	12 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
64 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	62 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	43 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	36 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	26 ⁴	°C/W
	Junction to case	—	θ_{JC}	9 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
64 QFN	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	68 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	24 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	55 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	19 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	8 ⁴	°C/W
	Junction to case (bottom)	—	θ_{JC}	0.6 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	3 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

Table 28. Oscillator and PLL Electrical Specifications (continued)
 $(V_{DD}$ and $V_{DDPLL} = 2.7$ to 3.6 V, $V_{SS} = V_{SSPLL} = 0$ V)

Characteristic	Symbol	Min	Max	Unit
Frequency un-LOCK range	f_{UL}	-1.5	1.5	% f_{ref}
Frequency LOCK range	f_{LCK}	-0.75	0.75	% f_{ref}
CLKOUT period jitter ^{4, 5, 10, 11} , measured at f_{SYS} Max <ul style="list-style-type: none"> • Peak-to-peak (clock edge to clock edge) • Long term (averaged over 2 ms interval) 	C_{jitter}	— —	10 .01	% f_{sys}
On-chip oscillator frequency	f_{oco}	7.84	8.16	MHz

¹ In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

² This value has been updated.

³ All internal registers retain data at 0 Hz.

⁴ Depending on packaging; see the orderable part number summary.

⁵ Loss of Reference Frequency is the reference frequency detected internally, which transitions the PLL into self clocked mode.

⁶ Self clocked mode frequency is the frequency at which the PLL operates when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

⁷ This parameter is characterized before qualification rather than 100% tested.

⁸ Proper PC board layout procedures must be followed to achieve specifications.

⁹ This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

¹⁰ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys} .

Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{jitter} percentage for a given interval.

¹¹ Based on slow system clock of 40 MHz measured at f_{sys} max.

2.9 USB Operation

Table 29. USB Operation Specifications

Characteristic	Symbol	Value	Unit
Minimum core speed for USB operation	$f_{sys_USB_min}$	16	MHz

2.10 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, timer, UART, Interrupt and USB interfaces. When in GPIO mode, the timing specification for these pins is given in [Table 30](#) and [Figure 5](#).

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive
- 25 pF / 25 Ω for low drive

2.12 I²C Input/Output Timing Specifications

Table 32 lists specifications for the I²C input timing parameters shown in Figure 7.

Table 32. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11	Start condition hold time	$2 \times t_{CYC}$	—	ns
12	Clock low period	$8 \times t_{CYC}$	—	ns
13	SCL/SDA rise time ($V_{IL} = 0.5 \text{ V}$ to $V_{IH} = 2.4 \text{ V}$)	—	1	ms
14	Data hold time	0	—	ns
15	SCL/SDA fall time ($V_{IH} = 2.4 \text{ V}$ to $V_{IL} = 0.5 \text{ V}$)	—	1	ms
16	Clock high time	$4 \times t_{CYC}$	—	ns
17	Data setup time	0	—	ns
18	Start condition setup time (for repeated start condition only)	$2 \times t_{CYC}$	—	ns
19	Stop condition setup time	$2 \times t_{CYC}$	—	ns

Table 33 lists specifications for the I²C output timing parameters shown in Figure 7.

Table 33. I²C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11 ¹	Start condition hold time	$6 \times t_{CYC}$	—	ns
12 ¹	Clock low period	$10 \times t_{CYC}$	—	ns
13 ²	I2C_SCL/I2C_SDA rise time ($V_{IL} = 0.5 \text{ V}$ to $V_{IH} = 2.4 \text{ V}$)	—	—	μs
14 ¹	Data hold time	$7 \times t_{CYC}$	—	ns
15 ³	I2C_SCL/I2C_SDA fall time ($V_{IH} = 2.4 \text{ V}$ to $V_{IL} = 0.5 \text{ V}$)	—	3	ns
16 ¹	Clock high time	$10 \times t_{CYC}$	—	ns
17 ¹	Data setup time	$2 \times t_{CYC}$	—	ns
18 ¹	Start condition setup time (for repeated start condition only)	$20 \times t_{CYC}$	—	ns
19 ¹	Stop condition setup time	$10 \times t_{CYC}$	—	ns

¹ Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 33. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 33 are minimum values.

² Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

³ Specified at a nominal 50-pF load.

Table 37. JTAG and Boundary Scan Timing

Num	Characteristics ¹	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	\overline{TRST} assert time	t_{TRSTAT}	100	—	ns
J14	\overline{TRST} setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

¹ JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

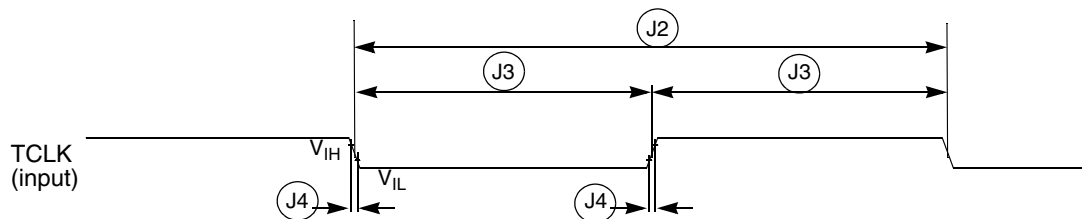


Figure 10. Test Clock Input Timing

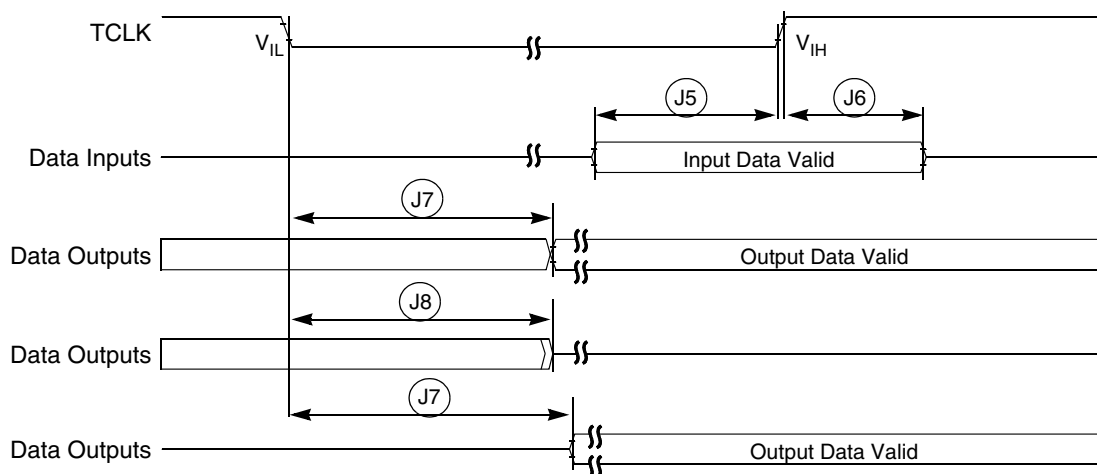


Figure 11. Boundary Scan (JTAG) Timing

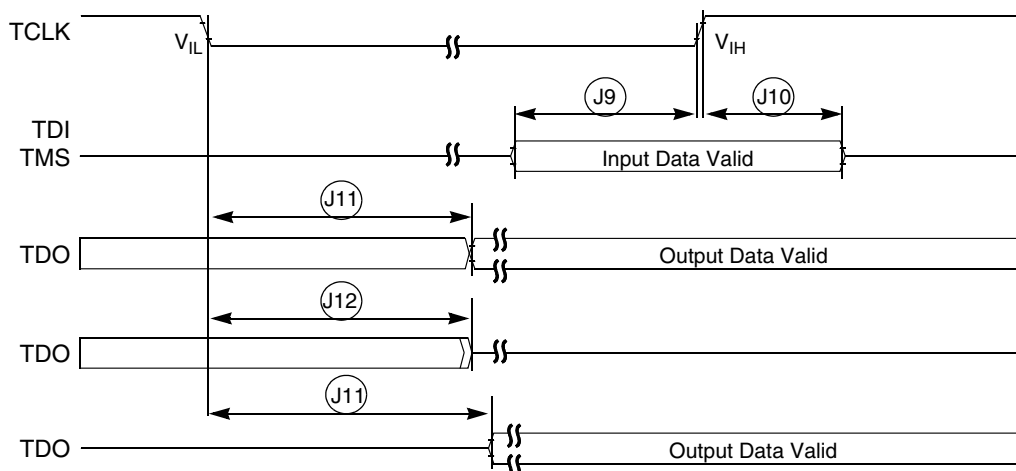


Figure 12. Test Access Port Timing

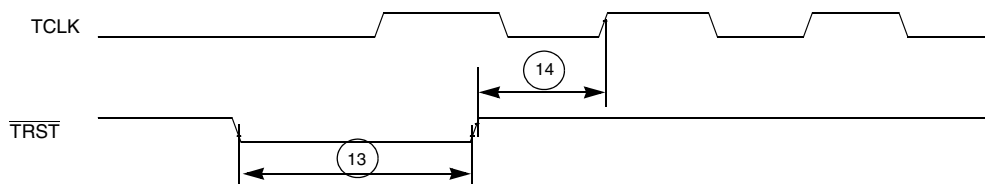


Figure 13. TRST Timing

2.18 Debug AC Timing Specifications

Table 38 lists specifications for the debug AC timing parameters shown in Figure 14.

Table 38. Debug AC Timing Specification

Num	Characteristic	66/80 MHz		Units
		Min	Max	
D1	PST, DDATA to CLKOUT setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.5	—	ns
D3	DSI-to-DSCLK setup	$1 \times t_{CYC}$	—	ns
D4 ¹	DSCLK-to-DSO hold	$4 \times t_{CYC}$	—	ns
D5	DSCLK cycle time	$5 \times t_{CYC}$	—	ns
D6	\overline{BKPT} input data setup time to CLKOUT rise	4	—	ns
D7	\overline{BKPT} input data hold time to CLKOUT rise	1.5	—	ns
D8	CLKOUT high to \overline{BKPT} high Z	0.0	10.0	ns

¹ DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 14 shows real-time trace timing for the values in Table 38.

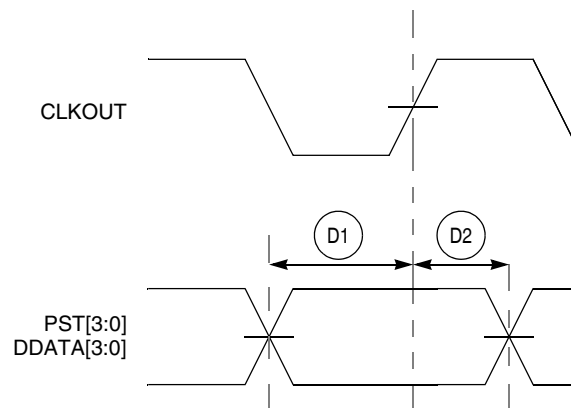


Figure 14. Real-Time Trace AC Timing

Mechanical Outline Drawings

Figure 15 shows BDM serial port AC timing for the values in Table 38.

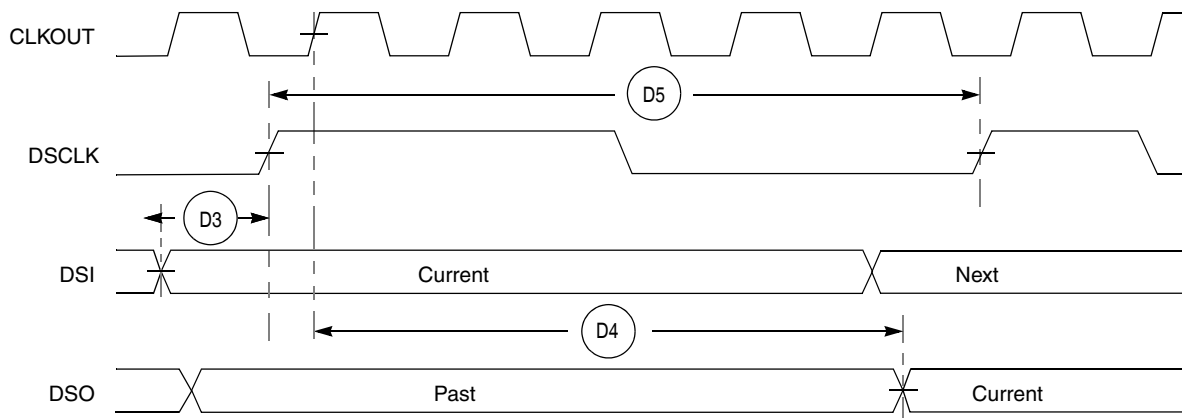
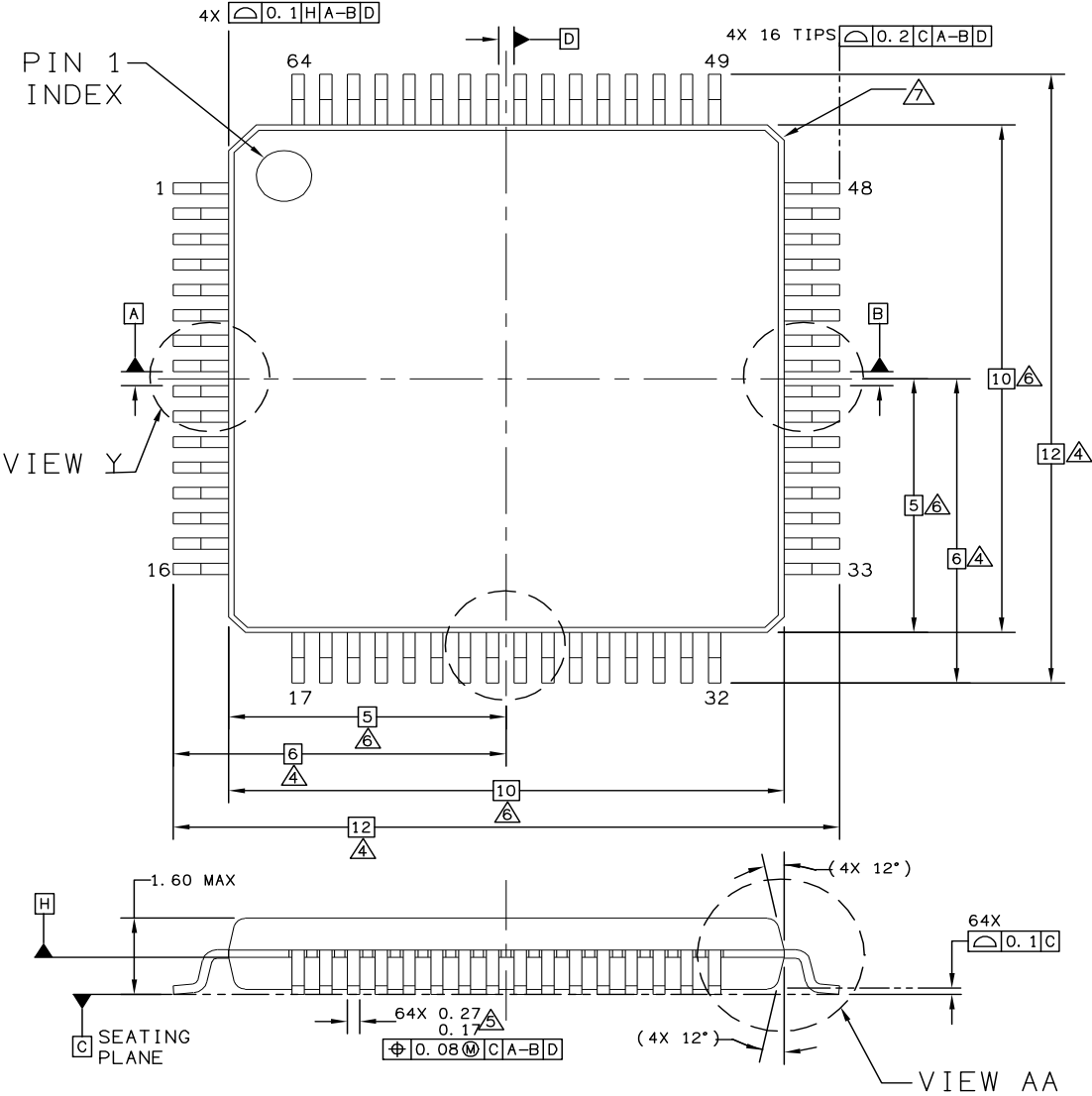


Figure 15. BDM Serial Port AC Timing

3 Mechanical Outline Drawings

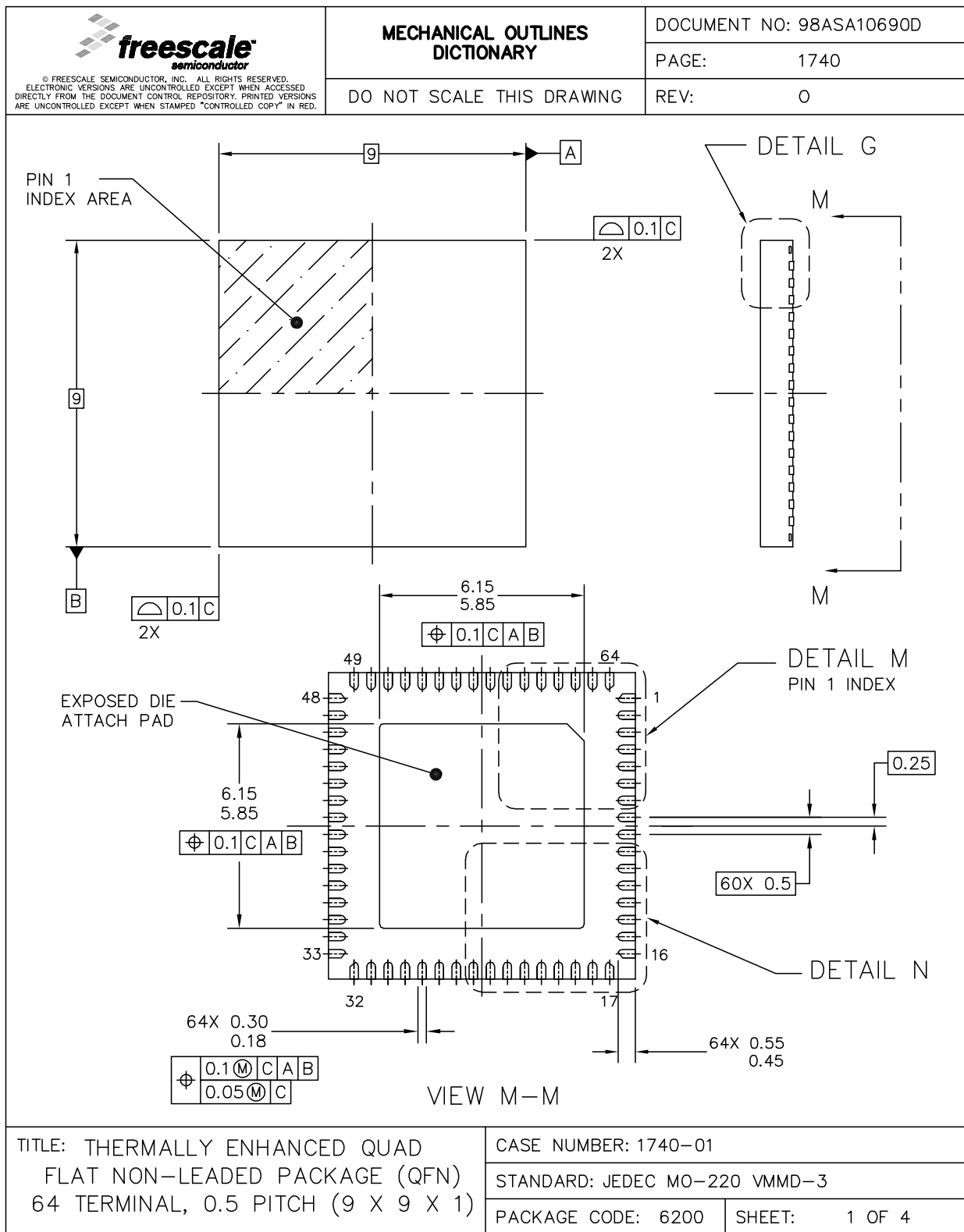
This section describes the physical properties of the device and its derivatives.

3.1 64-pin LQFP Package

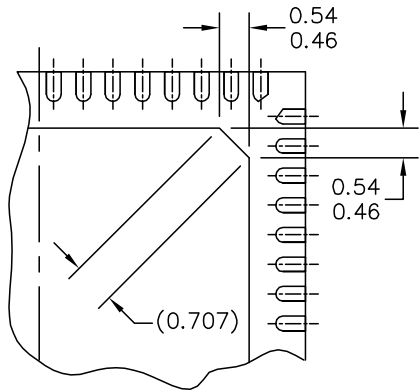


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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D	
	CASE NUMBER: 840F-02	06 APR 2005	
	STANDARD: JEDEC MS-026 BCD		

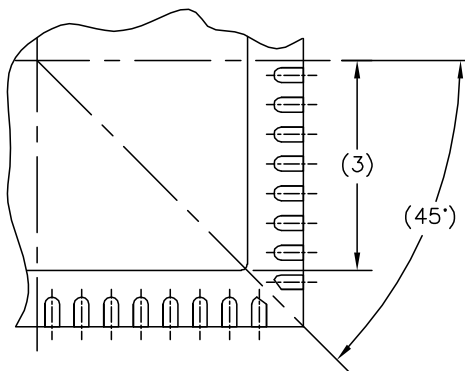
3.2 64 QFN Package



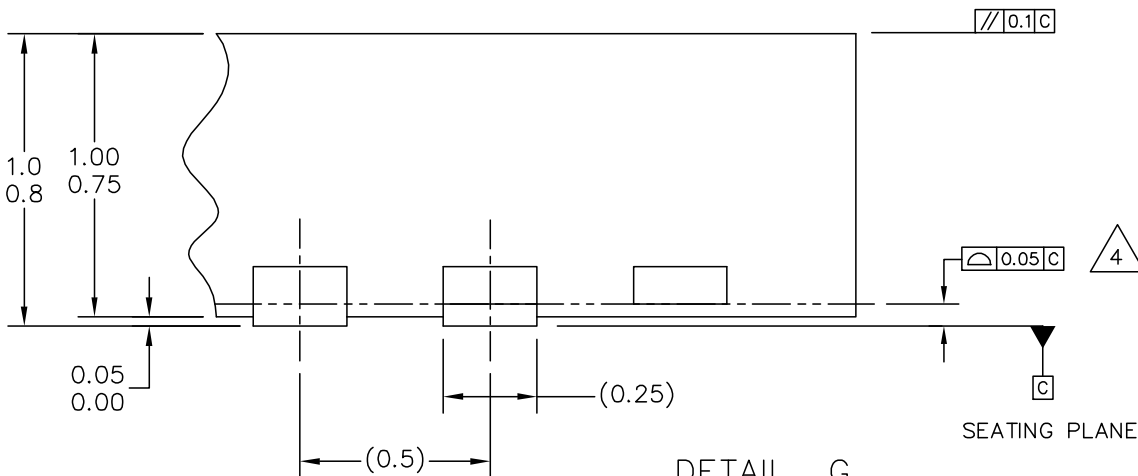
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		PAGE: 1740
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DETAIL M
PREFERRED PIN1 BACKSIDE IDENTIFIER



DETAIL N
PREFERRED CORNER CONFIGURATION



DETAIL G
VIEW ROTATED 90° CW

TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	CASE NUMBER: 1740-01	
	STANDARD: JEDEC MO-220 VMMD-3	
	PACKAGE CODE: 6200	SHEET: 2 OF 4