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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52211cvm80

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1.1 Block Diagram

Figure 1 shows a top-level block diagram of the device. Package options for this family are described later in this document.

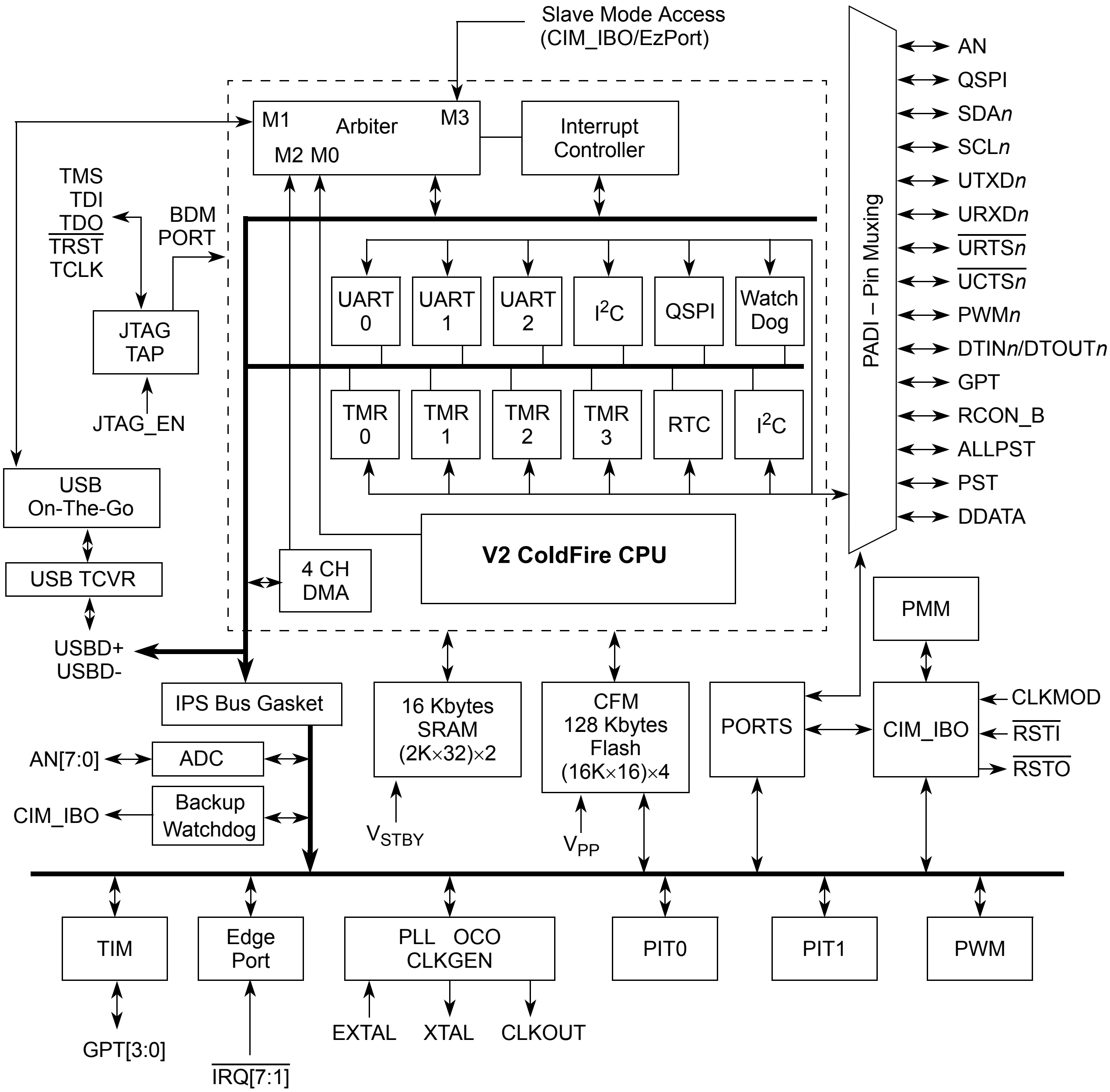


Figure 1. Block Diagram

1.2 Features

1.2.1 Feature Overview

The MCF52211 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data paths on-chip
  - Up to 80 MHz processor core frequency
  - 40 MHz and 33 MHz off-platform bus frequency
  - Sixteen general-purpose, 32-bit data and address registers
  - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
  - Multiply-Accumulate (MAC) unit with 32-bit accumulator to support $16 \times 16 \rightarrow 32$ or $32 \times 32 \rightarrow 32$ operations
- System debug support
  - Real-time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
  - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
  - Up to 16-Kbyte dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support
  - Up to 128 Kbytes of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used (except backup watchdog timer)
  - Software controlled disable of external clock output for low-power consumption
- Universal Serial Bus On-The-Go (USB OTG) dual-mode host and device controller
  - Full-speed / low-speed host controller
  - USB 1.1 and 2.0 compliant full-speed / low speed device controller
  - 16 bidirectional end points
  - DMA or FIFO data stream interfaces
  - Low power consumption
  - OTG protocol logic
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic with maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7 or 8 bits with even, odd, or no parity
  - Up to two stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
  - Transmit and receive FIFO buffers
- Two I^2C modules

The full debug/trace interface is available only on the 100-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The processor supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The device implementation can:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.5 On-Chip Memories

1.2.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 8- or 16-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 8- or 16-Kbyte boundary within the 4-Gbyte address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.5.2 Flash Memory

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with up to four banks of 16-Kbyte×16-bit flash memory arrays to generate up to 128 Kbytes of 32-bit flash memory. These electrically erasable and programmable arrays serve as non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller that supports interleaved accesses from the 2-cycle flash memory arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash memory programming interface that allows the flash memory to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips.

1.2.6 Power Management

The device incorporates several low-power modes of operation entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage to the chip falls below the standby battery voltage.

Figure 3 shows the pinout configuration for the 81 MAPBGA.

	1	2	3	4	5	6	7	8	9
A	V_{SS}	UTXD1	$\overline{\text{RSTI}}$	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ3}}$	ALLPST	TDO	TMS	V_{SS}
B	$\overline{\text{URTS1}}$	URXD1	$\overline{\text{RSTO}}$	$\overline{\text{IRQ6}}$	$\overline{\text{IRQ2}}$	$\overline{\text{TRST}}$	TDI	V_{DD}PLL	EXTAL
C	$\overline{\text{UCTS0}}$	TEST	$\overline{\text{UCTS1}}$	$\overline{\text{IRQ7}}$	$\overline{\text{IRQ4}}$	$\overline{\text{IRQ1}}$	TCLK	V_{SS}PLL	XTAL
D	URXD0	UTXD0	$\overline{\text{URTS0}}$	V_{SS}	V_{DD}	V_{SS}	PWM7	GPT3	GPT2
E	SCL	SDA	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	PWM5	GPT1
F	QSPI_CS3	QSPI_CS2	QSPI_DIN	V_{SS}	V_{DD}	V_{SS}	GPT0	V_{STBY}	AN4
G	QSPI_DOUT	QSPI_CLK	$\overline{\text{RCON}}$	DTIN1	CLKMOD0	AN2	AN3	AN5	AN6
H	QSPI_CS0	QSPI_CS1	DTIN3	DTIN0	CLKMOD1	AN1	V_{SSA}	V_{DDA}	AN7
J	V_{SS}	JTAG_EN	DTIN2	PWM3	PWM1	AN0	V_{RL}	V_{RH}	V_{SSA}

Figure 3. 81 MAPBGA Pin Assignments

Figure 4 shows the pinout configuration for the 64 LQFP and 64 QFN.

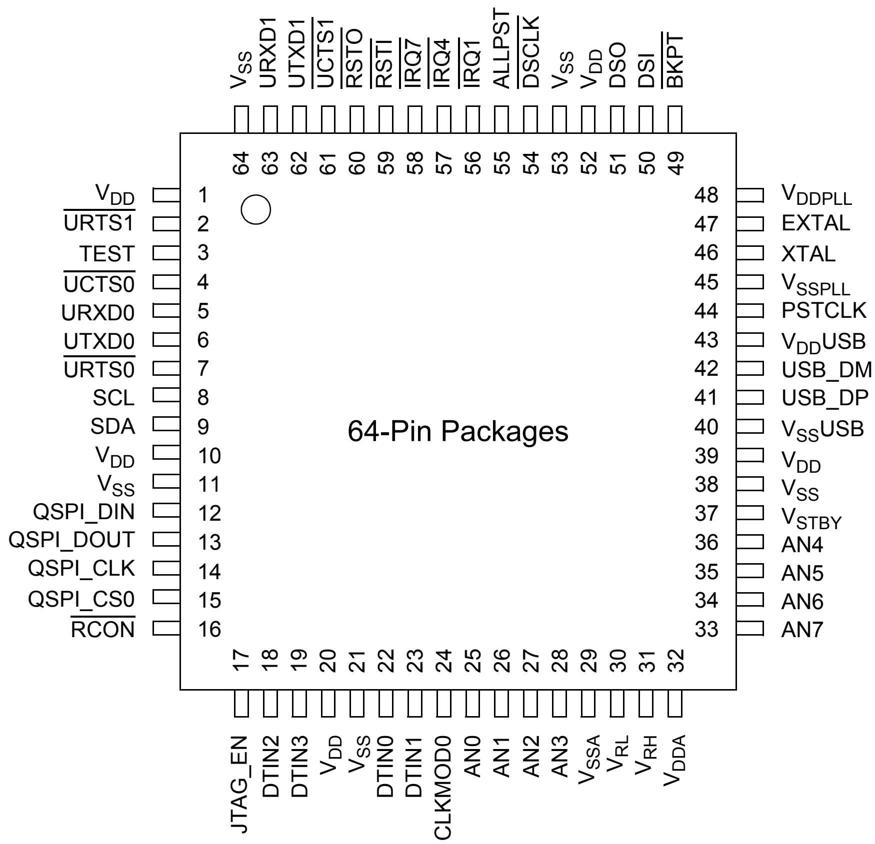


Figure 4. 64 LQFP and 64 QFN Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
UART 1	$\overline{\text{UCTS1}}$	SYNCA	URXD2	GPIO	PDSR[15]	PSRR[15]	—	98	C3	61
	$\overline{\text{URTS1}}$	SYNCB	UTXD2	GPIO	PDSR[14]	PSRR[14]	—	4	B1	2
	URXD1	—	—	GPIO	PDSR[13]	PSRR[13]	—	100	B2	63
	UTXD1	—	—	GPIO	PDSR[12]	PSRR[12]	—	99	A2	62
UART 2	$\overline{\text{UCTS2}}$	—	—	GPIO	PDSR[27]	PSRR[27]	—	27	—	—
	$\overline{\text{URTS2}}$	—	—	GPIO	PDSR[26]	PSRR[26]	—	30	—	—
	URXD2	—	—	GPIO	PDSR[25]	PSRR[25]	—	28	—	—
	UTXD2	—	—	GPIO	PDSR[24]	PSRR[24]	—	29	—	—
VSTBY	VSTBY	—	—	—	N/A	N/A	—	55	F8	37
USB	VDDUSB	—	—	—	N/A	N/A	—	62	D8	43
	VSSUSB	—	—	—	N/A	N/A	—	59	F7	40
	USB_DM	—	—	—	N/A	N/A	—	61	D9	42
	USB_DP	—	—	—	N/A	N/A	—	60	E9	41
VDD	VDD	—	—	—	N/A	N/A	—	1,2,14,22, 23,34,41, 57,68,81,93	D5,E3–E7, F5	1,10,20,39,5 2
VSS	VSS	—	—	—	N/A	N/A	—	3,15,24,25,3 5,42,56, 67,75,82,92	A1,A9,D4,D 6,F4,F6,J1	11,21,38, 53,64

1 The PDSR and PSSR registers are described in the General Purpose I/O chapter. All programmable signals default to 2 mA drive and FAST slew rate in normal (single-chip) mode.

2 All signals have a pull-up in GPIO mode.

3 These signals are multiplexed on other pins.

4 For primary and GPIO functions only.

5 Only when JTAG mode is enabled.

6 CLKMOD0 and CLKMOD1 have internal pull-down resistors; however, the use of external resistors is very strongly recommended.

7 When these pins are configured for USB signals, they should use the USB transceiver's internal pull-up/pull-down resistors (see the description of the OTG_CTRL register). If these pins are not configured for USB signals, each pin should be pulled down externally using a 10 kΩ resistor.

8 For secondary and GPIO functions only.

9 $\overline{\text{RSTI}}$ has an internal pull-up resistor; however, the use of an external resistor is very strongly recommended.

10 For GPIO function. Primary Function has pull-up control within the GPT module.

Table 17. EzPort Signal Descriptions

Signal Name	Abbreviation	Function	I/O
EzPort Clock	EZPCK	Shift clock for EzPort transfers.	I
EzPort Chip Select	EZPCS	Chip select for signalling the start and end of serial transfers.	I
EzPort Serial Data In	EZPD	EZPD is sampled on the rising edge of EZPCK.	I
EzPort Serial Data Out	EZPQ	EZPQ transitions on the falling edge of EZPCK.	O

1.17 Power and Ground Pins

The pins described in Table 18 provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

Table 18. Power and Ground Pins

Signal Name	Abbreviation	Function
PLL Analog Supply	VDDPLL, VSSPLL	Dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply.
Positive Supply	VDD	These pins supply positive power to the core logic.
Ground	VSS	This pin is the negative supply (ground) to the chip.

Table 24. SGFM Flash Module Life Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles[1] before failure	P/E	10,000[2]	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

1 A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

2 Reprogramming of a flash memory array block prior to erase is not required.

2.5 EzPort Electrical Specifications

Table 25. EzPort Electrical Specifications

Name	Characteristic	Min	Max	Unit
EP1	EPCK frequency of operation (all commands except READ)	—	f_{sys} / 2	MHz
EP1a	EPCK frequency of operation (READ command)	—	f_{sys} / 8	MHz
EP2	EPCS_b negation to next EPCS_b assertion	2 × T_{cyc}	—	ns
EP3	EPCS_B input valid to EPCK high (setup)	5	—	ns
EP4	EPCK high to EPCS_B input invalid (hold)	5	—	ns
EP5	EPD input valid to EPCK high (setup)	2	—	ns
EP6	EPCK high to EPD input invalid (hold)	5	—	ns
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

2.6 ESD Protection

Table 26. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD target for Human Body Model	HBM	2000	V
ESD target for Machine Model	MM	200	V
HBM circuit description	R_{series}	1500	Ω
	C	100	pF
MM circuit description	R_{series}	0	Ω
	C	200	pF
Number of pulses per pin (HBM) • Positive pulses • Negative pulses	 — —	 1 1	—
Number of pulses per pin (MM) • Positive pulses • Negative pulses	 — —	 3 3	—
Interval of pulses	—	1	sec

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

2.7 DC Electrical Specifications

Table 27. DC Electrical Specifications [1]

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	3.0	3.6	V
Standby voltage	V_{STBY}	1.8	3.5	V
Input high voltage	V_{IH}	$0.7 \times V_{DD}$	4.0	V
Input low voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DD}$	V
Input hysteresis[2]	V_{HYS}	$0.06 \times V_{DD}$	—	mV
Low-voltage detect trip voltage (V_{DD} falling)	V_{LVD}	2.15	2.3	V
Low-voltage detect hysteresis (V_{DD} rising)	V_{LVDHYS}	60	120	mV
Input leakage current $V_{in} = V_{DD}$ or V_{SS}, digital pins	I_{in}	–1.0	1.0	μA
Output high voltage (all input/output and all output pins) $I_{OH} = –2.0$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (all input/output and all output pins) $I_{OL} = 2.0$mA	V_{OL}	—	0.5	V

Table 27. DC Electrical Specifications (continued)[1]

Characteristic	Symbol	Min	Max	Unit
Output high voltage (high drive) I_{OH} = -5 mA	V_{OH}	V_{DD} – 0.5	—	V
Output low voltage (high drive) I_{OL} = 5 mA	V_{OL}	—	0.5	V
Output high voltage (low drive) I_{OH} = -2 mA	V_{OH}	V_{DD} - 0.5	—	V
Output low voltage (low drive) I_{OL} = 2 mA	V_{OL}	—	0.5	V
Weak internal pull Up device current, tested at V_{IL} Max.[3]	I_{APU}	–10	–130	µA
Input Capacitance [4] • All input-only pins • All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to Table 28 for additional PLL specifications.
2 Only for pins: IRQ1, IRQ2. IRQ3, IRQ4, IRQ5, IRQ6. IRQ7, RSTIN_B, RCON_B, PCS0, SCK, I2C_SDA, I2C_SCL, TCLK, TRST_B, TEST
3 Refer toTable 3 for pins having internal pull-up devices.
4 This parameter is characterized before qualification rather than 100% tested.

2.8 Clock Source Electrical Specifications

Table 28. Oscillator and PLL Electrical Specifications

(V_{DD} and V_{DDPLL} = 2.7 to 3.6 V, V_{SS} = V_{SSPLL} = 0 V)

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External[1]	 $f_{crystal}$ f_{ext}	 1 0	 25.0[2] 50-80	MHz
PLL reference frequency range	f_{ref_pll}	2	10.0	MHz
System frequency [3] • External clock mode • On-chip PLL frequency	f_{sys}	 0 f_{ref} / 32	 50-80[4] 50-80[4]	MHz
Loss of reference frequency [5, 7]	f_{LOR}	100	1000	kHz
Self clocked mode frequency [6]	f_{SCM}	1	5	MHz
Crystal start-up time [7, 8]	t_{cst}	—	0.1	ms
EXTAL input high voltage • External reference	V_{IHEXT}	 2.0	 3.0[2]	V
EXTAL input low voltage • External reference	V_{ILEXT}	 V_{SS}	 0.8	V
PLL lock time[4,9]	t_{lpll}	—	500	µs
Duty cycle of reference [4]	t_{dc}	40	60	% f_{ref}

Table 28. Oscillator and PLL Electrical Specifications (continued)

(V_{DD} and V_{DDPLL} = 2.7 to 3.6 V, V_{SS} = V_{SSPLL} = 0 V)

Characteristic	Symbol	Min	Max	Unit
Frequency un-LOCK range	f_{UL}	–1.5	1.5	% f_{ref}
Frequency LOCK range	f_{LCK}	–0.75	0.75	% f_{ref}
CLKOUT period jitter [4, 5, 10, 11], measured at f_{SYS} Max • Peak-to-peak (clock edge to clock edge) • Long term (averaged over 2 ms interval)	C_{jitter}	 — —	 10 .01	% f_{sys}
On-chip oscillator frequency	f_{oco}	7.84	8.16	MHz

1 In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

2 This value has been updated.

3 All internal registers retain data at 0 Hz.

4 Depending on packaging; see the orderable part number summary.

5 Loss of Reference Frequency is the reference frequency detected internally, which transitions the PLL into self clocked mode.

6 Self clocked mode frequency is the frequency at which the PLL operates when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

7 This parameter is characterized before qualification rather than 100% tested.

8 Proper PC board layout procedures must be followed to achieve specifications.

9 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

10 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{jitter} percentage for a given interval.

11 Based on slow system clock of 40 MHz measured at f_{sys} max.

2.9 USB Operation

Table 29. USB Operation Specifications

Characteristic	Symbol	Value	Unit
Minimum core speed for USB operation	$f_{sys\_USB\_min}$	16	MHz

2.10 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, timer, UART, Interrupt and USB interfaces. When in GPIO mode, the timing specification for these pins is given in Table 30 and Figure 5.

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive
- 25 pF / 25 Ω for low drive

Table 30. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

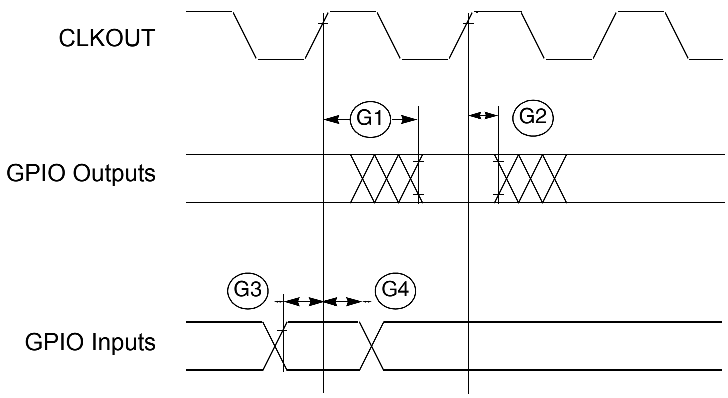


Figure 5. GPIO Timing

2.11 Reset Timing

Table 31. Reset and Configuration Override Timing

(V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V, $T_A = T_L$ to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{RSTI}$ input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{RSTI}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{RSTI}$ input valid time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{RSTO}$ Valid	t_{CHROV}	—	10	ns

1 All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

2 During low power STOP, the synchronizers for the $\overline{RSTI}$ input are bypassed and $\overline{RSTI}$ is asserted asynchronously to the system. Thus, $\overline{RSTI}$ must be held a minimum of 100 ns.

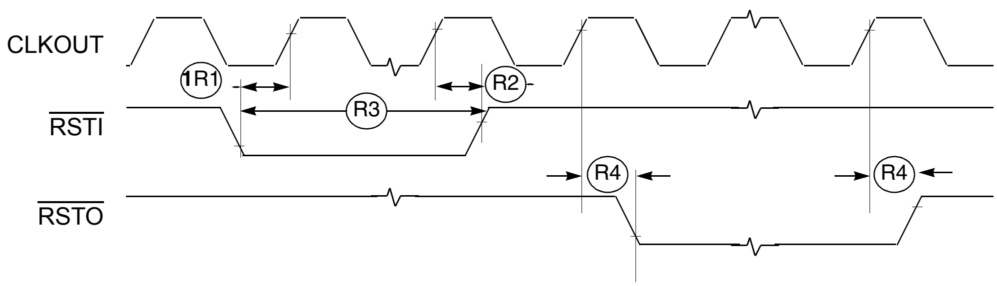


Figure 6. $\overline{RSTI}$ and Configuration Override Timing

2.12 I²C Input/Output Timing Specifications

Table 32 lists specifications for the I²C input timing parameters shown in Figure 7.

Table 32. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11	Start condition hold time	$2 \times t_{CYC}$	—	ns
I2	Clock low period	$8 \times t_{CYC}$	—	ns
I3	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	$4 \times t_{CYC}$	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	$2 \times t_{CYC}$	—	ns
I9	Stop condition setup time	$2 \times t_{CYC}$	—	ns

Table 33 lists specifications for the I²C output timing parameters shown in Figure 7.

Table 33. I²C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11[1]	Start condition hold time	$6 \times t_{CYC}$	—	ns
I2[1]	Clock low period	$10 \times t_{CYC}$	—	ns
I3[2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4[1]	Data hold time	$7 \times t_{CYC}$	—	ns
I5[3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6[1]	Clock high time	$10 \times t_{CYC}$	—	ns
I7[1]	Data setup time	$2 \times t_{CYC}$	—	ns
I8[1]	Start condition setup time (for repeated start condition only)	$20 \times t_{CYC}$	—	ns
I9[1]	Stop condition setup time	$10 \times t_{CYC}$	—	ns

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 33. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 33 are minimum values.

2 Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

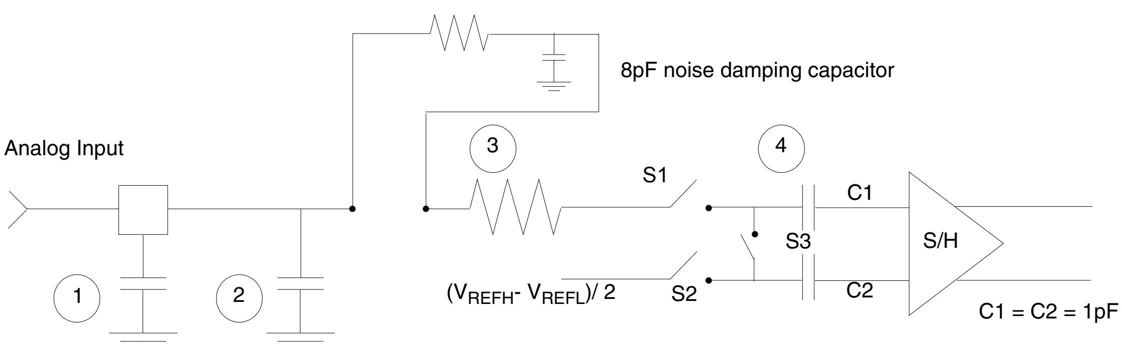
Table 34. ADC Parameters[1] (continued)

Name	Characteristic	Min	Typical	Max	Unit
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	67 to 70.3	—	dB
SINAD	Signal-to-noise plus distortion	—	61 to 63.9	—	dB
ENOB	Effective number of bits	9.1	10.6	—	Bits

[1] All measurements are preliminary pending full characterization, and made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
[2] INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$
[3] LSB = Least Significant Bit
[4] INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$
[5] Includes power-up of ADC and V_{REF}
[6] ADC clock cycles
[7] Current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.14 Equivalent Circuit for ADC Inputs

Figure 8 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed & S3 is open, one input of the sample and hold circuit moves to (V_{REFH}-V_{REFL})/2, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about (V_{REFH}-V_{REFL})/2. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF
3. Equivalent resistance for the channel select mux; 100 Ωs
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4pF
5. Equivalent input impedance, when the input is selected = $\frac{1}{(\text{ADC Clock Rate}) \times (1.4 \times 10^{-12})}$

Figure 8. Equivalent Circuit for A/D Loading

2.18 Debug AC Timing Specifications

Table 38 lists specifications for the debug AC timing parameters shown in Figure 14.

Table 38. Debug AC Timing Specification

Num	Characteristic	66/80 MHz		Units
		Min	Max	
D1	PST, DDATA to CLKOUT setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.5	—	ns
D3	DSI-to-DSCLK setup	$1 \times t_{CYC}$	—	ns
D4[1]	DSCLK-to-DSO hold	$4 \times t_{CYC}$	—	ns
D5	DSCLK cycle time	$5 \times t_{CYC}$	—	ns
D6	$\overline{\text{BKPT}}$ input data setup time to CLKOUT rise	4	—	ns
D7	$\overline{\text{BKPT}}$ input data hold time to CLKOUT rise	1.5	—	ns
D8	CLKOUT high to $\overline{\text{BKPT}}$ high Z	0.0	10.0	ns

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 14 shows real-time trace timing for the values in Table 38.

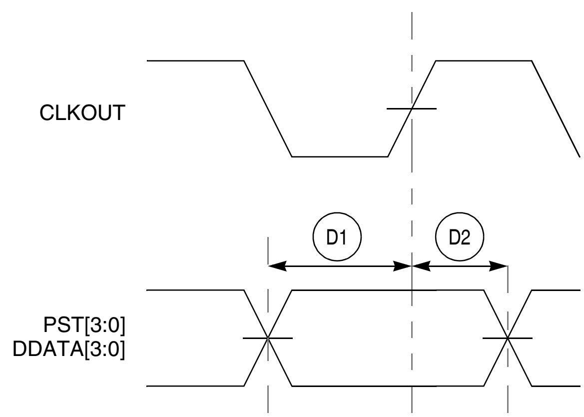


Figure 14. Real-Time Trace AC Timing

Figure 15 shows BDM serial port AC timing for the values in Table 38.

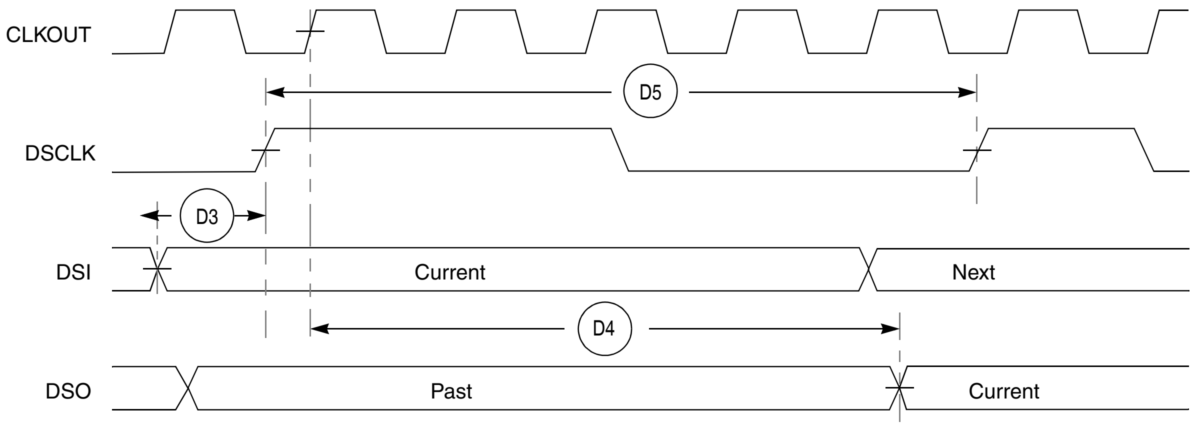
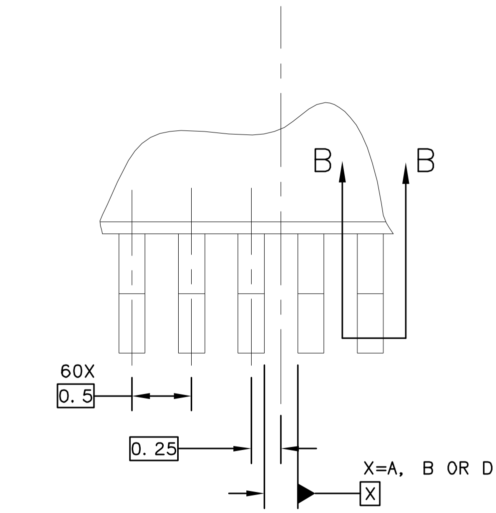


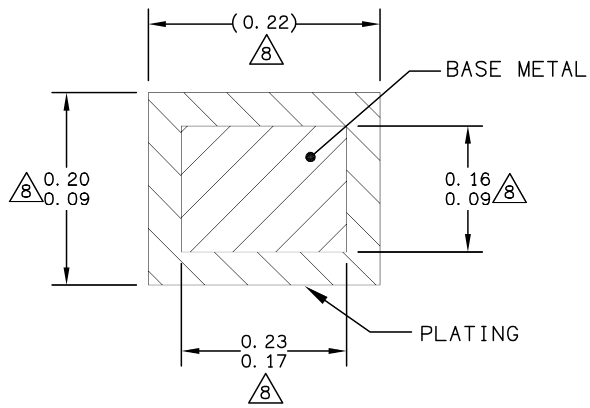
Figure 15. BDM Serial Port AC Timing

3 Mechanical Outline Drawings

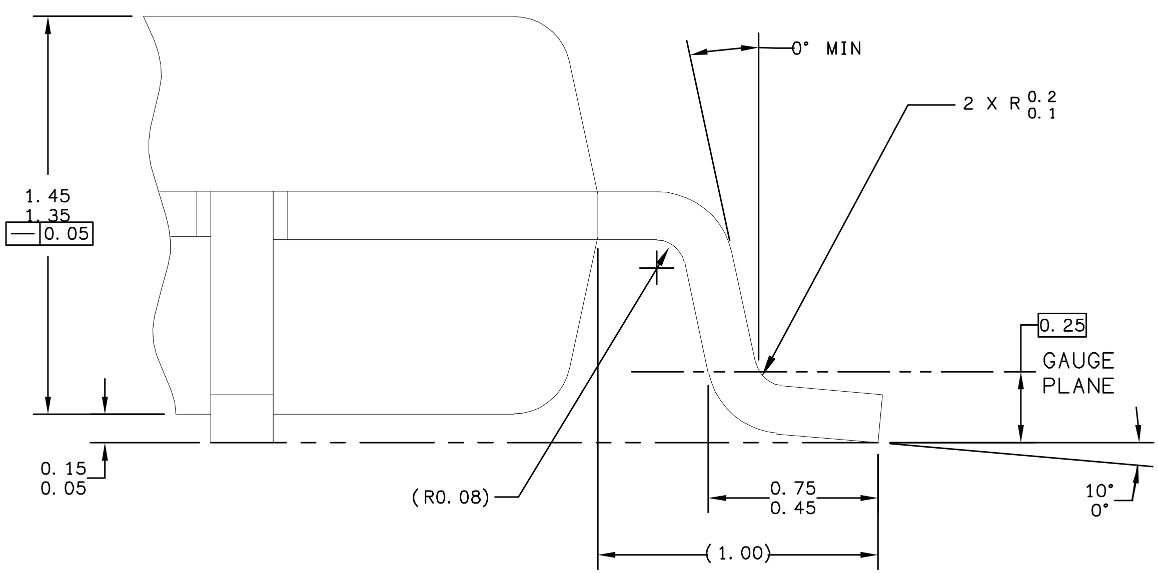
This section describes the physical properties of the device and its derivatives.



VIEW Y



SECTION B-B



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	CASE NUMBER: 840F-02	06 APR 2005
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3.2 64 QFN Package

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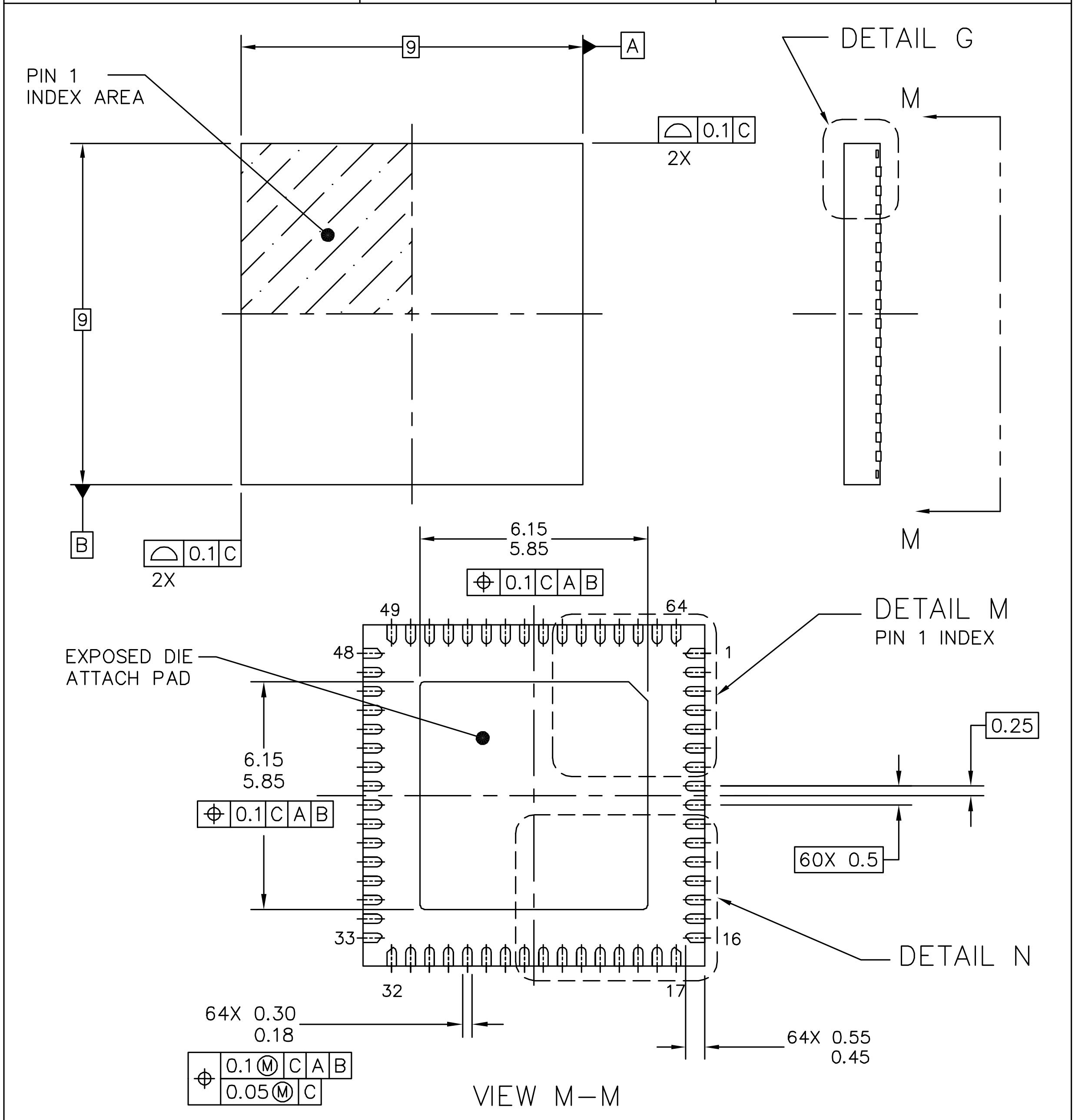

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	STANDARD: JEDEC MO–220 VMMD–3	
	PACKAGE CODE: 6200	SHEET: 1 OF 4

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
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	PACKAGE CODE: 6200	SHEET: 3 OF 4