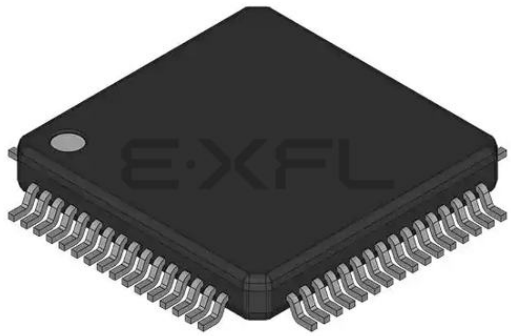

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf52212ae50

Table of Contents

  - Low-voltage detection (LVD)
  - JTAG
- Status flag indication of source of last reset

- Chip configuration module (CCM)
  - System configuration during reset
  - Selects one of six clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the core includes the multiply-accumulate (MAC) unit for improved signal processing capabilities. The MAC implements a three-stage arithmetic pipeline, optimized for 16x16 bit operations, with support for one 32-bit accumulator. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The MAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, access to debug information and real-time tracing capability is provided on 100-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. This device implements revision B+ of the ColdFire Debug Architecture.

The processor's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event. This ensures the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The device includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

1.2.13 General Purpose Timer (GPT)

The general purpose timer (GPT) is a four-channel timer module consisting of a 16-bit programmable counter driven by a seven-stage programmable prescaler. Each of the four channels can be configured for input capture or output compare. Additionally, channel three, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator.

1.2.14 Periodic Interrupt Timers (PIT0 and PIT1)

The two periodic interrupt timers (PIT0 and PIT1) are 16-bit timers that provide interrupts at regular intervals with minimal processor intervention. Each timer can count down from the value written in its PIT modulus register or it can be a free-running down-counter.

1.2.15 Real-Time Clock (RTC)

The Real-Time Clock (RTC) module maintains the system (time-of-day) clock and provides stopwatch, alarm, and interrupt functions. It includes full clock features: seconds, minutes, hours, days and supports a host of time-of-day interrupt functions along with an alarm interrupt.

1.2.16 Pulse-Width Modulation (PWM) Timers

The device has an 8-channel, 8-bit PWM timer. Each channel has a programmable period and duty cycle as well as a dedicated counter. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The timer supports PCM mode, which results in superior signal quality when compared to that of a conventional PWM. The PWM outputs have programmable polarity, and can be programmed as left aligned outputs or center aligned outputs. For higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.17 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.18 Backup Watchdog Timer

The backup watchdog timer is an independent 16-bit timer that, like the software watchdog timer, facilitates recovery from runaway code. This timer is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown. The backup watchdog timer can be clocked by either the relaxation oscillator or the system clock.

1.2.19 Phase-Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

Table 2. Orderable Part Number Summary (continued)

Freescale Part Number	Description	Speed (MHz)	Flash/SRAM (Kbytes)	Package	Temp range (°C)
MCF52211CVM66	MCF52211 Microcontroller, 2 UARTs	66	128 / 16	81 MAPBGA	-40 to +85
MCF52211CVM80	MCF52211 Microcontroller, 2 UARTs	80	128 / 16	81 MAPBGA	-40 to +85
MCF52212CAE50	MCF52212 Microcontroller, 2 UARTs	50	64 / 8	64 LQFP	-40 to +85
MCF52212AE50	MCF52212 Microcontroller, 2 UARTs	50	64 / 8	64 LQFP	0 to +70
MCF52213CAE50	MCF52213 Microcontroller, 2 UARTs	50	128 / 8	64 LQFP	-40 to +85
MCF52213AE50	MCF52213 Microcontroller, 2 UARTs	50	128 / 8	64 LQFP	0 to +70

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
Interrupts	$\overline{\text{IRQ7}}$	—	—	GPIO	Low	FAST	—	95	C4	58
	$\overline{\text{IRQ6}}$	—	—	GPIO	Low	FAST	—	94	B4	—
	$\overline{\text{IRQ5}}$	—	—	GPIO	Low	FAST	—	91	A4	—
	$\overline{\text{IRQ4}}$	—	—	GPIO	Low	FAST	—	90	C5	57
	$\overline{\text{IRQ3}}$	—	—	GPIO	Low	FAST	—	89	A5	—
	$\overline{\text{IRQ2}}$	—	—	GPIO	Low	FAST	—	88	B5	—
	$\overline{\text{IRQ1}}$	SYNCA	USB_ALT_CLK	GPIO	High	FAST	pull-up[4]	87	C6	56
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	pull-down	26	J2	17
	TCLK/ PSTCLK	CLKOUT	—	—	High	FAST	pull-up[5]	64	C7	44
	TDI/DSI	—	—	—	N/A	N/A	pull-up[5]	79	B7	50
	TDO/DSO	—	—	—	High	FAST	—	80	A7	51
	TMS /$\overline{\text{BKPT}}$	—	—	—	N/A	N/A	pull-up[5]	76	A8	49
	$\overline{\text{TRST}}$ /DSCLK	—	—	—	N/A	N/A	pull-up[5]	85	B6	54
Mode Selection[6]	CLKMOD0	—	—	—	N/A	N/A	pull-down[6]	40	G5	24
	CLKMOD1	—	—	—	N/A	N/A	pull-down[6]	39	H5	—
	$\overline{\text{RCON}}$/ EZPCS	—	—	—	N/A	N/A	pull-up	21	G3	16

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
QSPI	QSPI_DIN/ EZPD	—	URXD1	GPIO	PDSR[2]	PSRR[2]	—	16	F3	12
	QSPI_DOUT/ EZPQ	—	UTXD1	GPIO	PDSR[1]	PSRR[1]	—	17	G1	13
	QSPI_CLK/ EZPCK	SCL	$\overline{\text{URTS1}}$	GPIO	PDSR[3]	PSRR[3]	pull-up[8]	18	G2	14
	QSPI_CS3	SYNCA	—	GPIO	PDSR[7]	PSRR[7]	pull-up/pull-down[7]	12	F1	—
	QSPI_CS2	—	—	GPIO	PDSR[6]	PSRR[6]	pull-up/pull-down[7]	13	F2	—
	QSPI_CS1	—	—	GPIO	PDSR[5]	PSRR[5]	—	19	H2	—
	QSPI_CS0	SDA	$\overline{\text{UCTS1}}$	GPIO	PDSR[4]	PSRR[4]	pull-up[8]	20	H1	15
Reset[9]	$\overline{\text{RSTI}}$	—	—	—	N/A	N/A	pull-up[9]	96	A3	59
	$\overline{\text{RSTO}}$	—	—	—	high	FAST	—	97	B3	60
Test	TEST	—	—	—	N/A	N/A	pull-down	5	C2	3
Timers, 16-bit	GPT3	—	PWM7	GPIO	PDSR[23]	PSRR[23]	pull-up[10]	63	D7	—
	GPT2	—	PWM5	GPIO	PDSR[22]	PSRR[22]	pull-up[10]	58	E8	—
	GPT1	—	PWM3	GPIO	PDSR[21]	PSRR[21]	pull-up[10]	33	J4	—
	GPT0	—	PWM1	GPIO	PDSR[20]	PSRR[20]	pull-up[10]	38	J5	—
Timers, 32-bit	DTIN3	DTOUT3	PWM6	GPIO	PDSR[19]	PSRR[19]	—	32	H3	19
	DTIN2	DTOUT2	PWM4	GPIO	PDSR[18]	PSRR[18]	—	31	J3	18
	DTIN1	DTOUT1	PWM2	GPIO	PDSR[17]	PSRR[17]	—	37	G4	23
	DTIN0	DTOUT0	PWM0	GPIO	PDSR[16]	PSRR[16]	—	36	H4	22
UART 0	$\overline{\text{UCTS0}}$	—	—	GPIO	PDSR[11]	PSRR[11]	—	6	C1	4
	$\overline{\text{URTS0}}$	—	—	GPIO	PDSR[10]	PSRR[10]	—	9	D3	7
	URXD0	RTC_EXTAL	—	GPIO	PDSR[9]	PSRR[9]	—	7	D1	5
	UTXD0	RTC_XTAL	—	GPIO	PDSR[8]	PSRR[8]	—	8	D2	6

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
UART 1	$\overline{\text{UCTS1}}$	SYNCA	URXD2	GPIO	PDSR[15]	PSRR[15]	—	98	C3	61
	$\overline{\text{URTS1}}$	SYNCB	UTXD2	GPIO	PDSR[14]	PSRR[14]	—	4	B1	2
	URXD1	—	—	GPIO	PDSR[13]	PSRR[13]	—	100	B2	63
	UTXD1	—	—	GPIO	PDSR[12]	PSRR[12]	—	99	A2	62
UART 2	$\overline{\text{UCTS2}}$	—	—	GPIO	PDSR[27]	PSRR[27]	—	27	—	—
	$\overline{\text{URTS2}}$	—	—	GPIO	PDSR[26]	PSRR[26]	—	30	—	—
	URXD2	—	—	GPIO	PDSR[25]	PSRR[25]	—	28	—	—
	UTXD2	—	—	GPIO	PDSR[24]	PSRR[24]	—	29	—	—
VSTBY	VSTBY	—	—	—	N/A	N/A	—	55	F8	37
USB	VDDUSB	—	—	—	N/A	N/A	—	62	D8	43
	VSSUSB	—	—	—	N/A	N/A	—	59	F7	40
	USB_DM	—	—	—	N/A	N/A	—	61	D9	42
	USB_DP	—	—	—	N/A	N/A	—	60	E9	41
VDD	VDD	—	—	—	N/A	N/A	—	1,2,14,22, 23,34,41, 57,68,81,93	D5,E3–E7, F5	1,10,20,39,52
VSS	VSS	—	—	—	N/A	N/A	—	3,15,24,25,35,42,56, 67,75,82,92	A1,A9,D4,D6,F4,F6,J1	11,21,38, 53,64

1 The PDSR and PSSR registers are described in the General Purpose I/O chapter. All programmable signals default to 2 mA drive and FAST slew rate in normal (single-chip) mode.
2 All signals have a pull-up in GPIO mode.
3 These signals are multiplexed on other pins.
4 For primary and GPIO functions only.
5 Only when JTAG mode is enabled.
6 CLKMOD0 and CLKMOD1 have internal pull-down resistors; however, the use of external resistors is very strongly recommended.
7 When these pins are configured for USB signals, they should use the USB transceiver's internal pull-up/pull-down resistors (see the description of the OTG_CTRL register). If these pins are not configured for USB signals, each pin should be pulled down externally using a 10 kΩ resistor.
8 For secondary and GPIO functions only.
9 $\overline{\text{RSTI}}$ has an internal pull-up resistor; however, the use of an external resistor is very strongly recommended.
10 For GPIO function. Primary Function has pull-up control within the GPT module.

1.3 Reset Signals

Table 4 describes signals used to reset the chip or as a reset indication.

Table 4. Reset Signals

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RSTI}}$	Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ for at least 8 CPU clock cycles immediately resets the CPU and peripherals.	I
Reset Out	$\overline{\text{RSTO}}$	Driven low for 1024 CPU clocks after the reset source has deasserted.	O

1.4 PLL and Clock Signals

Table 5 describes signals used to support the on-chip clock generation circuitry.

Table 5. PLL and Clock Signals

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Crystal oscillator or external clock input except when the on-chip relaxation oscillator is used.	I
Crystal	XTAL	Crystal oscillator output except when CLKMOD0=0, then sampled as part of the clock mode selection mechanism.	O
Clock Out	CLKOUT	This output signal reflects the internal system clock.	O

1.5 Mode Selection

Table 6 describes signals used in mode selection; Table 7 describes the particular clocking modes.

Table 6. Mode Selection Signals

Signal Name	Abbreviation	Function	I/O
Clock Mode Selection	CLKMOD[1:0]	Selects the clock boot mode.	I
Reset Configuration	RCON	The Serial Flash Programming mode is entered by asserting the $\overline{\text{RCON}}$ pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the flash memory which can be programmed from an external device.	
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I

Table 7. Clocking Modes

CLKMOD[1:0]	XTAL	Configure the clock mode.
00	0	PLL disabled, clock driven by external oscillator
00	1	PLL disabled, clock driven by on-chip oscillator

Table 7. Clocking Modes (continued)

CLKMOD[1:0]	XTAL	Configure the clock mode.
01	N/A	PLL disabled, clock driven by crystal
10	0	PLL in normal mode, clock driven by external oscillator[1]
10	1	Reserved[2]
11	N/A	PLL in normal mode, clock driven by crystal

1 The PLL pre-divider (CCHR+1) reset value is 6 and the PLL input reference range is 2–10 MHz, so in order to boot with the PLL enabled, the external clock or crystal frequency needs to be greater than 12 MHz. MCF5221x devices cannot boot with PLL enabled from an external clock or crystal oscillator with frequency less than 12 MHz. This constraint does not apply to booting with PLL disabled.

2 Cannot boot from the Internal 8 MHz Relaxation oscillator with the PLL enabled. Refer Note1. Thus this mode has been removed from the table.

1.6 External Interrupt Signals

Table 8 describes the external interrupt signals.

Table 8. External Interrupt Signals

Signal Name	Abbreviation	Function	I/O
External Interrupts	$\overline{\text{IRQ}}$[7:1]	External interrupt sources.	I

1.7 Queued Serial Peripheral Interface (QSPI)

Table 9 describes the QSPI signals.

Table 9. Queued Serial Peripheral Interface (QSPI) Signals

Signal Name	Abbreviation	Function	I/O
QSPI Synchronous Serial Output	QSPI_DOUT	Provides the serial data from the QSPI and can be programmed to be driven on the rising or falling edge of QSPI_CLK.	O
QSPI Synchronous Serial Data Input	QSPI_DIN	Provides the serial data to the QSPI and can be programmed to be sampled on the rising or falling edge of QSPI_CLK.	I
QSPI Serial Clock	QSPI_CLK	Provides the serial clock from the QSPI. The polarity and phase of QSPI_CLK are programmable.	O
Synchronous Peripheral Chip Selects	QSPI_CS[3:0]	QSPI peripheral chip select; can be programmed to be active high or low.	O

1.8 USB On-the-Go

This device is compliant with industry standard USB 2.0 specification.

1.9 I^2C I/O Signals

Table 10 describes the I^2C serial interface module signals.

1.12 ADC Signals

Table 13 describes the signals of the Analog-to-Digital Converter.

Table 13. ADC Signals

Signal Name	Abbreviation	Function	I/O
Analog Inputs	AN[7:0]	Inputs to the analog-to-digital converter.	I
Analog Reference	V_{RH}	Reference voltage high and low inputs.	I
	V_{RL}		I
Analog Supply	V_{DDA}	Isolate the ADC circuitry from power supply noise.	—
	V_{SSA}		—
ADC Sync Inputs	SYNCA / SYNCB	These signals can initiate an analog-to-digital conversion process.	I

1.13 General Purpose Timer Signals

Table 14 describes the general purpose timer signals.

Table 14. GPT Signals

Signal Name	Abbreviation	Function	I/O
General Purpose Timer Input/Output	GPT[3:0]	Inputs to or outputs from the general purpose timer module.	I/O

1.14 Pulse Width Modulator Signals

Table 15 describes the PWM signals.

Table 15. PWM Signals

Signal Name	Abbreviation	Function	I/O
PWM Output Channels	PWM[7:0]	Pulse width modulated output for PWM channels.	O

1.15 Debug Support Signals

These signals are used as the interface to the on-chip JTAG controller and the BDM logic.

Table 16. Debug Support Signals

Signal Name	Abbreviation	Function	I/O
JTAG Enable	JTAG_EN	Select between debug module and JTAG signals at reset.	I
Test Reset	$\overline{\text{TRST}}$	This active-low signal is used to initialize the JTAG logic asynchronously.	I
Test Clock	TCLK	Used to synchronize the JTAG logic.	I
Test Mode Select	TMS	Used to sequence the JTAG state machine. TMS is sampled on the rising edge of TCLK.	I
Test Data Input	TDI	Serial input for test instructions and data. TDI is sampled on the rising edge of TCLK.	I

Table 16. Debug Support Signals (continued)

Signal Name	Abbreviation	Function	I/O
Test Data Output	TDO	Serial output for test instructions and data. TDO is tri-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.	O
Development Serial Clock	DSCLK	Development Serial Clock - Internally synchronized input. (The logic level on DSCLK is validated if it has the same value on two consecutive rising bus clock edges.) Clocks the serial communication port to the debug module during packet transfers. Maximum frequency is PSTCLK/5. At the synchronized rising edge of DSCLK, the data input on DSI is sampled and DSO changes state.	I
Breakpoint	$\overline{\text{BKPT}}$	Breakpoint - Input used to request a manual breakpoint. Assertion of $\overline{\text{BKPT}}$ puts the processor into a halted state after the current instruction completes. Halt status is reflected on processor status/debug data signals (PST[3:0] and PSTDDATA[7:0]) as the value 0xF. If CSR[BKD] is set (disabling normal $\overline{\text{BKPT}}$ functionality), asserting $\overline{\text{BKPT}}$ generates a debug interrupt exception in the processor.	I
Development Serial Input	DSI	Development Serial Input - Internally synchronized input that provides data input for the serial communication port to the debug module, after the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output - Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock - Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, and PST and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be reenabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical AND of PST[3:0]. The CLKOUT signal can be used by the development system to know when to sample ALLPST.	O

1.16 EzPort Signal Descriptions

Table 17 contains a list of EzPort external signals.

Table 17. EzPort Signal Descriptions

Signal Name	Abbreviation	Function	I/O
EzPort Clock	EZPCK	Shift clock for EzPort transfers.	I
EzPort Chip Select	EZPCS	Chip select for signalling the start and end of serial transfers.	I
EzPort Serial Data In	EZPD	EZPD is sampled on the rising edge of EZPCK.	I
EzPort Serial Data Out	EZPQ	EZPQ transitions on the falling edge of EZPCK.	O

1.17 Power and Ground Pins

The pins described in Table 18 provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

Table 18. Power and Ground Pins

Signal Name	Abbreviation	Function
PLL Analog Supply	VDDPLL, VSSPLL	Dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply.
Positive Supply	VDD	These pins supply positive power to the core logic.
Ground	VSS	This pin is the negative supply (ground) to the chip.

1 θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

3 Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

4 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A = ambient temperature, °C

Θ_{JA} = package thermal resistance, junction-to-ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, watts

$P_{I/O}$ = power dissipation on input and output pins — user determined, watts

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.4 Flash Memory Characteristics

The flash memory characteristics are shown in Table 23 and Table 24.

Table 23. SGFM Flash Program and Erase Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{sys(R)}$	0	—	50–80[1]	MHz
System clock (program/erase)[2]	$f_{sys(P/E)}$	0.15	—	102.4	MHz

1 Depending on packaging; see the orderable part number summary.

2 Refer to the flash memory section for more information

Figure 7 shows timing for the values in Table 32 and Table 33.

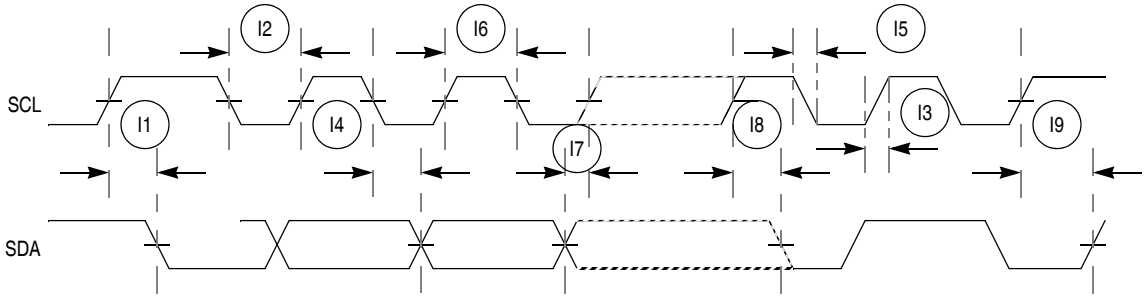


Figure 7. I²C Input/Output Timings

2.13 Analog-to-Digital Converter (ADC) Parameters

Table 34 lists specifications for the analog-to-digital converter.

Table 34. ADC Parameters[1]

Name	Characteristic	Min	Typical	Max	Unit
V_{REFL}	Low reference voltage	V_{SS}	—	V_{REFH}	V
V_{REFH}	High reference voltage	V_{REFL}	—	V_{DDA}	V
V_{DDA}	ADC analog supply voltage	3.0	3.3	3.6	V
V_{ADIN}	Input voltages	V_{REFL}	—	V_{REFH}	V
RES	Resolution	12	—	12	Bits
INL	Integral non-linearity (full input signal range)[2]	—	±2.5	±3	LSB[3]
INL	Integral non-linearity (10% to 90% input signal range)[4]	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	–1 < DNL < +1	<+1	LSB
Monotonicity		GUARANTEED			
f_{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R_{AD}	Conversion range	V_{REFL}	—	V_{REFH}	V
t_{ADPU}	ADC power-up time[5]	—	6	13	t_{AIC} cycles[6]
t_{REC}	Recovery from auto standby	—	0	1	t_{AIC} cycles
t_{ADC}	Conversion time	—	6	—	t_{AIC} cycles
t_{ADS}	Sample time	—	1	—	t_{AIC} cycles
C_{ADI}	Input capacitance	—	See Figure 8	—	pF
X_{IN}	Input impedance	—	See Figure 8	—	W
I_{ADI}	Input injection current[7], per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	mA
V_{OFFSET}	Offset voltage internal reference	—	±8	±15	mV
E_{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	9	mV
SNR	Signal-to-noise ratio	—	62 to 66	—	dB

Table 37. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

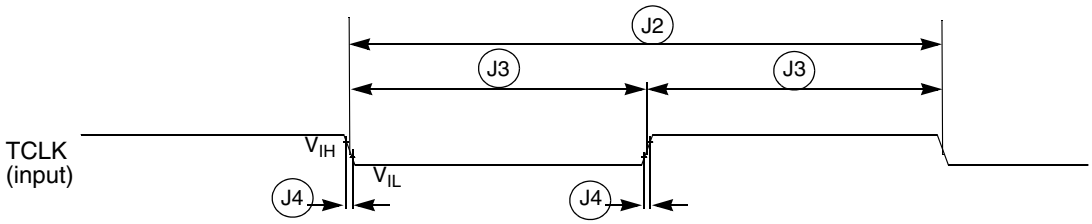


Figure 10. Test Clock Input Timing

2.18 Debug AC Timing Specifications

Table 38 lists specifications for the debug AC timing parameters shown in Figure 14.

Table 38. Debug AC Timing Specification

Num	Characteristic	66/80 MHz		Units
		Min	Max	
D1	PST, DDATA to CLKOUT setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.5	—	ns
D3	DSI-to-DSCLK setup	$1 \times t_{CYC}$	—	ns
D4[1]	DSCLK-to-DSO hold	$4 \times t_{CYC}$	—	ns
D5	DSCLK cycle time	$5 \times t_{CYC}$	—	ns
D6	$\overline{\text{BKPT}}$ input data setup time to CLKOUT rise	4	—	ns
D7	$\overline{\text{BKPT}}$ input data hold time to CLKOUT rise	1.5	—	ns
D8	CLKOUT high to $\overline{\text{BKPT}}$ high Z	0.0	10.0	ns

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 14 shows real-time trace timing for the values in Table 38.

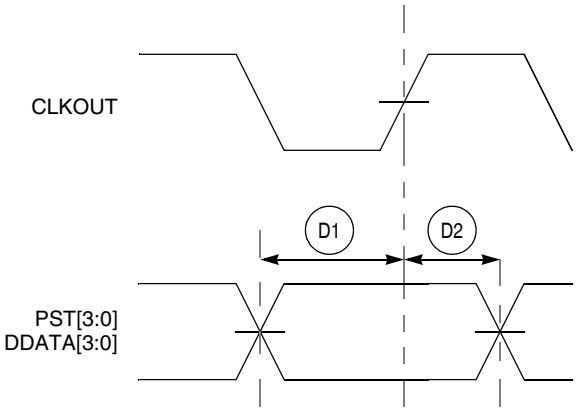
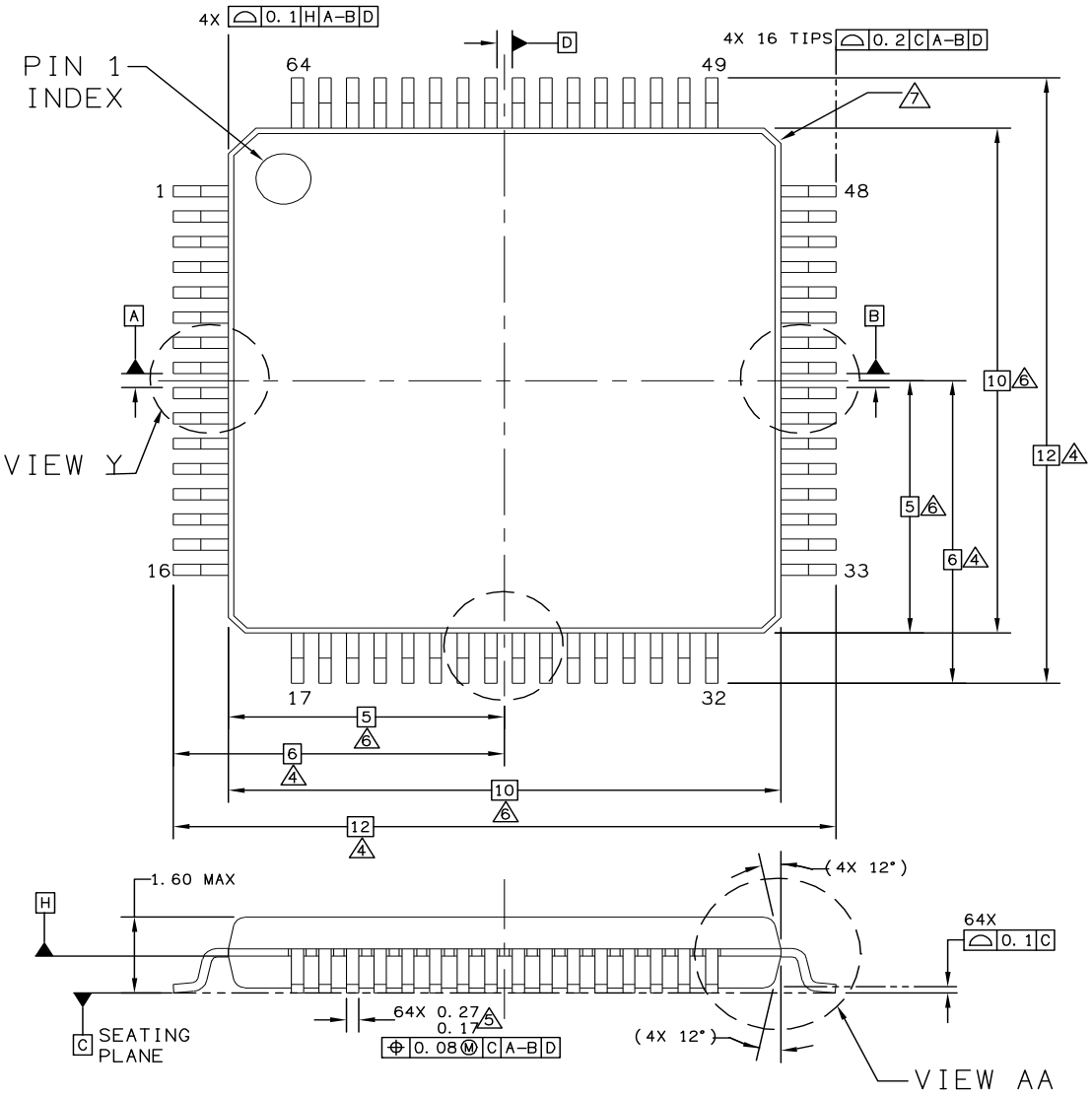


Figure 14. Real-Time Trace AC Timing

3.1 64-pin LQFP Package



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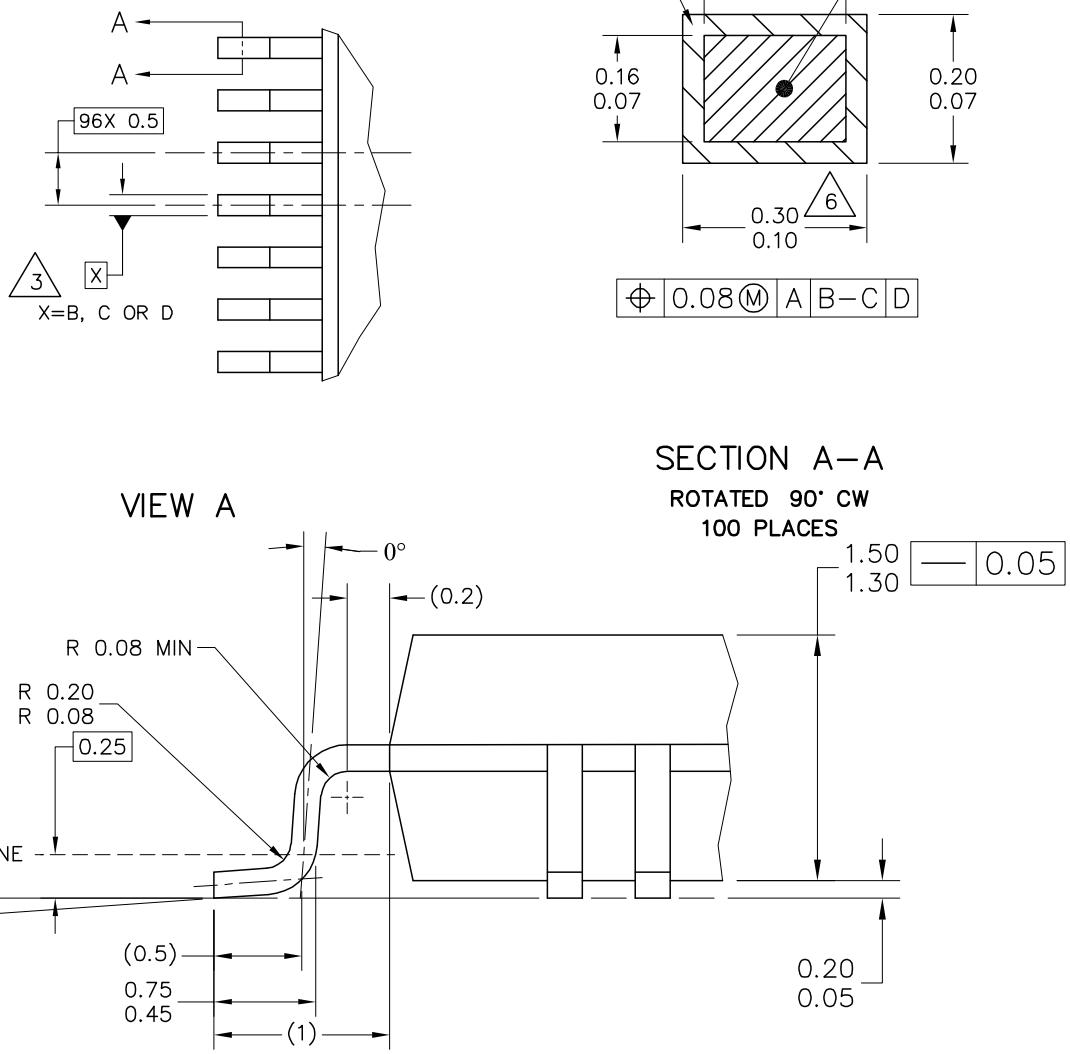
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D
	CASE NUMBER: 840F-02	06 APR 2005
	STANDARD: JEDEC MS-026 BCD	

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA10690D
		PAGE: 1740
	DO NOT SCALE THIS DRAWING	REV: O

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	CASE NUMBER: 1740–01	
	STANDARD: JEDEC MO–220 VMMD–3	
	PACKAGE CODE: 6200	SHEET: 3 OF 4



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE
TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23308W	REV: G
	CASE NUMBER: 983–03	07 APR 2005
	STANDARD: NON–JEDEC	

4 Revision History

Table 39. Revision History

Revision	Description
0	Initial public release.
1	• Formatting, layout, spelling, and grammar corrections. • Added information about the MCF52212 and MCF52213 devices. • Synchronized the “Pin Functions by Primary and Alternate Purpose” table in this document and the reference manual. • Added a specification for V_{DDUSB} to the “Absolute maximum ratings” table. • Added specifications for V_{LVD} and V_{LVDHYS} to the “DC electrical specifications” table. • Added the “USB Operation” section. • Changed the maximum value for $f_{sys(P/E)}$ in the “SGFM Flash Program and Erase Characteristics” table (was “66.67 or 80”, is “102.4”). • Changed the maximum value for $f_{sys(R)}$ in the “SGFM Flash Program and Erase Characteristics” table (was “66.67 or 80”, is “50–80”). • Changed the crystal start-up time in the “PLL Electrical Specifications” table (was 10 ms, is 0.1 ms). • Updated the current consumption specifications. • Updated the maximum temperature and added clarifying footnote. • Changed the absolute maximum rating for V_{STBY} (was “-0.3 to 4.0”, is “+1.8 to 3.5”). • Changed the maximum value for f_{sys} in the “PLL Electrical Specifications” table (was “66.67 or 80”, is “50–80”).
2	• Updated Clock generation features • Updated Table: Clocking Modes and added appropriate footnote • In Table: CLock Source Electrical Specifications, updated the following values: fcrystal, fext, fref_pll, EXTAL input high voltage (External reference)