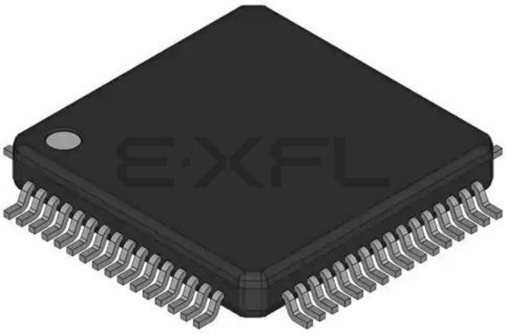

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf52213cae50

Table of Contents

1.1 Block Diagram

Figure 1 shows a top-level block diagram of the device. Package options for this family are described later in this document.

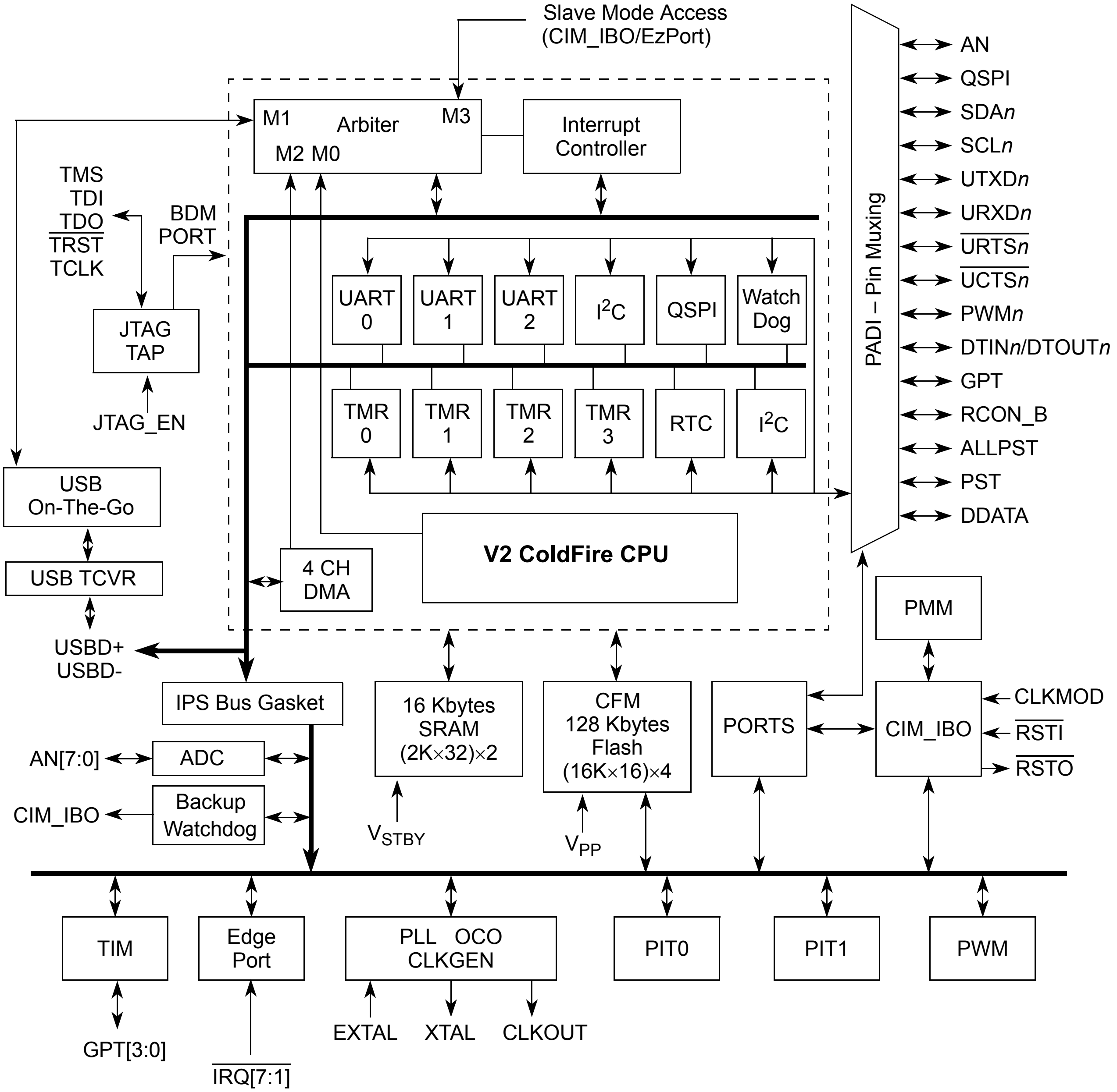


Figure 1. Block Diagram

1.2 Features

1.2.1 Feature Overview

The MCF52211 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data paths on-chip
  - Up to 80 MHz processor core frequency
  - 40 MHz and 33 MHz off-platform bus frequency
  - Sixteen general-purpose, 32-bit data and address registers
  - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
  - Multiply-Accumulate (MAC) unit with 32-bit accumulator to support $16\times16 \rightarrow 32$ or $32\times32 \rightarrow 32$ operations
- System debug support
  - Real-time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
  - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
  - Up to 16-Kbyte dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support
  - Up to 128 Kbytes of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used (except backup watchdog timer)
  - Software controlled disable of external clock output for low-power consumption
- Universal Serial Bus On-The-Go (USB OTG) dual-mode host and device controller
  - Full-speed / low-speed host controller
  - USB 1.1 and 2.0 compliant full-speed / low speed device controller
  - 16 bidirectional end points
  - DMA or FIFO data stream interfaces
  - Low power consumption
  - OTG protocol logic
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic with maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7 or 8 bits with even, odd, or no parity
  - Up to two stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
  - Transmit and receive FIFO buffers
- Two I^2C modules

  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I^2C bus
  - Master and slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to four chip selects available
  - Master mode operation only
  - Programmable bit rates up to half the CPU clock frequency
  - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
  - Eight analog input channels
  - 12-bit resolution
  - Minimum 1.125 µs conversion time
  - Simultaneous sampling of two channels for motor control applications
  - Single-scan or continuous operation
  - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit
  - Unused analog channels can be used as digital I/O
- Four 32-bit timers with DMA support
  - 12.5 ns resolution at 80 MHz
  - Programmable sources for clock input, including an external clock option
  - Programmable prescaler
  - Input capture capability with programmable trigger edge on input pin
  - Output compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts on input capture or output compare
  - DMA trigger capability on input capture or output compare
- Four-channel general purpose timer
  - 16-bit architecture
  - Programmable prescaler
  - Output pulse-widths variable from microseconds to seconds
  - Single 16-bit input pulse accumulator
  - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
  - Support for PCM mode (resulting in superior signal quality compared to conventional PWM)
  - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
  - Programmable period and duty cycle
  - Programmable enable/disable for each channel
  - Software selectable polarity for each channel
  - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
  - Programmable center or left aligned outputs on individual channels
  - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
  - Emergency shutdown

- Two periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Real-Time Clock (RTC)
  - Maintains system time-of-day clock
  - Provides stopwatch and alarm interrupt functions
- Software watchdog timer
  - 32-bit counter
  - Low-power mode support
- Backup watchdog timer (BWT)
  - Independent timer that can be used to help software recover from runaway code
  - 16-bit counter
  - Low-power mode support
- Clock generation features
  - Crystal, on-chip trimmed relaxation oscillator, or external oscillator reference options
  - Trimmed relaxation oscillator
  - Pre-divider capable of dividing the clock source frequency into the PLL reference frequency range
  - System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
  - Low power modes supported
  - 2^n ($0 \leq n \leq 15$) low-power divider for extremely low frequency operation
- Interrupt controller
  - Uniquely programmable vectors for all interrupt sources
  - Fully programmable level and priority for all peripheral interrupt sources
  - Seven external interrupt signals with fixed level and priority
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low-power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle-steal support
  - Software-programmable DMA requests for the UARTs (3) and 32-bit timers (4)
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock / loss of lock

Table 2. Orderable Part Number Summary (continued)

Freescale Part Number	Description	Speed (MHz)	Flash/SRAM (Kbytes)	Package	Temp range (°C)
MCF52211CVM66	MCF52211 Microcontroller, 2 UARTs	66	128 / 16	81 MAPBGA	-40 to +85
MCF52211CVM80	MCF52211 Microcontroller, 2 UARTs	80	128 / 16	81 MAPBGA	-40 to +85
MCF52212CAE50	MCF52212 Microcontroller, 2 UARTs	50	64 / 8	64 LQFP	-40 to +85
MCF52212AE50	MCF52212 Microcontroller, 2 UARTs	50	64 / 8	64 LQFP	0 to +70
MCF52213CAE50	MCF52213 Microcontroller, 2 UARTs	50	128 / 8	64 LQFP	-40 to +85
MCF52213AE50	MCF52213 Microcontroller, 2 UARTs	50	128 / 8	64 LQFP	0 to +70

Figure 3 shows the pinout configuration for the 81 MAPBGA.

	1	2	3	4	5	6	7	8	9
A	V_{SS}	UTXD1	$\overline{\text{RSTI}}$	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ3}}$	ALLPST	TDO	TMS	V_{SS}
B	$\overline{\text{URTS1}}$	URXD1	$\overline{\text{RSTO}}$	$\overline{\text{IRQ6}}$	$\overline{\text{IRQ2}}$	$\overline{\text{TRST}}$	TDI	V_{DD}PLL	EXTAL
C	$\overline{\text{UCTS0}}$	TEST	$\overline{\text{UCTS1}}$	$\overline{\text{IRQ7}}$	$\overline{\text{IRQ4}}$	$\overline{\text{IRQ1}}$	TCLK	V_{SS}PLL	XTAL
D	URXD0	UTXD0	$\overline{\text{URTS0}}$	V_{SS}	V_{DD}	V_{SS}	PWM7	GPT3	GPT2
E	SCL	SDA	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	PWM5	GPT1
F	QSPI_CS3	QSPI_CS2	QSPI_DIN	V_{SS}	V_{DD}	V_{SS}	GPT0	V_{STBY}	AN4
G	QSPI_DOUT	QSPI_CLK	$\overline{\text{RCON}}$	DTIN1	CLKMOD0	AN2	AN3	AN5	AN6
H	QSPI_CS0	QSPI_CS1	DTIN3	DTIN0	CLKMOD1	AN1	V_{SSA}	V_{DDA}	AN7
J	V_{SS}	JTAG_EN	DTIN2	PWM3	PWM1	AN0	V_{RL}	V_{RH}	V_{SSA}

Figure 3. 81 MAPBGA Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
QSPI	QSPI_DIN/ EZPD	—	URXD1	GPIO	PDSR[2]	PSRR[2]	—	16	F3	12
	QSPI_DOUT/ EZPQ	—	UTXD1	GPIO	PDSR[1]	PSRR[1]	—	17	G1	13
	QSPI_CLK/ EZPCK	SCL	$\overline{\text{URTS1}}$	GPIO	PDSR[3]	PSRR[3]	pull-up[8]	18	G2	14
	QSPI_CS3	SYNCA	—	GPIO	PDSR[7]	PSRR[7]	pull-up/pull-down[7]	12	F1	—
	QSPI_CS2	—	—	GPIO	PDSR[6]	PSRR[6]	pull-up/pull-down[7]	13	F2	—
	QSPI_CS1	—	—	GPIO	PDSR[5]	PSRR[5]	—	19	H2	—
	QSPI_CS0	SDA	$\overline{\text{UCTS1}}$	GPIO	PDSR[4]	PSRR[4]	pull-up[8]	20	H1	15
Reset[9]	$\overline{\text{RSTI}}$	—	—	—	N/A	N/A	pull-up[9]	96	A3	59
	$\overline{\text{RSTO}}$	—	—	—	high	FAST	—	97	B3	60
Test	TEST	—	—	—	N/A	N/A	pull-down	5	C2	3
Timers, 16-bit	GPT3	—	PWM7	GPIO	PDSR[23]	PSRR[23]	pull-up[10]	63	D7	—
	GPT2	—	PWM5	GPIO	PDSR[22]	PSRR[22]	pull-up[10]	58	E8	—
	GPT1	—	PWM3	GPIO	PDSR[21]	PSRR[21]	pull-up[10]	33	J4	—
	GPT0	—	PWM1	GPIO	PDSR[20]	PSRR[20]	pull-up[10]	38	J5	—
Timers, 32-bit	DTIN3	DTOUT3	PWM6	GPIO	PDSR[19]	PSRR[19]	—	32	H3	19
	DTIN2	DTOUT2	PWM4	GPIO	PDSR[18]	PSRR[18]	—	31	J3	18
	DTIN1	DTOUT1	PWM2	GPIO	PDSR[17]	PSRR[17]	—	37	G4	23
	DTIN0	DTOUT0	PWM0	GPIO	PDSR[16]	PSRR[16]	—	36	H4	22
UART 0	$\overline{\text{UCTS0}}$	—	—	GPIO	PDSR[11]	PSRR[11]	—	6	C1	4
	$\overline{\text{URTS0}}$	—	—	GPIO	PDSR[10]	PSRR[10]	—	9	D3	7
	URXD0	RTC_EXTAL	—	GPIO	PDSR[9]	PSRR[9]	—	7	D1	5
	UTXD0	RTC_XTAL	—	GPIO	PDSR[8]	PSRR[8]	—	8	D2	6

Table 17. EzPort Signal Descriptions

Signal Name	Abbreviation	Function	I/O
EzPort Clock	EZPCK	Shift clock for EzPort transfers.	I
EzPort Chip Select	EZPCS	Chip select for signalling the start and end of serial transfers.	I
EzPort Serial Data In	EZPD	EZPD is sampled on the rising edge of EZPCK.	I
EzPort Serial Data Out	EZPQ	EZPQ transitions on the falling edge of EZPCK.	O

1.17 Power and Ground Pins

The pins described in Table 18 provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

Table 18. Power and Ground Pins

Signal Name	Abbreviation	Function
PLL Analog Supply	VDDPLL, VSSPLL	Dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply.
Positive Supply	VDD	These pins supply positive power to the core logic.
Ground	VSS	This pin is the negative supply (ground) to the chip.

[1] θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

[2] Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

[3] Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

[4] Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[5] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

[6] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A = ambient temperature, °C
Θ_{JA} = package thermal resistance, junction-to-ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, watts
$P_{I/O}$ = power dissipation on input and output pins — user determined, watts

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^{\ 2} \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.4 Flash Memory Characteristics

The flash memory characteristics are shown in Table 23 and Table 24.

Table 23. SGFM Flash Program and Erase Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{sys(R)}$	0	—	50–80[1]	MHz
System clock (program/erase)[2]	$f_{sys(P/E)}$	0.15	—	102.4	MHz

[1] Depending on packaging; see the orderable part number summary.

[2] Refer to the flash memory section for more information

Table 24. SGFM Flash Module Life Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles[1] before failure	P/E	10,000[2]	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

[1] A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

[2] Reprogramming of a flash memory array block prior to erase is not required.

2.5 EzPort Electrical Specifications

Table 25. EzPort Electrical Specifications

Name	Characteristic	Min	Max	Unit
EP1	EPCK frequency of operation (all commands except READ)	—	f_{sys} / 2	MHz
EP1a	EPCK frequency of operation (READ command)	—	f_{sys} / 8	MHz
EP2	EPCS_b negation to next EPCS_b assertion	$2 \times T_{cyc}$	—	ns
EP3	EPCS_B input valid to EPCK high (setup)	5	—	ns
EP4	EPCK high to EPCS_B input invalid (hold)	5	—	ns
EP5	EPD input valid to EPCK high (setup)	2	—	ns
EP6	EPCK high to EPD input invalid (hold)	5	—	ns
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

Table 30. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

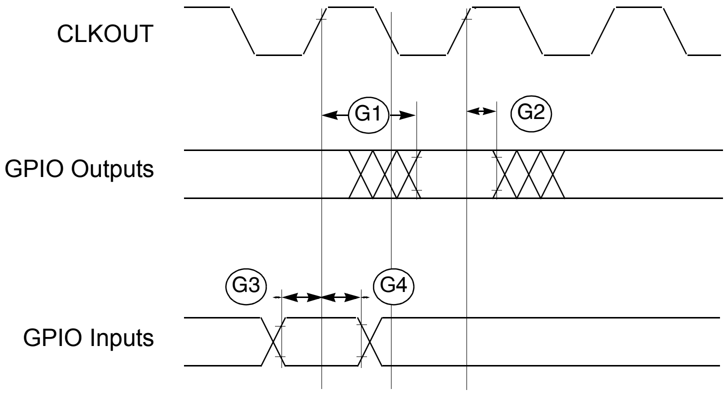


Figure 5. GPIO Timing

2.11 Reset Timing

Table 31. Reset and Configuration Override Timing

(V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V, $T_A = T_L$ to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RSTI}}$ input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RSTI}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RSTI}}$ input valid time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTO}}$ Valid	t_{CHROV}	—	10	ns

[1] All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

[2] During low power STOP, the synchronizers for the $\overline{\text{RSTI}}$ input are bypassed and $\overline{\text{RSTI}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RSTI}}$ must be held a minimum of 100 ns.

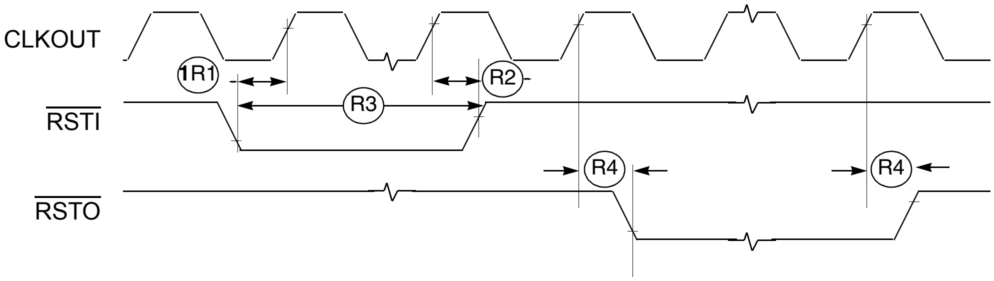


Figure 6. $\overline{\text{RSTI}}$ and Configuration Override Timing

2.12 I^{2}C Input/Output Timing Specifications

Table 32 lists specifications for the I^{2}C input timing parameters shown in Figure 7.

Table 32. I^{2}C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11	Start condition hold time	$2 \times t_{CYC}$	—	ns
I2	Clock low period	$8 \times t_{CYC}$	—	ns
I3	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	$4 \times t_{CYC}$	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	$2 \times t_{CYC}$	—	ns
I9	Stop condition setup time	$2 \times t_{CYC}$	—	ns

Table 33 lists specifications for the I^{2}C output timing parameters shown in Figure 7.

Table 33. I^{2}C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11[1]	Start condition hold time	$6 \times t_{CYC}$	—	ns
I2[1]	Clock low period	$10 \times t_{CYC}$	—	ns
I3[2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4[1]	Data hold time	$7 \times t_{CYC}$	—	ns
I5[3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6[1]	Clock high time	$10 \times t_{CYC}$	—	ns
I7[1]	Data setup time	$2 \times t_{CYC}$	—	ns
I8[1]	Start condition setup time (for repeated start condition only)	$20 \times t_{CYC}$	—	ns
I9[1]	Stop condition setup time	$10 \times t_{CYC}$	—	ns

[1] Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 33. The I^{2}C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 33 are minimum values.

[2] Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

[3] Specified at a nominal 50-pF load.

Figure 7 shows timing for the values in Table 32 and Table 33.

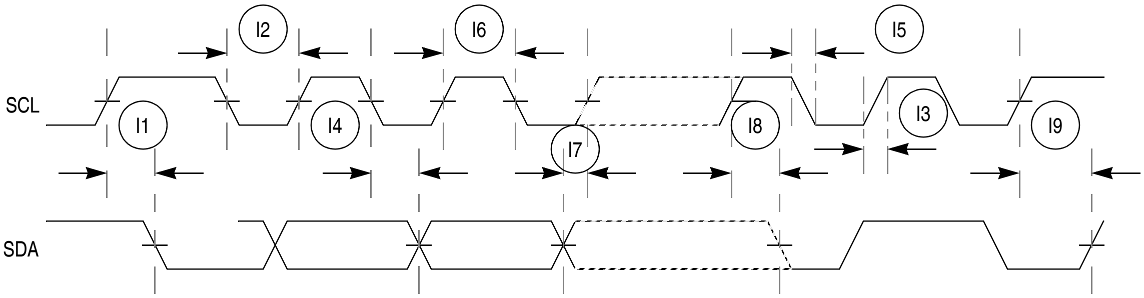


Figure 7. I^{2}C Input/Output Timings

2.13 Analog-to-Digital Converter (ADC) Parameters

Table 34 lists specifications for the analog-to-digital converter.

Table 34. ADC Parameters[1]

Name	Characteristic	Min	Typical	Max	Unit
V_{REFL}	Low reference voltage	V_{SS}	—	V_{REFH}	V
V_{REFH}	High reference voltage	V_{REFL}	—	V_{DDA}	V
V_{DDA}	ADC analog supply voltage	3.0	3.3	3.6	V
V_{ADIN}	Input voltages	V_{REFL}	—	V_{REFH}	V
RES	Resolution	12	—	12	Bits
INL	Integral non-linearity (full input signal range)[2]	—	±2.5	±3	LSB[3]
INL	Integral non-linearity (10% to 90% input signal range)[4]	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	–1 < DNL < +1	<+1	LSB
Monotonicity		GUARANTEED			
f_{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R_{AD}	Conversion range	V_{REFL}	—	V_{REFH}	V
t_{ADPU}	ADC power-up time[5]	—	6	13	t_{AIC} cycles[6]
t_{REC}	Recovery from auto standby	—	0	1	t_{AIC} cycles
t_{ADC}	Conversion time	—	6	—	t_{AIC} cycles
t_{ADS}	Sample time	—	1	—	t_{AIC} cycles
C_{ADI}	Input capacitance	—	See Figure 8	—	pF
X_{IN}	Input impedance	—	See Figure 8	—	W
I_{ADI}	Input injection current[7], per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	mA
V_{OFFSET}	Offset voltage internal reference	—	±8	±15	mV
E_{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	9	mV
SNR	Signal-to-noise ratio	—	62 to 66	—	dB

2.15 DMA Timers Timing Specifications

Table 35 lists timer module AC timings.

Table 35. Timer Module AC Timing Specifications

Name	Characteristic[1]	Min	Max	Unit
T1	DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time	3 × t_{CYC}	—	ns
T2	DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width	1 × t_{CYC}	—	ns

[1] All timing references to CLKOUT are given to its rising edge.

2.16 QSPI Electrical Specifications

Table 36 lists QSPI timings.

Table 36. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 36 correspond to Figure 9.

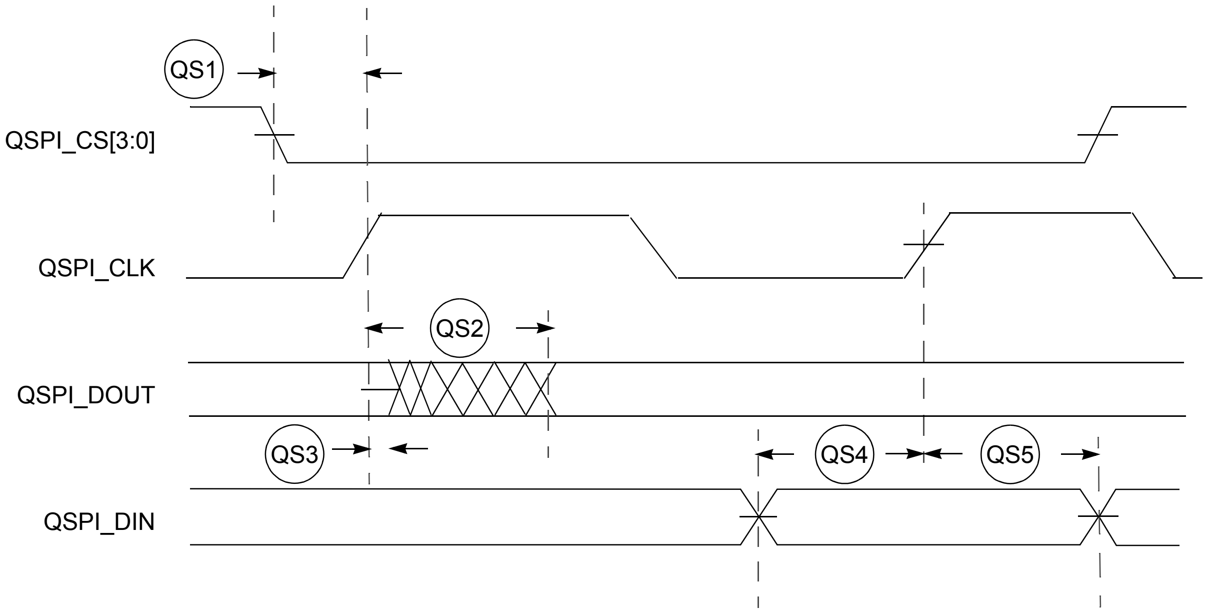


Figure 9. QSPI Timing

2.17 JTAG and Boundary Scan Timing

Table 37. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

[1] JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

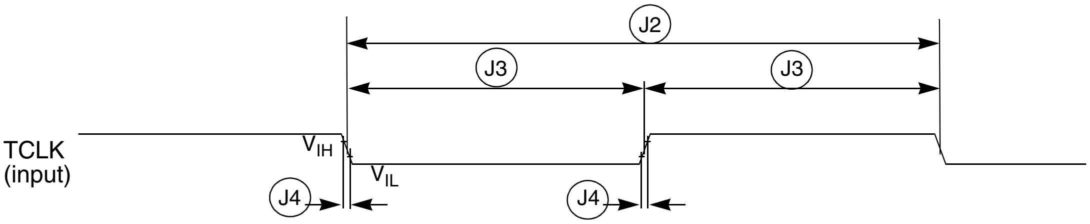


Figure 10. Test Clock Input Timing

2.18 Debug AC Timing Specifications

Table 38 lists specifications for the debug AC timing parameters shown in Figure 14.

Table 38. Debug AC Timing Specification

Num	Characteristic	66/80 MHz		Units
		Min	Max	
D1	PST, DDATA to CLKOUT setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.5	—	ns
D3	DSI-to-DSCLK setup	1 × t_{CYC}	—	ns
D4[1]	DSCLK-to-DSO hold	4 × t_{CYC}	—	ns
D5	DSCLK cycle time	5 × t_{CYC}	—	ns
D6	$\overline{\text{BKPT}}$ input data setup time to CLKOUT rise	4	—	ns
D7	$\overline{\text{BKPT}}$ input data hold time to CLKOUT rise	1.5	—	ns
D8	CLKOUT high to $\overline{\text{BKPT}}$ high Z	0.0	10.0	ns

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 14 shows real-time trace timing for the values in Table 38.

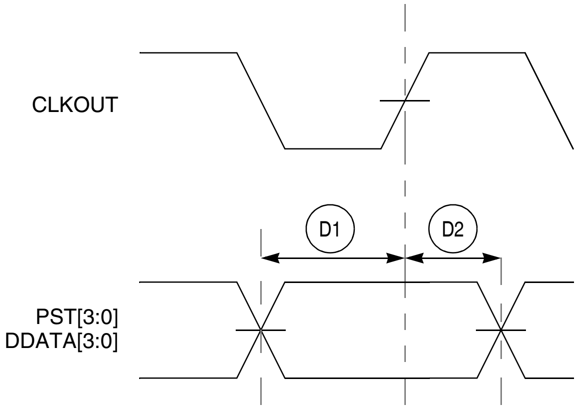
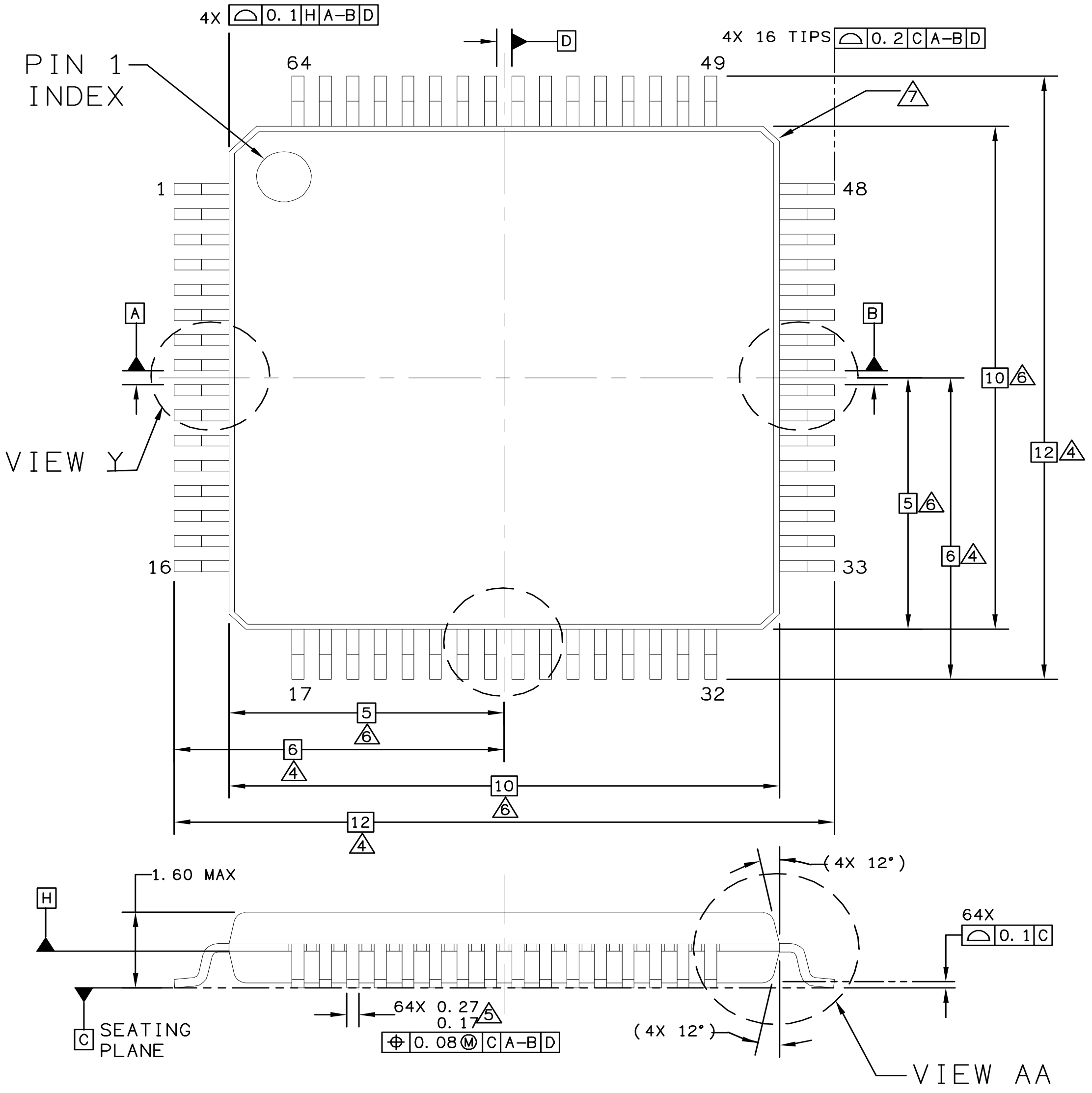


Figure 14. Real-Time Trace AC Timing

3.1 64-pin LQFP Package



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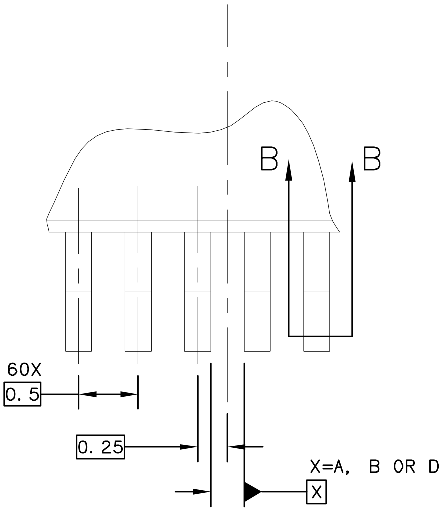
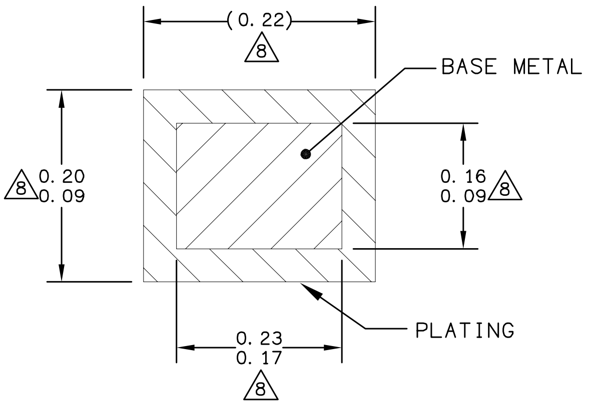
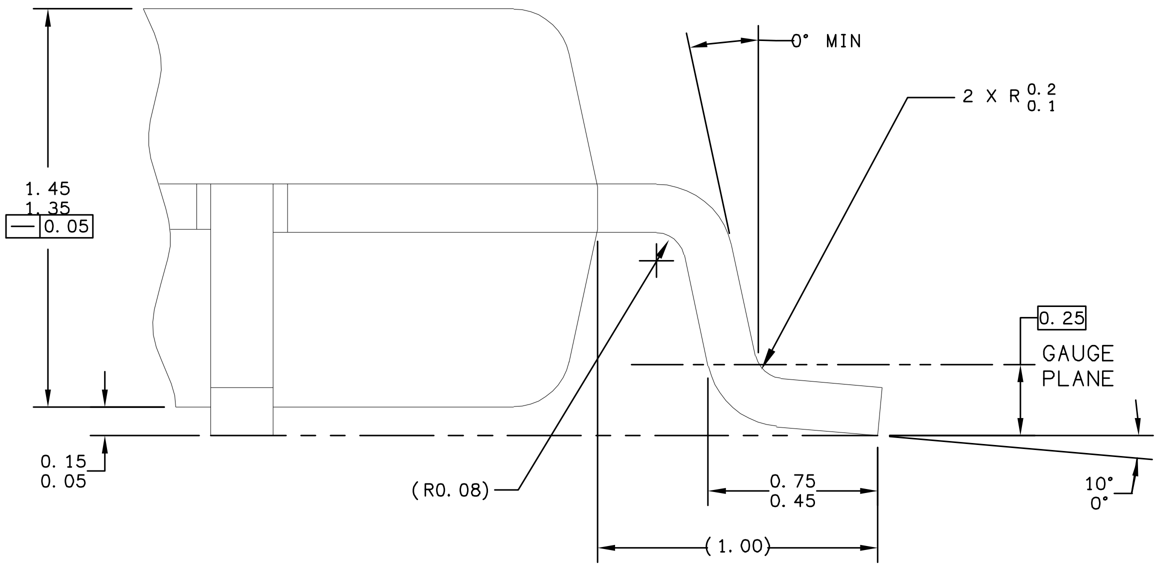
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D
	CASE NUMBER: 840F-02	06 APR 2005
	STANDARD: JEDEC MS-026 BCD	



VIEW Y



SECTION B–B



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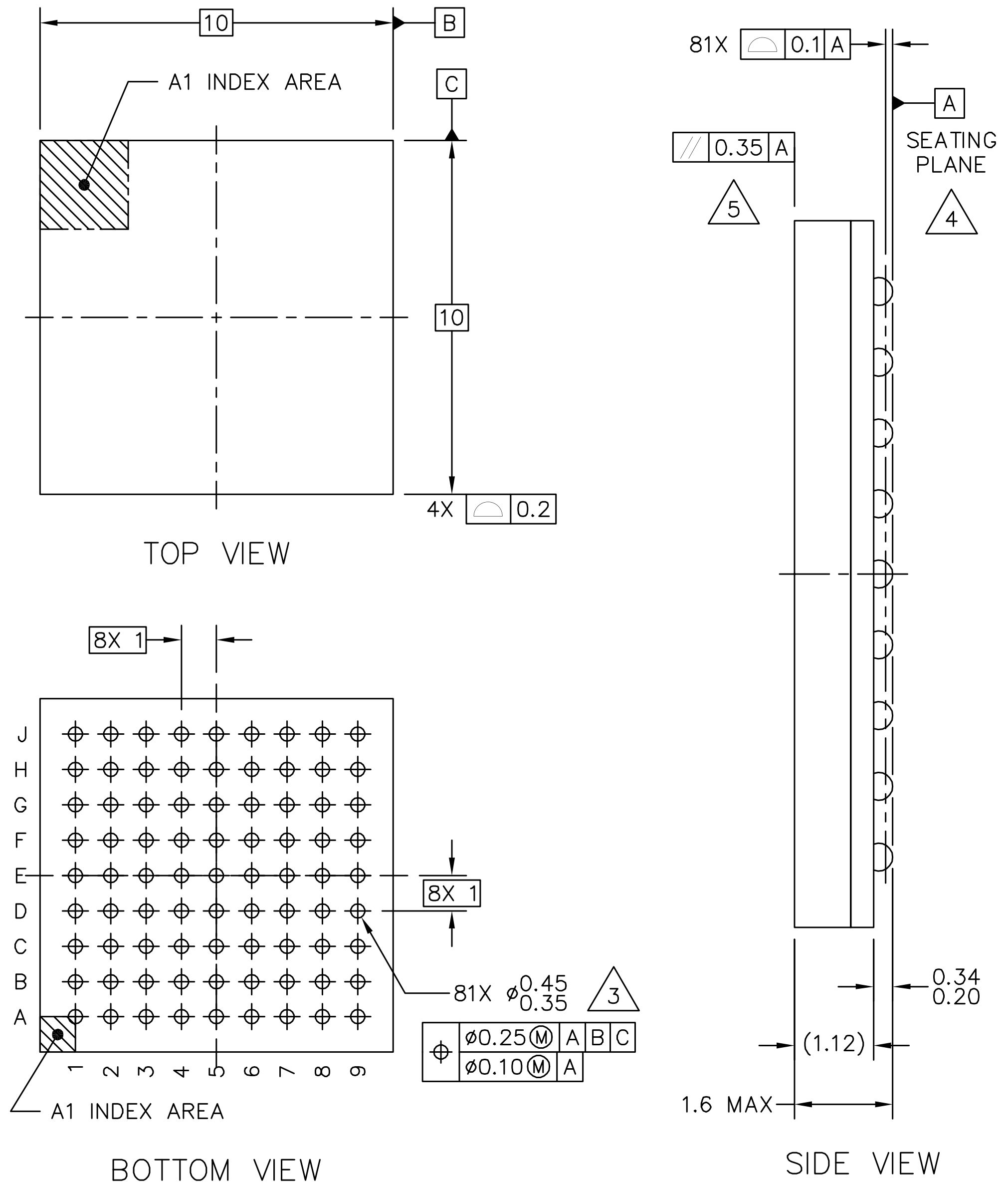
	CASE NUMBER: 840F–02	06 APR 2005
	STANDARD: JEDEC MS–026 BCD	

3.3 81 MAPBGA Package



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TITLE: PBGA, LOW PROFILE, 81 I/O, 10 X 10 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ASA10670D	REV: 0
	CASE NUMBER: 1662–01	04 FEB 2005
	STANDARD: NON–JEDEC	