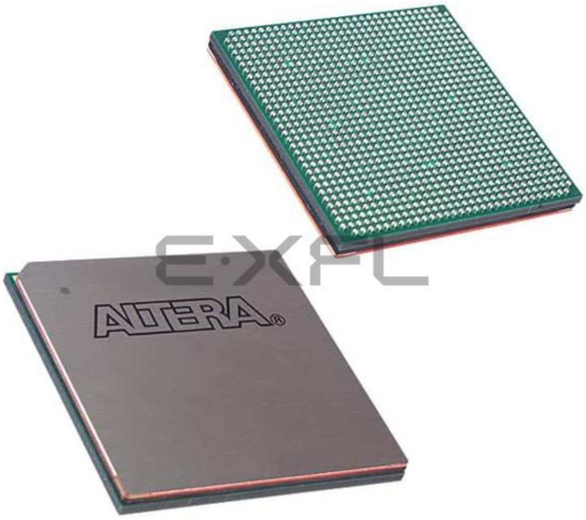


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6627
Number of Logic Elements/Cells	132540
Total RAM Bits	6747840
Number of I/O	742
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s130f1020c4

Stratix II devices are available in up to three speed grades, -3, -4, and -5, with -3 being the fastest. Table 1–5 shows Stratix II device speed-grade offerings.

Table 1–5. Stratix II Device Speed Grades

Device	Temperature Grade	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S30	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S60	Commercial	-3, -4, -5		-3, -4, -5		-3, -4, -5	
	Industrial	-4		-4		-4	
EP2S90	Commercial		-4, -5		-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S130	Commercial				-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S180	Commercial					-3, -4, -5	-3, -4, -5
	Industrial					-4	-4

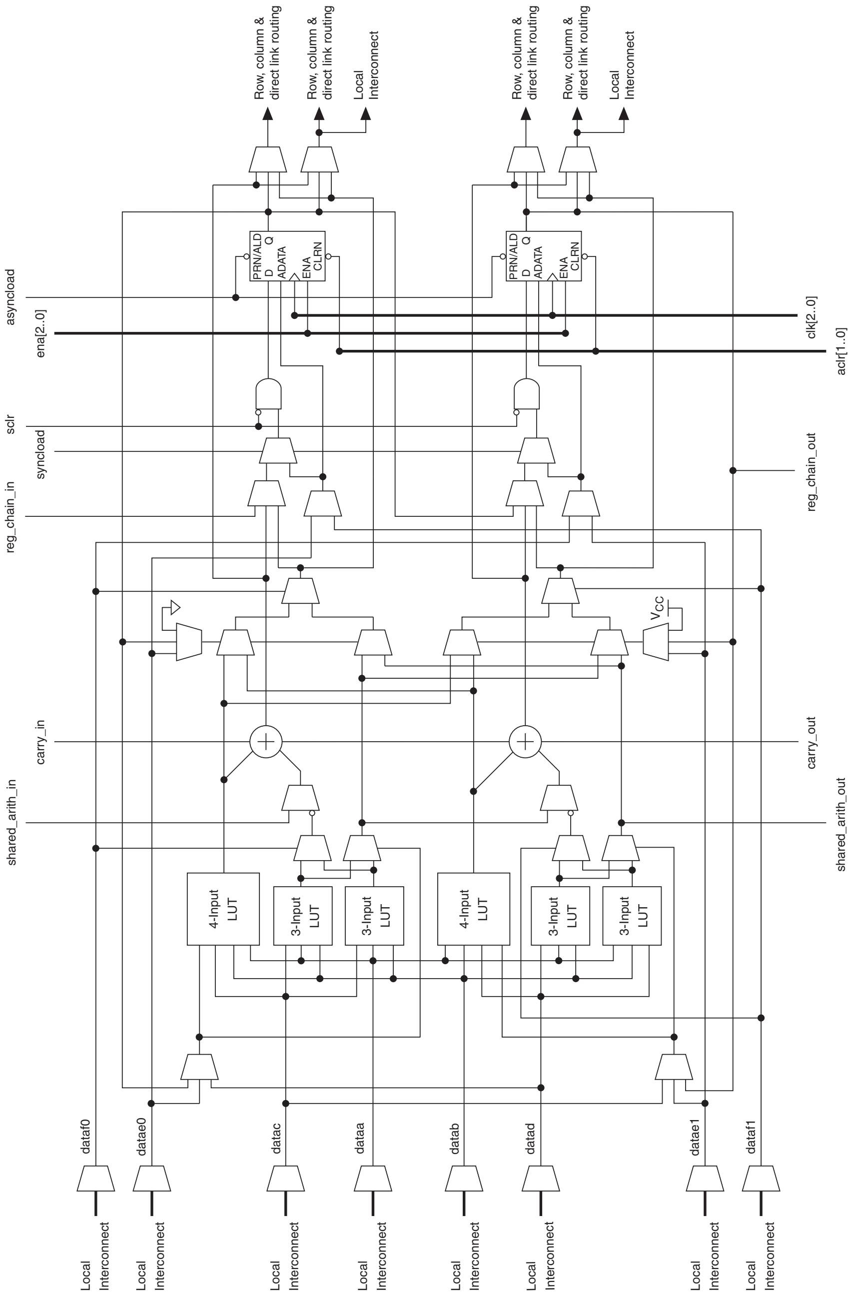
Document Revision History

Table 1–6 shows the revision history for this chapter.

Table 1–6. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007, v4.2	Moved Document Revision History to the end of the chapter.	—
April 2006, v4.1	● Updated "Features" section. ● Removed Note 4 from Table 1–2. ● Updated Table 1–4.	—
December 2005, v4.0	● Updated Tables 1–2, 1–4, and 1–5. ● Updated Figure 2–43.	—
July 2005, v3.1	● Added vertical migration information, including Table 1–4. ● Updated Table 1–5.	—
May 2005, v3.0	● Updated "Features" section. ● Updated Table 1–2.	—
March 2005, v2.1	Updated "Introduction" and "Features" sections.	—
January 2005, v2.0	Added note to Table 1–2.	—
October 2004, v1.2	Updated Tables 1–2, 1–3, and 1–5.	—
July 2004, v1.1	● Updated Tables 1–1 and 1–2. ● Updated "Features" section.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

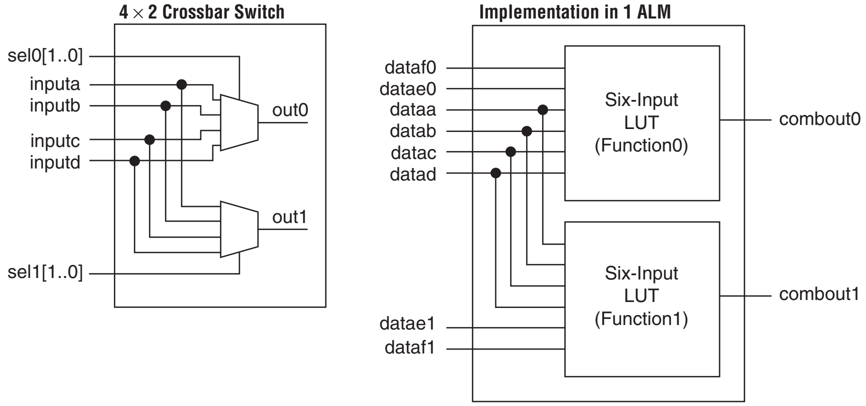
Figure 2–6. Stratix II ALM Details



For the packing of two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are `dataa` and `datab`. The combination of a four-input function with a five-input function requires one common input (either `dataa` or `datab`).

In the case of implementing two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–8. The shared inputs are `dataa`, `datab`, `datac`, and `datad`, while the unique select lines are `datae0` and `dataf0` for `function0`, and `datae1` and `dataf1` for `function1`. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

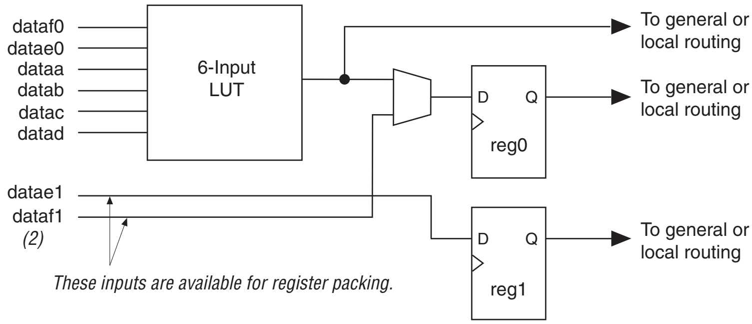
Figure 2–8. 4 × 2 Crossbar Switch Example



In a sparsely used device, functions that could be placed into one ALM may be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically utilizes the full potential of the Stratix II ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments.

Any six-input function can be implemented utilizing inputs `dataa`, `datab`, `datac`, `datad`, and either `datae0` and `dataf0` or `datae1` and `dataf1`. If `datae0` and `dataf0` are utilized, the output is driven to `register0`, and/or `register0` is bypassed and the data drives out to the interconnect using the top set of output drivers (see Figure 2–9). If datae1 and dataf1 are utilized, the output drives to register1 and/or bypasses register1 and drives to the interconnect using the bottom set of output drivers. The Quartus II Compiler automatically selects the inputs to the LUT. Asynchronous load data for the register comes from the datae or dataf input of the ALM. ALMs in normal mode support register packing.

Figure 2–9. 6-Input Function in Normal Mode *Notes (1), (2)*



Notes to Figure 2–9:

(1) If datae1 and dataf1 are used as inputs to the six-input function, then datae0 and dataf0 are available for register packing.

(2) The dataf1 input is available for register packing only if the six-input function is un-registered.

Extended LUT Mode

The extended LUT mode is used to implement a specific set of seven-input functions. The set must be a 2-to-1 multiplexer fed by two arbitrary five-input functions sharing four inputs. Figure 2–10 shows the template of supported seven-input functions utilizing extended LUT mode. In this mode, if the seven-input function is unregistered, the unused eighth input is available for register packing.

Functions that fit into the template shown in Figure 2–10 occur naturally in designs. These functions often appear in designs as “if-else” statements in Verilog HDL or VHDL code.

The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column.

To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only utilize either the top half or the bottom half of the LAB before connecting to the next LAB. This leaves the other half of the ALMs in the LAB available for implementing narrower fan-in functions in normal mode. Carry chains that use the top four ALMs in the first LAB carry into the top half of the ALMs in the next LAB within the column. Carry chains that use the bottom four ALMs in the first LAB carry into the bottom half of the ALMs in the next LAB within the column. Every other column of LABs is top-half bypassable, while the other LAB columns are bottom-half bypassable.

See the "MultiTrack Interconnect" on page 2–22 section for more information on carry chain interconnect.

Shared Arithmetic Mode

In shared arithmetic mode, the ALM can implement a three-input add. In this mode, the ALM is configured with four 4-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder (either to `adder1` in the same ALM or to `adder0` of the next ALM in the LAB) via a dedicated connection called the shared arithmetic chain. This shared arithmetic chain can significantly improve the performance of an adder tree by reducing the number of summation stages required to implement an adder tree. Figure 2–13 shows the ALM in shared arithmetic mode.

Figure 2–26. M-RAM Row Unit Interface to Interconnect

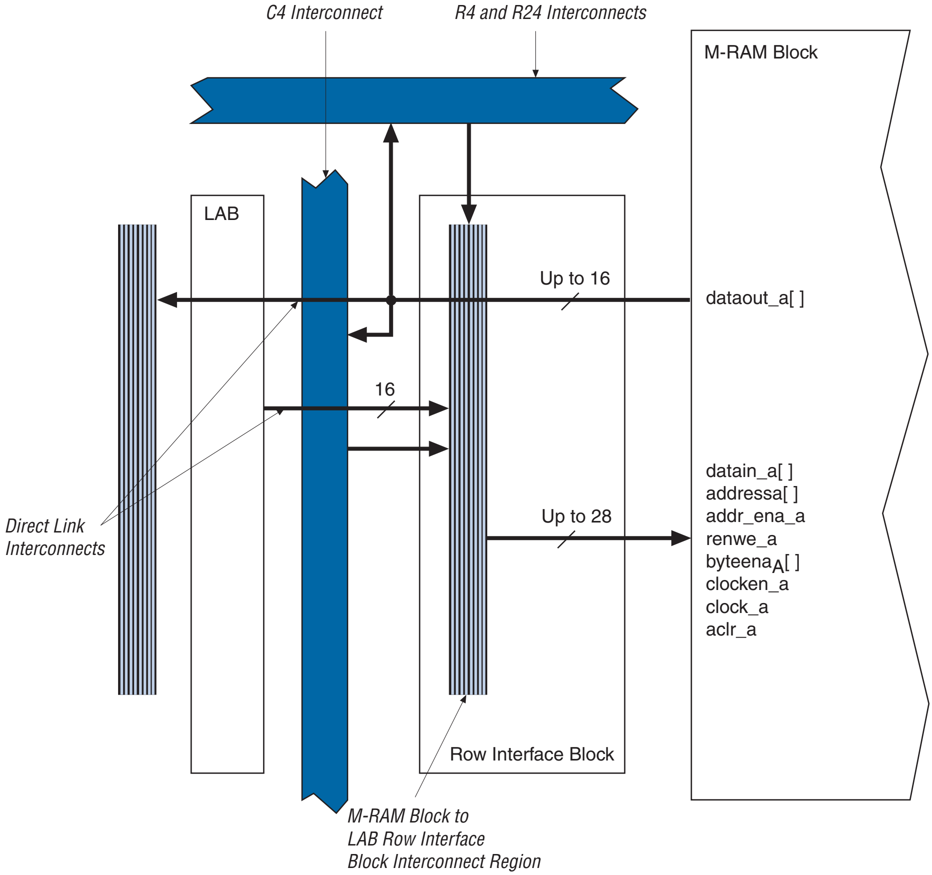


Table 2–4 shows the input and output data signal connections along with the address and control signal input connections to the row unit interfaces (L0 to L5 and R0 to R5).

Figure 2–27 shows one of the columns with surrounding LAB rows.

Figure 2–27. DSP Blocks Arranged in Columns

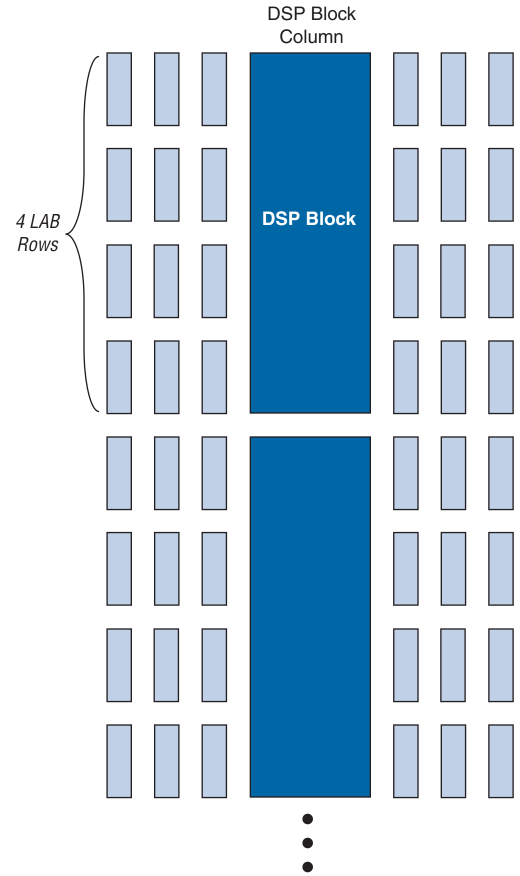
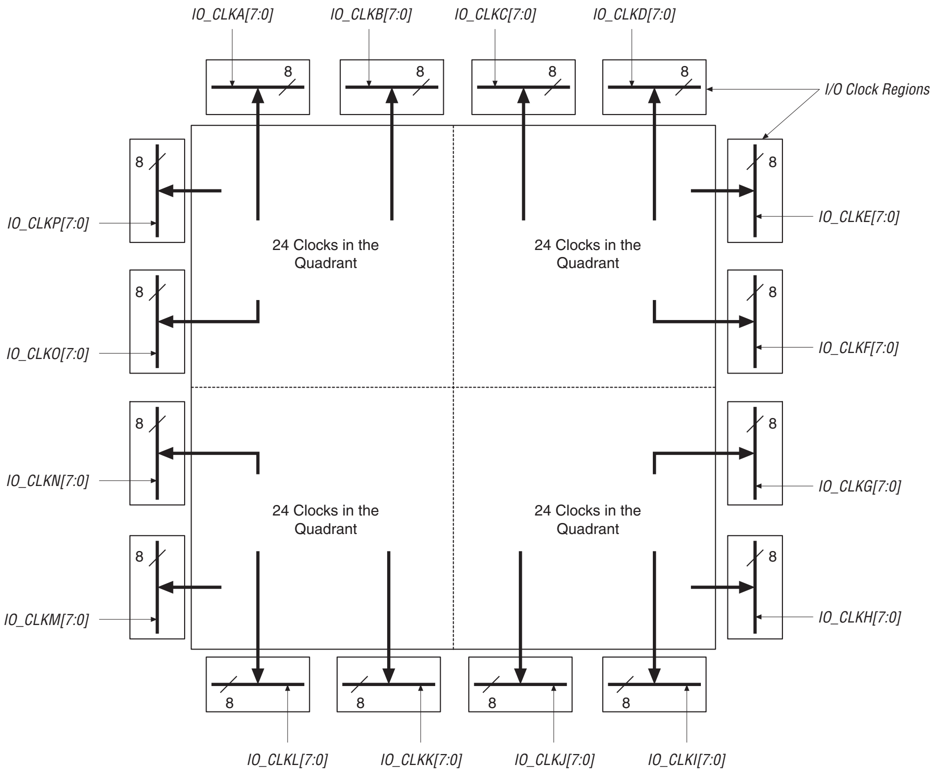


Figure 2–36. EP2S60, EP2S90, EP2S130 & EP2S180 Device I/O Clock Groups



You can use the Quartus II software to control whether a clock input pin drives either a global, regional, or dual-regional clock network. The Quartus II software automatically selects the clocking resources if not specified.

Clock Control Block

Each global clock, regional clock, and PLL external clock output has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable/disable)

Table 2–10 shows the enhanced PLL and fast PLL features in Stratix II devices.

Table 2–10. Stratix II PLL Features

Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	*m*/(*n* × post-scale counter) *(1)*	*m*/(*n* × post-scale counter) *(2)*
Phase shift	Down to 125-ps increments *(3)*, *(4)*	Down to 125-ps increments *(3)*, *(4)*
Clock switchover	✓	✓ *(5)*
PLL reconfiguration	✓	✓
Reconfigurable bandwidth	✓	✓
Spread spectrum clocking	✓	
Programmable duty cycle	✓	✓
Number of internal clock outputs	6	4
Number of external clock outputs	Three differential/six single-ended	*(6)*
Number of feedback clock inputs	One single-ended or differential *(7)*, *(8)*	

Notes to Table 2–10:
(1) For enhanced PLLs, *m* ranges from 1 to 256, while *n* and post-scale counters range from 1 to 512 with 50% duty cycle.
(2) For fast PLLs, *m*, and post-scale counters range from 1 to 32. The *n* counter ranges from 1 to 4.
(3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by 8.
(4) For degree increments, Stratix II devices can shift all output frequencies in increments of at least 45. Smaller degree increments are possible depending on the frequency and divide parameters.
(5) Stratix II fast PLLs only support manual clock switchover.
(6) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate txclkout.
(7) If the feedback input is used, you lose one (or two, if FBIN is differential) external clock output pin.
(8) Every Stratix II device has at least two enhanced PLLs with one single-ended or differential external feedback input per PLL.

Figure 2–43 shows the global and regional clocking from enhanced PLL outputs and top and bottom CLK pins. The connections to the global and regional clocks from the top clock pins and enhanced PLL outputs is shown in Table 2–11. The connections to the clocks from the bottom clock pins is shown in Table 2–12.

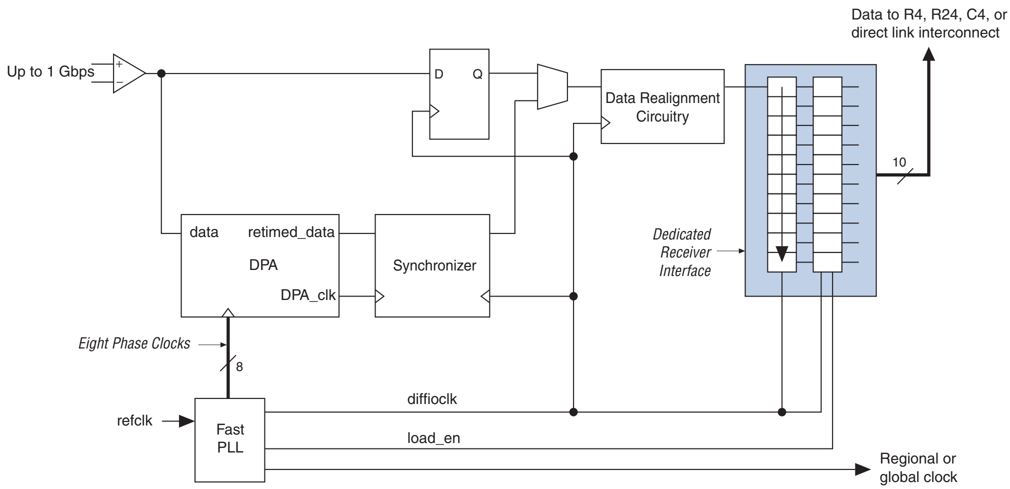
- 1.5-V HSTL Class I and II
- 1.8-V HSTL Class I and II
- 1.2-V HSTL
- SSTL-2 Class I and II
- SSTL-18 Class I and II

Table 2–16 describes the I/O standards supported by Stratix II devices.

Table 2–16. Stratix II Supported I/O Standards (Part 1 of 2)

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	-	3.3	-
LVCMOS	Single-ended	-	3.3	-
2.5 V	Single-ended	-	2.5	-
1.8 V	Single-ended	-	1.8	-
1.5-V LVCMOS	Single-ended	-	1.5	-
3.3-V PCI	Single-ended	-	3.3	-
3.3-V PCI-X mode 1	Single-ended	-	3.3	-
LVDS	Differential	-	2.5 *(3)*	-
LVPECL *(1)*	Differential	-	3.3	-
HyperTransport technology	Differential	-	2.5	-
Differential 1.5-V HSTL Class I and II *(2)*	Differential	0.75	1.5	0.75
Differential 1.8-V HSTL Class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-18 Class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-2 Class I and II *(2)*	Differential	1.25	2.5	1.25
1.2-V HSTL*(4)*	Voltage-referenced	0.6	1.2	0.6
1.5-V HSTL Class I and II	Voltage-referenced	0.75	1.5	0.75
1.8-V HSTL Class I and II	Voltage-referenced	0.9	1.8	0.9
SSTL-18 Class I and II	Voltage-referenced	0.90	1.8	0.90

Figure 2–59. Stratix II Receiver Channel



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the VCO can feed to the DPA circuitry.

For more information on the fast PLL, see the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of the channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Since every channel utilizing the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

Table 3–1. Stratix II JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring a Stratix II device via the JTAG port with a USB Blaster, MasterBlaster™, ByteBlasterMV™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Notes to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information on using the CONFIG_IO instruction, see the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper.*

Table 3–7. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
April 2006, v4.1	Updated “Device Security Using Configuration Bitstream Encryption” section.	—
December 2005, v4.0	Updated “Software Interface” section.	—
May 2005, v3.0	• Updated “IEEE Std. 1149.1 JTAG Boundary-Scan Support” section. • Updated “Operating Modes” section.	—
January 2005, v2.1	Updated JTAG chain device limits.	—
January 2005, v2.0	Updated Table 3–3.	—
July 2004, v1.1	• Added “Automated Single Event Upset (SEU) Detection” section. • Updated “Device Security Using Configuration Bitstream Encryption” section. • Updated Figure 3–2.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

Document Revision History

Table 4–1 shows the revision history for this chapter.

Table 4–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007, v3.2	Moved the Document Revision History section to the end of the chapter.	—
April 2006, v3.1	● Updated “Signal Pins Do Not Drive the VCCIO, VCCINT or VCCPD Power Supplies” section.	● Updated hot socketing AC specification.
May 2005, v3.0	● Updated “Signal Pins Do Not Drive the VCCIO, VCCINT or VCCPD Power Supplies” section. ● Removed information on ESD protection.	—
January 2005, v2.1	Updated input rise and fall time.	—
January 2005, v2.0	Updated the “Hot Socketing Feature Implementation in Stratix II Devices”, “ESD Protection”, and “Power-On Reset Circuitry” sections.	—
July 2004, v1.1	● Updated all tables. ● Added tables.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

Table 5–4. Stratix II Device DC Operating Conditions (Part 2 of 2) *Note (1)*							
Symbol	**Parameter**	**Conditions**		**Minimum**	**Typical**	**Maximum**	**Unit**
I_{CCI00}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25° C	EP2S15		4.0	*(3)*	mA
			EP2S30		4.0	*(3)*	mA
			EP2S60		4.0	*(3)*	mA
			EP2S90		4.0	*(3)*	mA
			EP2S130		4.0	*(3)*	mA
			EP2S180		4.0	*(3)*	mA
R_{CONF} *(4)*	Value of I/O pin pull-up resistor before and during configuration	Vi = 0; V_{CCIO} = 3.3 V		10	25	50	kΩ
		Vi = 0; V_{CCIO} = 2.5 V		15	35	70	kΩ
		Vi = 0; V_{CCIO} = 1.8 V		30	50	100	kΩ
		Vi = 0; V_{CCIO} = 1.5 V		40	75	150	kΩ
		Vi = 0; V_{CCIO} = 1.2 V		50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration				1	2	kΩ

Notes to Table 5–4:

(1) Typical values are for T_A = 25°C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(3) Maximum values depend on the actual T_J and design utilization. See the Excel-based PowerPlay Early Power Estimator (available at **www.altera.com**) or the Quartus II PowerPlay Power Analyzer feature for maximum values. See the section "Power Consumption" on page 5–20 for more information.

(4) Pin pull-up resistance values are lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Tables 5–5 through 5–32 show the Stratix II device family I/O standard specifications.

Table 5–5. LVTTL Specifications (Part 1 of 2)					
Symbol	**Parameter**	**Conditions**	**Minimum**	**Maximum**	**Unit**
V_{CCIO} *(1)*	Output supply voltage		3.135	3.465	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(2)*	2.4		V

Table 5–77. Maximum Input Toggle Rate on Stratix II Devices (Part 2 of 2)									
Input I/O Standard	**Column I/O Pins (MHz)**			**Row I/O Pins (MHz)**			**Dedicated Clock Inputs (MHz)**		
	-3	**-4**	**-5**	**-3**	**-4**	**-5**	**-3**	**-4**	**-5**
1.8-V HSTL Class II	500	500	500	500	500	500	500	500	500
PCI *(1)*	500	500	450	-	-	-	500	500	400
PCI-X *(1)*	500	500	450	-	-	-	500	500	400
1.2-V HSTL *(2)*	280	-	-	-	-	-	280	-	-
Differential SSTL-2 Class I *(1)*, *(3)*	500	500	500	-	-	-	500	500	500
Differential SSTL-2 Class II *(1)*, *(3)*	500	500	500	-	-	-	500	500	500
Differential SSTL-18 Class I *(1)*, *(3)*	500	500	500	-	-	-	500	500	500
Differential SSTL-18 Class II *(1)*, *(3)*	500	500	500	-	-	-	500	500	500
1.8-V Differential HSTL Class I *(1)*, *(3)*	500	500	500	-	-	-	500	500	500
1.8-V Differential HSTL Class II *(1)*, *(3)*	500	500	500	-	-	-	500	500	500
1.5-V Differential HSTL Class I *(1)*, *(3)*	500	500	500	-	-	-	500	500	500
1.5-V Differential HSTL Class II *(1)*, *(3)*	500	500	500	-	-	-	500	500	500
HyperTransport technology *(4)*	-	-	-	520	520	420	717	717	640
LVPECL *(1)*	-	-	-	-	-	-	450	450	400
LVDS *(5)*	-	-	-	520	520	420	717	717	640
LVDS *(6)*	-	-	-	-	-	-	450	450	400

Notes to Table 5–77:

(1) Row clock inputs don't support PCI, PCI-X, LVPECL, and differential HSTL and SSTL standards.
(2) 1.2-V HSTL is only supported on column I/O pins.
(3) Differential HSTL and SSTL standards are only supported on column clock and DQS inputs.
(4) HyperTransport technology is only supported on row I/O and row dedicated clock input pins.
(5) These numbers apply to I/O pins and dedicated clock pins in the left and right I/O banks.
(6) These numbers apply to dedicated clock pins in the top and bottom I/O banks.

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 4 of 5) Note (1)										
I/O Standard	**Drive Strength**	**Column I/O Pins (MHz)**			**Row I/O Pins (MHz)**			**Clock Outputs (MHz)**		
		-3	**-4**	**-5**	**-3**	**-4**	**-5**	**-3**	**-4**	**-5**
1.8-V LVTTL	OCT 50 Ω	700	550	450	700	550	450	700	550	450
3.3-V LVCMOS	OCT 50 Ω	350	350	300	350	350	300	350	350	300
1.5-V LVCMOS	OCT 50 Ω	550	450	400	550	450	400	550	450	400
SSTL-2 Class I	OCT 50 Ω	600	500	500	600	500	500	600	500	500
SSTL-2 Class II	OCT 25 Ω	600	550	500	600	550	500	600	550	500
SSTL-18 Class I	OCT 50 Ω	560	400	350	590	400	350	450	400	350
SSTL-18 Class II	OCT 25 Ω	550	500	450	-	-	-	550	500	450
1.2-V HSTL *(2)*	OCT 50 Ω	280	-	-	-	-	-	280	-	-
1.5-V HSTL Class I	OCT 50 Ω	600	550	500	600	550	500	600	550	500
1.8-V HSTL Class I	OCT 50 Ω	650	600	600	650	600	600	650	600	600
1.8-V HSTL Class II	OCT 25 Ω	500	500	450	-	-	-	500	500	450
Differential SSTL-2 Class I	OCT 50 Ω	600	500	500	600	500	500	600	500	500
Differential SSTL-2 Class II	OCT 25 Ω	600	550	500	600	550	500	600	550	500
Differential SSTL-18 Class I	OCT 50 Ω	560	400	350	590	400	350	560	400	350
Differential SSTL-18 Class II	OCT 25 Ω	550	500	450	-	-	-	550	500	450
1.8-V Differential HSTL Class I	OCT 50 Ω	650	600	600	650	600	600	650	600	600
1.8-V Differential HSTL Class II	OCT 25 Ω	500	500	450	-	-	-	500	500	450
1.5-V Differential HSTL Class I	OCT 50 Ω	600	550	500	600	550	500	600	550	500

Table 5–84. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 2 of 2) Notes (1), (2)

DDIO Column Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	1.2-V HSTL	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	1.2 V	
1.8 V	150	265	85	85	85	ps
1.5-V LVCMOS	255	370	140	140	140	ps
SSTL-2 Class I	175	295	65	65	65	ps
SSTL-2 Class II	170	290	60	60	60	ps
SSTL-18 Class I	155	275	55	50	50	ps
SSTL-18 Class II	140	260	70	70	70	ps
1.8-V HSTL Class I	150	270	60	60	60	ps
1.8-V HSTL Class II	150	270	60	60	60	ps
1.5-V HSTL Class I	150	270	55	55	55	ps
1.5-V HSTL Class II	125	240	85	85	85	ps
1.2-V HSTL	240	360	155	155	155	ps
LVPECL	180	180	180	180	180	ps

Notes to Table 5–84:

(1) Table 5–84 assumes the input clock has zero DCD.

(2) The DCD specification is based on a no logic array noise condition.

Table 5–85. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -4 & -5 Devices (Part 1 of 2) Notes (1), (2)

DDIO Column Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)				Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	
3.3-V LVTTL	440	495	170	160	ps
3.3-V LVCMOS	390	450	120	110	ps
2.5 V	375	430	105	95	ps
1.8 V	325	385	90	100	ps
1.5-V LVCMOS	430	490	160	155	ps
SSTL-2 Class I	355	410	85	75	ps
SSTL-2 Class II	350	405	80	70	ps