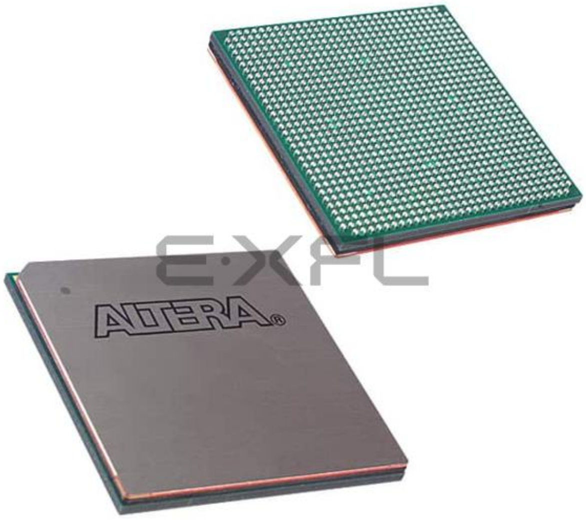


Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	6627
Number of Logic Elements/Cells	132540
Total RAM Bits	6747840
Number of I/O	742
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s130f1020c5n

Chapter 6. Reference & Ordering Information

1. Introduction

SII51001-4.2

Introduction

The Stratix® II FPGA family is based on a 1.2-V, 90-nm, all-layer copper SRAM process and features a new logic structure that maximizes performance, and enables device densities approaching 180,000 equivalent logic elements (LEs). Stratix II devices offer up to 9 Mbits of on-chip, TriMatrix™ memory for demanding, memory intensive applications and has up to 96 DSP blocks with up to 384 (18-bit × 18-bit) multipliers for efficient implementation of high performance filters and other DSP functions. Various high-speed external memory interfaces are supported, including double data rate (DDR) SDRAM and DDR2 SDRAM, RLDRAM II, quad data rate (QDR) II SRAM, and single data rate (SDR) SDRAM. Stratix II devices support various I/O standards along with support for 1-gigabit per second (Gbps) source synchronous signaling with DPA circuitry. Stratix II devices offer a complete clock management solution with internal clock frequency of up to 550 MHz and up to 12 phase-locked loops (PLLs). Stratix II devices are also the industry's first FPGAs with the ability to decrypt a configuration bitstream using the Advanced Encryption Standard (AES) algorithm to protect designs.

Features

The Stratix II family offers the following features:

- 15,600 to 179,400 equivalent LEs; see Table 1–1
- New and innovative adaptive logic module (ALM), the basic building block of the Stratix II architecture, maximizes performance and resource usage efficiency
- Up to 9,383,040 RAM bits (1,172,880 bytes) available without reducing logic resources
- TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers
- High-speed DSP blocks provide dedicated implementation of multipliers (at up to 450 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
- Up to 16 global clocks with 24 clocking resources per device region
- Clock control blocks support dynamic clock network enable/disable, which allows clock networks to power down to reduce power consumption in user mode
- Up to 12 PLLs (four enhanced PLLs and eight fast PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting

After compilation, check the information messages for a full list of I/O, DQ, LVDS, and other pins that are not available because of the selected migration path.

Table 1–4 lists the Stratix II device package offerings and shows the total number of non-migratable user I/O pins when migrating from one density device to a larger density device. Additional I/O pins may not be migratable if migrating from the larger device to the smaller density device.

When moving from one density to a larger density, the larger density device may have fewer user I/O pins. The larger device requires more power and ground pins to support the additional logic within the device. Use the Quartus II Pin Planner to determine which user I/O pins are migratable between the two devices.

Table 1–4. Total Number of Non-Migratable I/O Pins for Stratix II Vertical Migration Paths

Vertical Migration Path	484-Pin FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1020-Pin FineLine BGA	1508-Pin FineLine BGA
EP2S15 to EP2S30	0 *(1)*	0			
EP2S15 to EP2S60	8 *(1)*	0			
EP2S30 to EP2S60	8 *(1)*	8			
EP2S60 to EP2S90				0	
EP2S60 to EP2S130				0	
EP2S60 to EP2S180				0	
EP2S90 to EP2S130			0 *(1)*	16	17
EP2S90 to EP2S180				16	0
EP2S130 to EP2S180				0	0

Note to Table 1–4:

(1) Some of the DQ/DQS pins are not migratable. Refer to the Quartus II software information messages for more detailed information.

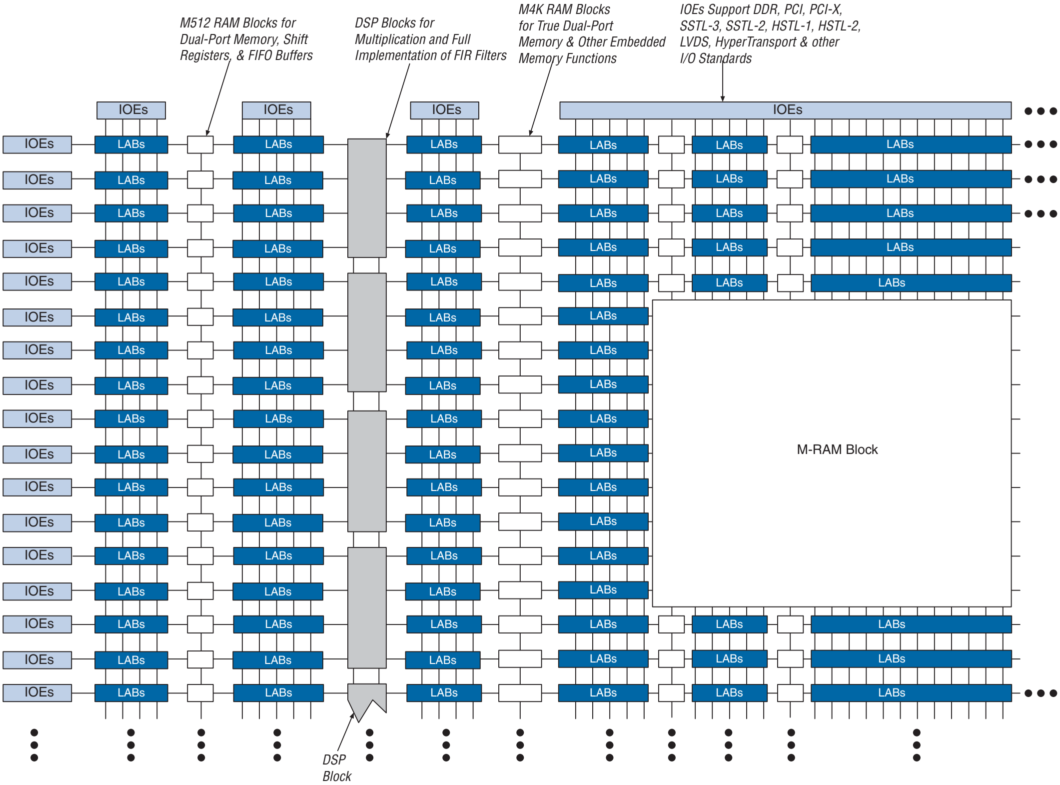
To determine if your user I/O assignments are correct, run the I/O Assignment Analysis command in the Quartus II software (Processing > Start > Start I/O Assignment Analysis).

Refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook* for more information on pin migration.

Each Stratix II device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with dedicated clocks, these registers provide exceptional performance and interface support with external memory devices such as DDR and DDR2 SDRAM, RLDRAM II, and QDR II SRAM devices. High-speed serial interface channels with dynamic phase alignment (DPA) support data transfer at up to 1 Gbps using LVDS or HyperTransport™ technology I/O standards.

Figure 2–1 shows an overview of the Stratix II device.

Figure 2–1. Stratix II Block Diagram



The number of M512 RAM, M4K RAM, and DSP blocks varies by device along with row and column numbers and M-RAM blocks. Table 2–1 lists the resources available in Stratix II devices.

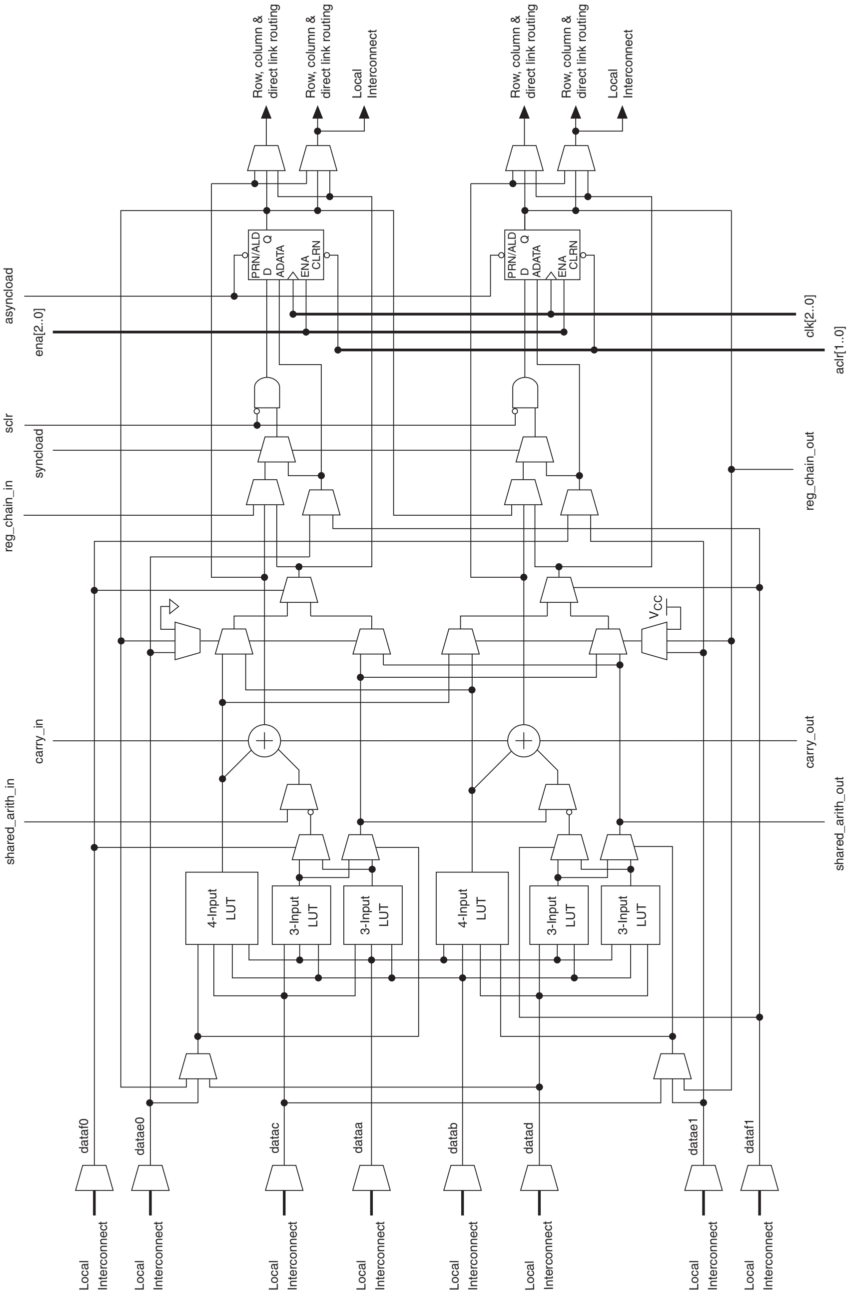
Table 2–1. Stratix II Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks	LAB Columns	LAB Rows
EP2S15	4 / 104	3 / 78	0	2 / 12	30	26
EP2S30	6 / 202	4 / 144	1	2 / 16	49	36
EP2S60	7 / 329	5 / 255	2	3 / 36	62	51
EP2S90	8 / 488	6 / 408	4	3 / 48	71	68
EP2S130	9 / 699	7 / 609	6	3 / 63	81	87
EP2S180	11 / 930	8 / 768	9	4 / 96	100	96

Logic Array Blocks

Each LAB consists of eight ALMs, carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines. The local interconnect transfers signals between ALMs in the same LAB. Register chain connections transfer the output of an ALM register to the adjacent ALM register in an LAB. The Quartus® II Compiler places associated logic in an LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency. Figure 2–2 shows the Stratix II LAB structure.

Figure 2–6. Stratix II ALM Details



One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, asynchronous load data, and synchronous and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous load data. The asynchronous load data input comes from the `datae` or `dataf` input of the ALM, which are the same inputs that can be used for register packing. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of the ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers independently (see Figure 2–6). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.

See the *Performance & Logic Efficiency Analysis of Stratix II Devices White Paper* for more information on the efficiencies of the Stratix II ALM and comparisons with previous architectures.

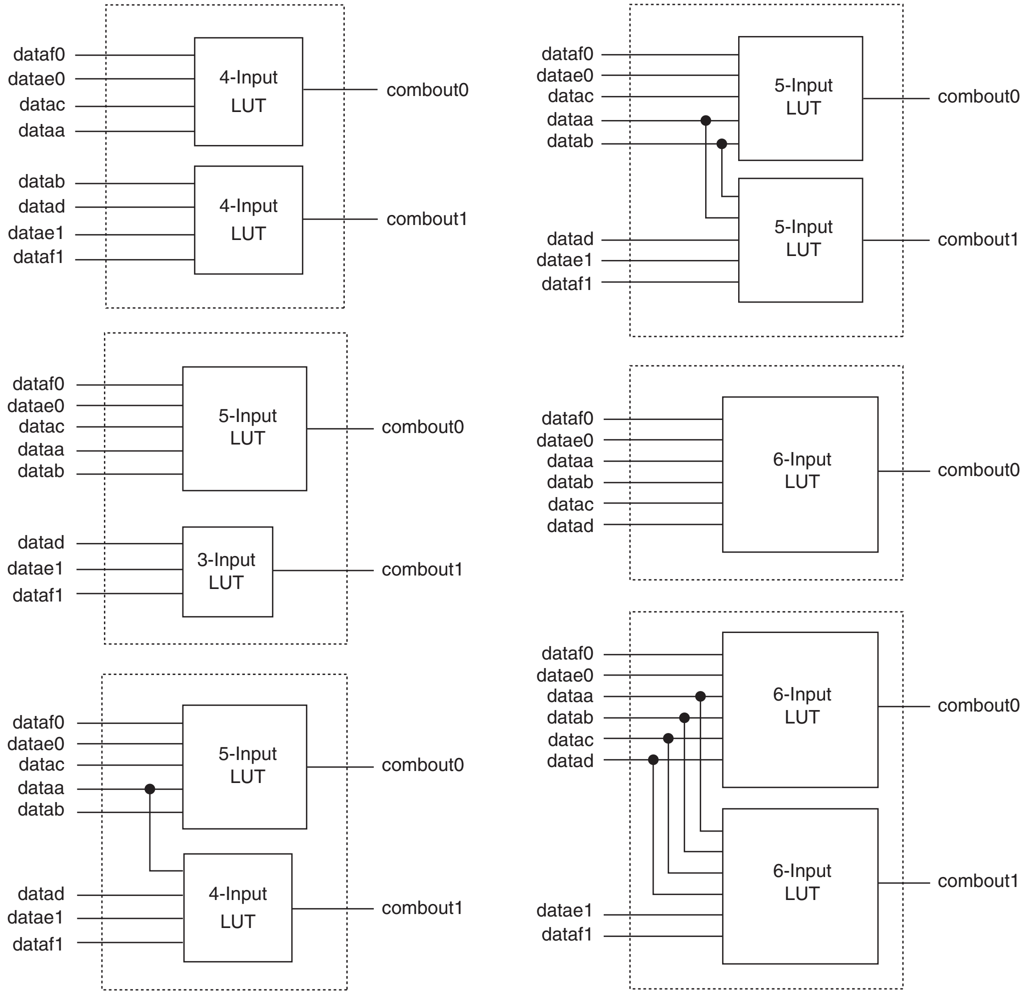
ALM Operating Modes

The Stratix II ALM can operate in one of the following modes:

- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

Each mode uses ALM resources differently. In each mode, eleven available inputs to the ALM--the eight data inputs from the LAB local interconnect; `carry-in` from the previous ALM or LAB; the shared arithmetic chain connection from the previous ALM or LAB; and the register chain connection--are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear,

Figure 2–7. ALM in Normal Mode *Note (1)*

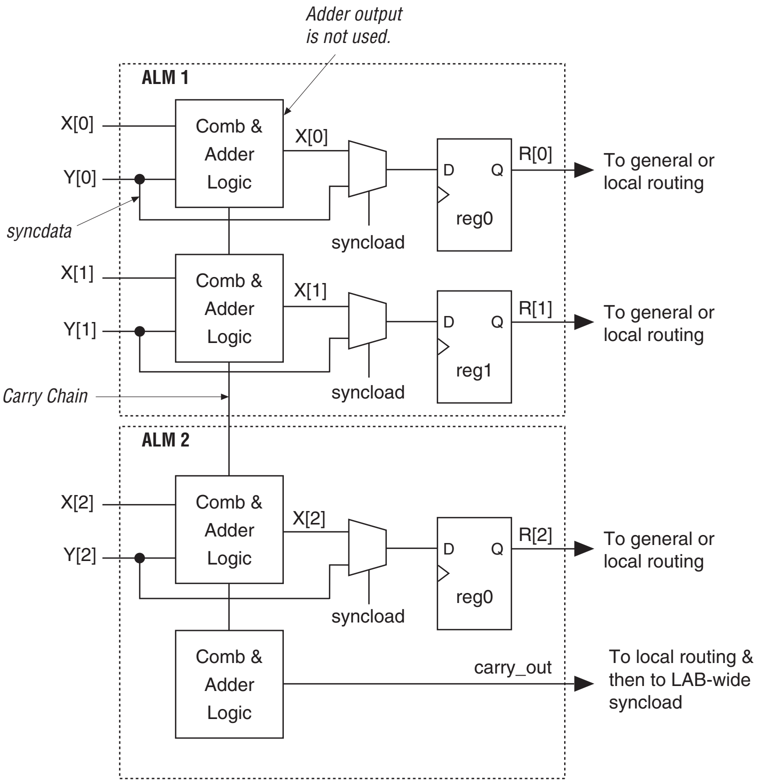


Note to Figure 2–7:

(1) Combinations of functions with fewer inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, etc.

The normal mode provides complete backward compatibility with four-input LUT architectures. Two independent functions of four inputs or less can be implemented in one Stratix II ALM. In addition, a five-input function and an independent three-input function can be implemented without sharing inputs.

Figure 2–12. Conditional Operation Example



The arithmetic mode also offers clock enable, counter enable, synchronous up/down control, add/subtract control, synchronous clear, synchronous load. The LAB local interconnect data inputs generate the clock enable, counter enable, synchronous up/down and add/subtract control signals. These control signals are good candidates for the inputs that are shared between the four LUTs in the ALM. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Carry Chain

The carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. Carry chains can begin in either the first ALM or the fifth ALM in an LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column.

To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only utilize either the top half or the bottom half of the LAB before connecting to the next LAB. This leaves the other half of the ALMs in the LAB available for implementing narrower fan-in functions in normal mode. Carry chains that use the top four ALMs in the first LAB carry into the top half of the ALMs in the next LAB within the column. Carry chains that use the bottom four ALMs in the first LAB carry into the bottom half of the ALMs in the next LAB within the column. Every other column of LABs is top-half bypassable, while the other LAB columns are bottom-half bypassable.

See the "MultiTrack Interconnect" on page 2–22 section for more information on carry chain interconnect.

Shared Arithmetic Mode

In shared arithmetic mode, the ALM can implement a three-input add. In this mode, the ALM is configured with four 4-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder (either to `adder1` in the same ALM or to `adder0` of the next ALM in the LAB) via a dedicated connection called the shared arithmetic chain. This shared arithmetic chain can significantly improve the performance of an adder tree by reducing the number of summation stages required to implement an adder tree. Figure 2–13 shows the ALM in shared arithmetic mode.

R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and Row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect. These column resources include:

- Shared arithmetic chain interconnects in an LAB
- Carry chain interconnects in an LAB and from LAB to LAB
- Register chain interconnects in an LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix II devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM to ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–17 shows the shared arithmetic chain, carry chain and register chain interconnects.

Table 2–3. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support		✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Output registers	Output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

Notes to Table 2–3:

(1) The M-RAM block does not support memory initializations. However, the M-RAM block can emulate a ROM function using a dual-port RAM bock. The Stratix II device must write to the dual-port memory once and then disable the write-enable ports afterwards.

Memory Block Size

TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

When applied to input registers, the asynchronous clear signal for the TriMatrix embedded memory immediately clears the input registers. However, the output of the memory block does not show the effects until the next clock edge. When applied to output registers, the asynchronous clear signal clears the output registers and the effects are seen immediately.

Figure 2–19. M512 RAM Block Control Signals

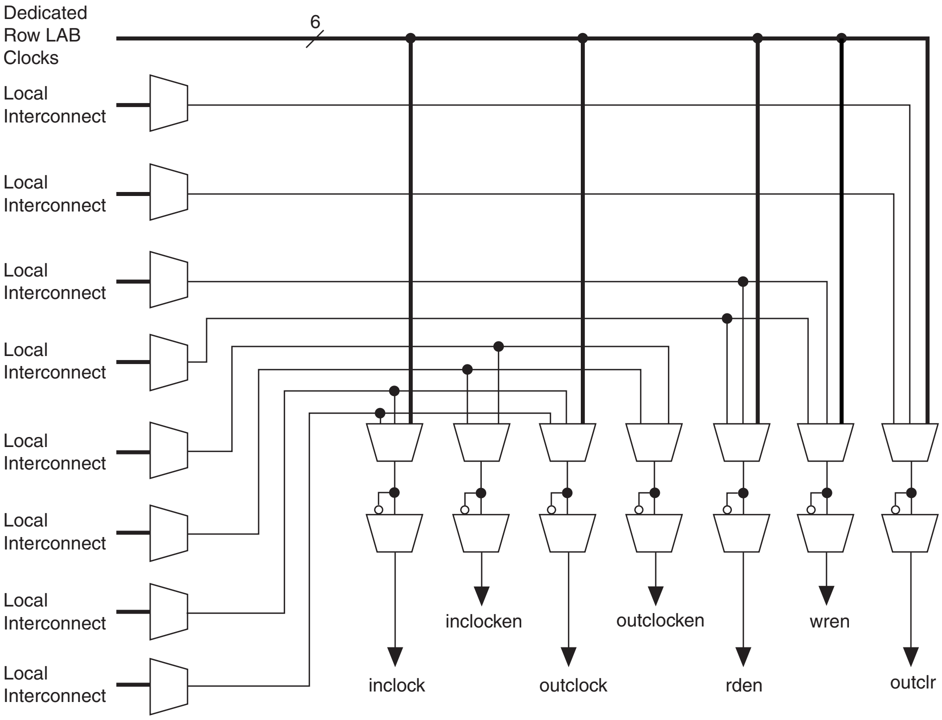
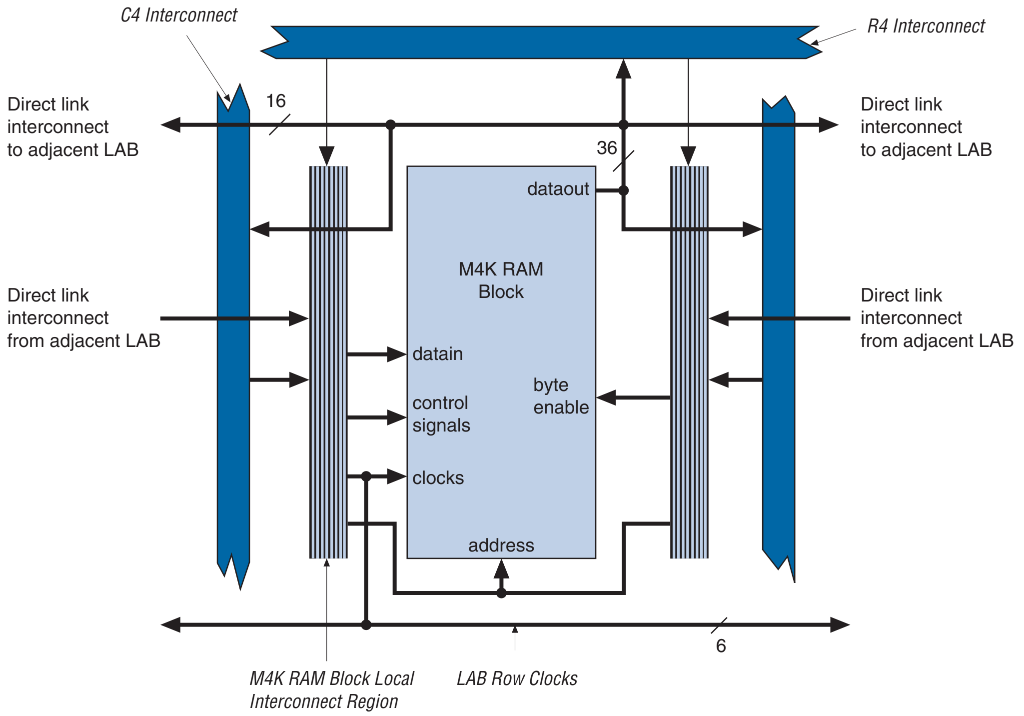


Figure 2–22. M4K RAM Block LAB Row Interface



M-RAM Block

The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO

You cannot use an initialization file to initialize the contents of an M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed.

Differential On-Chip Termination

Stratix II devices support internal differential termination with a nominal resistance value of 100 Ω for LVDS or HyperTransport technology input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. Differential on-chip termination is supported across the full range of supported differential data rates as shown in the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*.

For more information on differential on-chip termination, refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

For more information on tolerance specifications for differential on-chip termination, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook.*

On-Chip Series Termination Without Calibration

Stratix II devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Stratix II devices support on-chip series termination for single-ended I/O standards with typical R_S values of 25 and 50 Ω. Once matching impedance is selected, current drive strength is no longer selectable. Table 2–17 shows the list of output standards that support on-chip series termination without calibration.

On-Chip Series Termination with Calibration

Stratix II devices support on-chip series termination with calibration in column I/O pins in top and bottom banks. There is one calibration circuit for the top I/O banks and one circuit for the bottom I/O banks. Each on-chip series termination calibration circuit compares the total impedance of each I/O buffer to the external 25- or 50-Ω resistors connected to the `RUP` and `RDN` pins, and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.

For more information on series on-chip termination supported by Stratix II devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

Table 5–74. Stratix II I/O Input Delay for Row Pins (Part 2 of 2)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (1)	-3 Speed Grade (2)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
1.5-V HSTL Class II	t_{PI}	602	631	1056	1107	1212	1413	ps
	t_{PCOUT}	278	292	529	555	608	708	ps
1.8-V HSTL Class I	t_{PI}	577	605	960	1006	1101	1285	ps
	t_{PCOUT}	253	266	433	454	497	580	ps
1.8-V HSTL Class II	t_{PI}	577	605	960	1006	1101	1285	ps
	t_{PCOUT}	253	266	433	454	497	580	ps
LVDS	t_{PI}	515	540	948	994	1088	1269	ps
	t_{PCOUT}	191	201	421	442	484	564	ps
HyperTransport	t_{PI}	515	540	948	994	1088	1269	ps
	t_{PCOUT}	191	201	421	442	484	564	ps

Notes for Table 5–74:

(1) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.

(2) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 1 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
LVTTL	4 mA	t_{OP}	1178	1236	2351	2467	2702	2820	ps
		t_{DIP}	1198	1258	2417	2537	2778	2910	ps
	8 mA	t_{OP}	1041	1091	2036	2136	2340	2448	ps
		t_{DIP}	1061	1113	2102	2206	2416	2538	ps
	12 mA	t_{OP}	976	1024	2036	2136	2340	2448	ps
		t_{DIP}	996	1046	2102	2206	2416	2538	ps
	16 mA	t_{OP}	951	998	1893	1986	2176	2279	ps
		t_{DIP}	971	1020	1959	2056	2252	2369	ps
	20 mA	t_{OP}	931	976	1787	1875	2054	2154	ps
		t_{DIP}	951	998	1853	1945	2130	2244	ps
	24 mA (1)	t_{OP}	924	969	1788	1876	2055	2156	ps
		t_{DIP}	944	991	1854	1946	2131	2246	ps

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 2 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
1.8-V LVTTL/LVCMOS	2 mA	951	1421	1421	951	1421	1421	904	1421	1421
	4 mA	405	516	516	405	516	516	393	516	516
	6 mA	261	325	325	261	325	325	253	325	325
	8 mA	223	274	274	223	274	274	224	274	274
	10 mA	194	236	236	-	-	-	199	236	236
	12 mA	174	209	209	-	-	-	180	209	209
1.5-V LVTTL/LVCMOS	2 mA	652	963	963	652	963	963	618	963	963
	4 mA	333	347	347	333	347	347	270	347	347
	6 mA	182	247	247	-	-	-	198	247	247
	8 mA	135	194	194	-	-	-	155	194	194
SSTL-2 Class I	8 mA	364	680	680	364	680	680	350	680	680
	12 mA	163	207	207	163	207	207	188	207	207
SSTL-2 Class II	16 mA	118	147	147	118	147	147	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116
SSTL-18 Class I	4 mA	458	570	570	458	570	570	505	570	570
	6 mA	305	380	380	305	380	380	336	380	380
	8 mA	225	282	282	225	282	282	248	282	282
	10 mA	167	220	220	167	220	220	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175
SSTL-18 Class II	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
SSTL-2 Class I	8 mA	364	680	680	364	680	680	350	680	680
	12 mA	163	207	207	163	207	207	188	207	207
SSTL-2 Class II	16 mA	118	147	147	118	147	147	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 4 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
Differential SSTL-18 Class I *(3)*	4 mA	458	570	570	-	-	-	505	570	570
	6 mA	305	380	380	-	-	-	336	380	380
	8 mA	225	282	282	-	-	-	248	282	282
	10 mA	167	220	220	-	-	-	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175
Differential SSTL-18 Class II *(3)*	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
1.8-V Differential HSTL Class I *(3)*	4 mA	245	282	282	-	-	-	229	282	282
	6 mA	164	188	188	-	-	-	153	188	188
	8 mA	123	140	140	-	-	-	114	140	140
	10 mA	110	124	124	-	-	-	108	124	124
	12 mA	97	110	110	-	-	-	104	110	110
1.8-V Differential HSTL Class II *(3)*	16 mA	101	104	104	-	-	-	99	104	104
	18 mA	98	102	102	-	-	-	93	102	102
	20 mA	93	99	99	-	-	-	88	99	99
1.5-V Differential HSTL Class I *(3)*	4 mA	168	196	196	-	-	-	188	196	196
	6 mA	112	131	131	-	-	-	125	131	131
	8 mA	84	99	99	-	-	-	95	99	99
	10 mA	87	98	98	-	-	-	90	98	98
	12 mA	86	98	98	-	-	-	87	98	98
1.5-V Differential HSTL Class II *(3)*	16 mA	95	101	101	-	-	-	96	101	101
	18 mA	95	100	100	-	-	-	101	100	100
	20 mA	94	101	101	-	-	-	104	101	101
3.3-V PCI		134	177	177	-	-	-	143	177	177
3.3-V PCI-X		134	177	177	-	-	-	143	177	177
LVDS		-	-	-	155 *(1)*	155 *(1)*	155 *(1)*	134	134	134
HyperTransport technology		-	-	-	155 *(1)*	155 *(1)*	155 *(1)*	-	-	-
LVPECL *(4)*		-	-	-	-	-	-	134	134	134

Table 5–85. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -4 & -5 Devices (Part 2 of 2) Notes (1), (2)

DDIO Column Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)				Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	
SSTL-18 Class I	335	390	65	65	ps
SSTL-18 Class II	320	375	70	80	ps
1.8-V HSTL Class I	330	385	60	70	ps
1.8-V HSTL Class II	330	385	60	70	ps
1.5-V HSTL Class I	330	390	60	70	ps
1.5-V HSTL Class II	330	360	90	100	ps
1.2-V HSTL	420	470	155	165	ps
LVPECL	180	180	180	180	ps

Notes to Table 5–85:

(1) Table 5–85 assumes the input clock has zero DCD.

(2) The DCD specification is based on a no logic array noise condition.

Table 5–86. Maximum DCD for DDIO Output on Row I/O Pins with PLL in the Clock Path (Part 1 of 2) Note (1)

Row DDIO Output I/O Standard	Maximum DCD (PLL Output Clock Feeding DDIO Clock Port)		Unit
	-3 Device	-4 & -5 Device	
3.3-V LVTTL	110	105	ps
3.3-V LVCMOS	65	75	ps
2.5V	75	90	ps
1.8V	85	100	ps
1.5-V LVCMOS	105	100	ps
SSTL-2 Class I	65	75	ps
SSTL-2 Class II	60	70	ps
SSTL-18 Class I	50	65	ps
1.8-V HSTL Class I	50	70	ps
1.5-V HSTL Class I	55	70	ps

Table 5–103. Document Revision History (Part 2 of 3)

Date and Document Version	Changes Made	Summary of Changes
August, 2006, v4.2	Updated Table 5–73, Table 5–75, Table 5–77, Table 5–78, Table 5–79, Table 5–81, Table 5–85, and Table 5–87.	—
April 2006, v4.1	• Updated Table 5–3. • Updated Table 5–11. • Updated Figures 5–8 and 5–9. • Added parallel on-chip termination information to “On-Chip Termination Specifications” section. • Updated Tables 5–28, 5–30,5–31, and 5–34. • Updated Table 5–78, Tables 5–81 through 5–90, and Tables 5–92, 5–93, and 5–98. • Updated “PLL Timing Specifications” section. • Updated “External Memory Interface Specifications” section. • Added Tables 5–95 and 5–101. • Updated “JTAG Timing Specifications” section, including Figure 5–10 and Table 5–102.	• Changed 0.2 MHz to 2 MHz in Table 5–93. • Added new spec for half period jitter (Table 5–101). • Added support for PLL clock switchover for industrial temperature range. • Changed f_{INPFD} (min) spec from 4 MHz to 2 MHz in Table 5–92. • Fixed typo in $t_{OUTJITTER}$ specification in Table 5–92. • Updated V_{DIF} AC & DC max specifications in Table 5–28. • Updated minimum values for t_{JCH}, t_{JCL}, and t_{JPSU} in Table 5–102. • Update maximum values for t_{JPCO}, t_{JPZX}, and t_{JPXZ} in Table 5–102.
December 2005, v4.0	• Updated “External Memory Interface Specifications” section. • Updated timing numbers throughout chapter.	—
July 2005, v3.1	• Updated HyperTransport technology information in Table 5–13. • Updated “Timing Model” section. • Updated “PLL Timing Specifications” section. • Updated “External Memory Interface Specifications” section.	—
May 2005, v3.0	• Updated tables throughout chapter. • Updated “Power Consumption” section. • Added various tables. • Replaced “Maximum Input & Output Clock Rate” section with “Maximum Input & Output Clock Toggle Rate” section. • Added “Duty Cycle Distortion” section. • Added “External Memory Interface Specifications” section.	—
March 2005, v2.2	Updated tables in “Internal Timing Parameters” section.	—
January 2005, v2.1	Updated input rise and fall time.	—