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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	6627
Number of Logic Elements/Cells	132540
Total RAM Bits	6747840
Number of I/O	1126
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s130f1508c3

Stratix II devices are available in up to three speed grades, -3, -4, and -5, with -3 being the fastest. [Table 1–5](#) shows Stratix II device speed-grade offerings.

Table 1–5. Stratix II Device Speed Grades

Device	Temperature Grade	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S30	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S60	Commercial	-3, -4, -5		-3, -4, -5		-3, -4, -5	
	Industrial	-4		-4		-4	
EP2S90	Commercial		-4, -5		-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S130	Commercial				-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S180	Commercial					-3, -4, -5	-3, -4, -5
	Industrial					-4	-4

One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, asynchronous load data, and synchronous and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous load data. The asynchronous load data input comes from the `dataae` or `dataaf` input of the ALM, which are the same inputs that can be used for register packing. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of the ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers independently (see [Figure 2-6](#)). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.



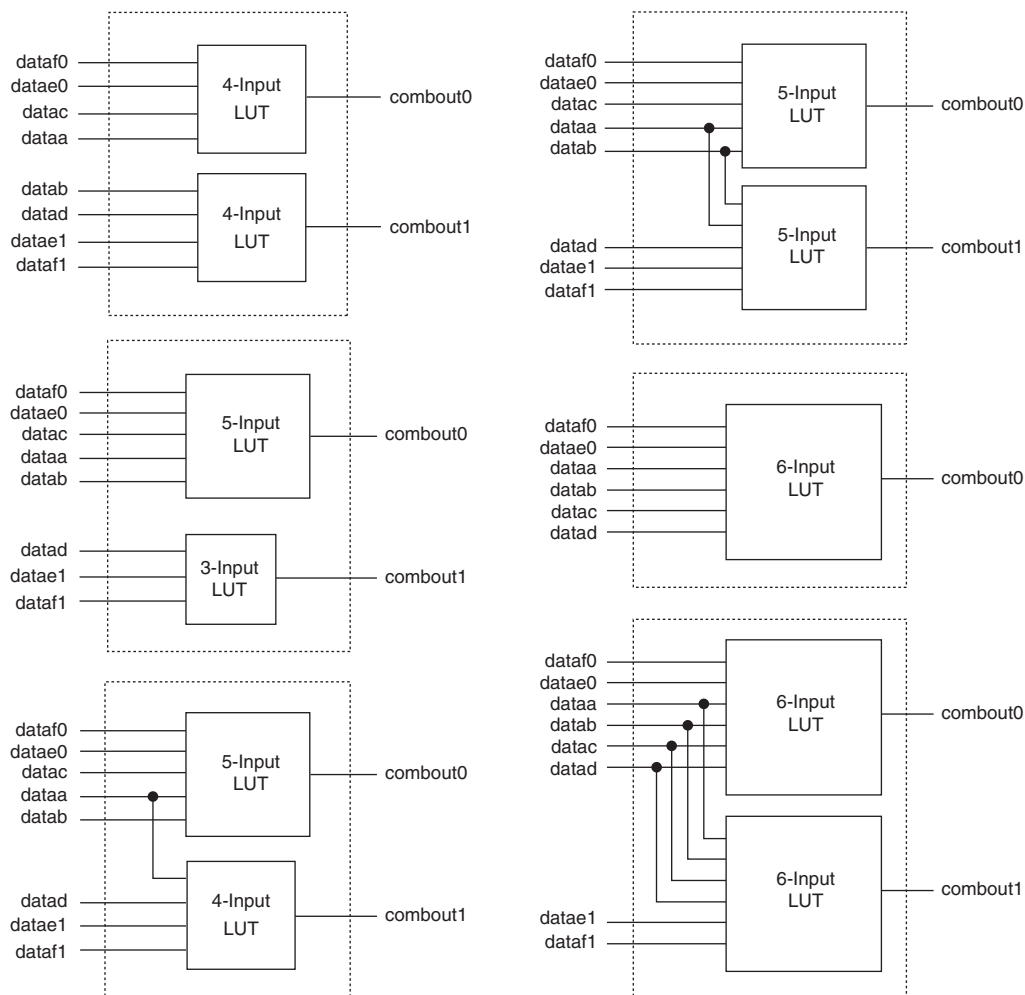
See the *Performance & Logic Efficiency Analysis of Stratix II Devices White Paper* for more information on the efficiencies of the Stratix II ALM and comparisons with previous architectures.

ALM Operating Modes

The Stratix II ALM can operate in one of the following modes:

- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

Each mode uses ALM resources differently. In each mode, eleven available inputs to the ALM—the eight data inputs from the LAB local interconnect; `carry-in` from the previous ALM or LAB; the shared arithmetic chain connection from the previous ALM or LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear,

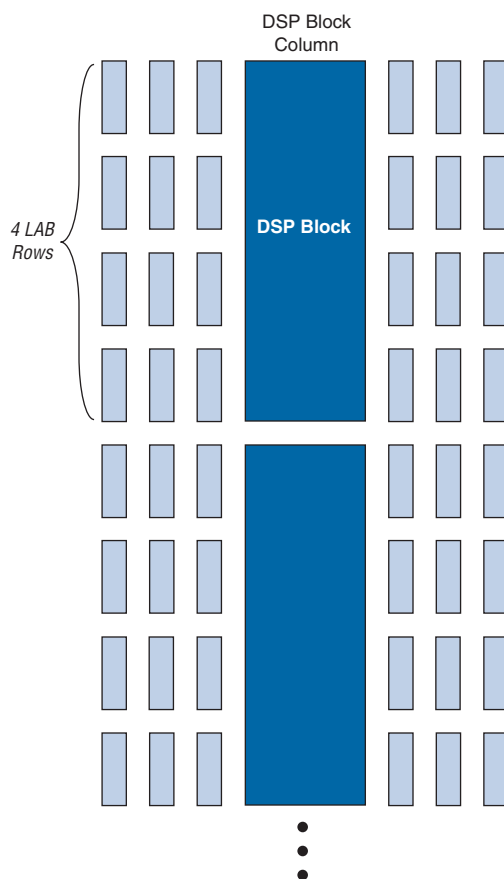
Figure 2–7. ALM in Normal Mode *Note (1)***Note to Figure 2–7:**

- (1) Combinations of functions with fewer inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, etc.

The normal mode provides complete backward compatibility with four-input LUT architectures. Two independent functions of four inputs or less can be implemented in one Stratix II ALM. In addition, a five-input function and an independent three-input function can be implemented without sharing inputs.

Figure 2–27 shows one of the columns with surrounding LAB rows.

Figure 2–27. DSP Blocks Arranged in Columns



Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Table 2–6 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, and 2D FIR filters, equalizers, IIR, correlators, matrix multiplication and many other functions. The DSP blocks also support mixed modes and mixed multiplier sizes in the same block. For example, half of one DSP block can implement one 18×18 -bit multiplier in multiply-accumulator mode, while the other half of the DSP block implements four 9×9 -bit multipliers in simple multiplier mode.

Table 2–6. Multiplier Size & Configurations per DSP Block

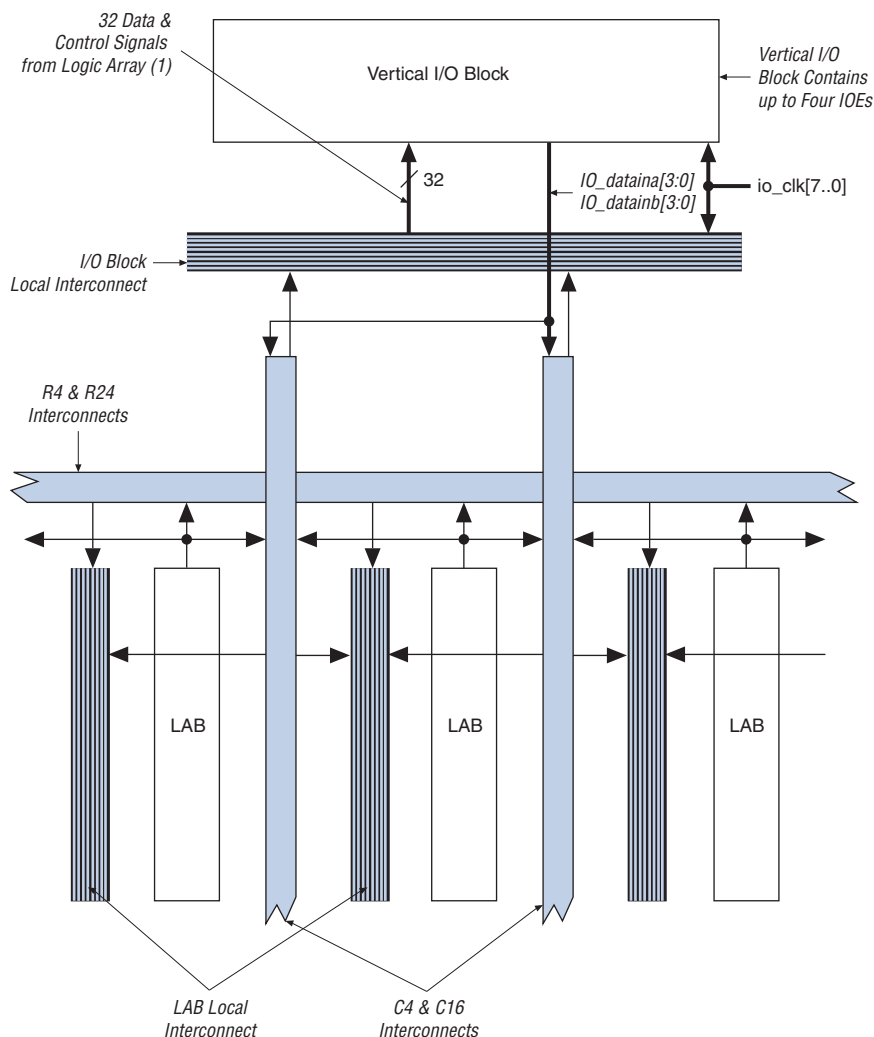
DSP Block Mode	9×9	18×18	36×36
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	-	Two 52-bit multiply-accumulate blocks	-
Two-multipliers adder	Four two-multiplier adder (two 9×9 complex multiply)	Two two-multiplier adder (one 18×18 complex multiply)	-
Four-multipliers adder	Two four-multiplier adder	One four-multiplier adder	-

DSP Block Interface

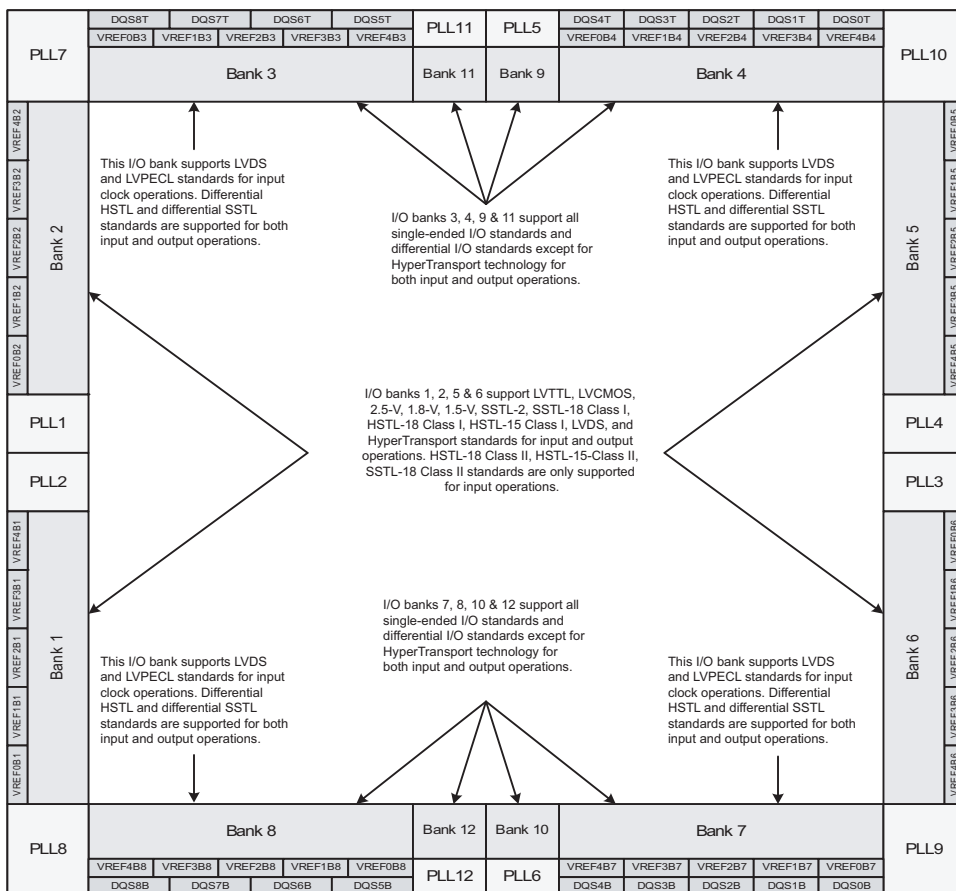
Stratix II device DSP block input registers can generate a shift register that can cascade down in the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade registers within multiple DSP blocks for 9×9 - or 18×18 -bit FIR filters larger than four taps, with additional adder stages implemented in ALMs. If the DSP block is configured as 36×36 bits, the adder, subtractor, or accumulator stages are implemented in ALMs. Each DSP block can route the shift register chain out of the block to cascade multiple columns of DSP blocks.

- Output drive strength control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- Double data rate (DDR) registers

The IOE in Stratix II devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. [Figure 2-46](#) shows the Stratix II IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

Figure 2–48. Column I/O Block Connection to the Interconnect *Note (1)***Note to Figure 2–48:**

- (1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

Figure 2–57. Stratix II I/O Banks Notes (1), (2), (3), (4)**Notes to Figure 2–57:**

- (1) Figure 2–57 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only.
- (2) Depending on the size of the device, different device members have different numbers of V_{REF} groups. Refer to the pin list and the Quartus II software for exact locations.
- (3) Banks 9 through 12 are enhanced PLL external clock output banks. These PLL banks utilize the adjacent V_{REF} group when voltage-referenced standards are implemented. For example, if an SSTL input is implemented in PLL bank 10, the voltage level at VREFB7 is the reference voltage level for the SSTL input.
- (4) Horizontal I/O banks feature SERDES and DPA circuitry for high speed differential I/O standards. See the *High Speed Differential I/O Interfaces in Stratix II & Stratix II GX Devices* chapter of the *Stratix II Device Handbook, Volume 2* or the *Stratix II GX Device Handbook, Volume 2* for more information on differential I/O standards.

Table 2–20. Supported TDO/TDI Voltage Combinations (Part 2 of 2)

Device	TDI Input Buffer Power	Stratix II TDO V_{CCIO} Voltage Level in I/O Bank 4				
		$V_{CCIO} = 3.3\text{ V}$	$V_{CCIO} = 2.5\text{ V}$	$V_{CCIO} = 1.8\text{ V}$	$V_{CCIO} = 1.5\text{ V}$	$V_{CCIO} = 1.2\text{ V}$
Non-Stratix II	VCC = 3.3 V	✓ (1)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 2.5 V	✓ (1), (4)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 1.8 V	✓ (1), (4)	✓ (2), (5)	✓	Level shifter required	Level shifter required
	VCC = 1.5 V	✓ (1), (4)	✓ (2), (5)	✓ (6)	✓	✓

Notes to Table 2–20:

- (1) The TDO output buffer meets $V_{OH}(\text{MIN}) = 2.4\text{ V}$.
- (2) The TDO output buffer meets $V_{OH}(\text{MIN}) = 2.0\text{ V}$.
- (3) An external $250\text{-}\Omega$ pull-up resistor is not required, but recommended if signal levels on the board are not optimal.
- (4) Input buffer must be 3.3-V tolerant.
- (5) Input buffer must be 2.5-V tolerant.
- (6) Input buffer must be 1.8-V tolerant.

High-Speed Differential I/O with DPA Support

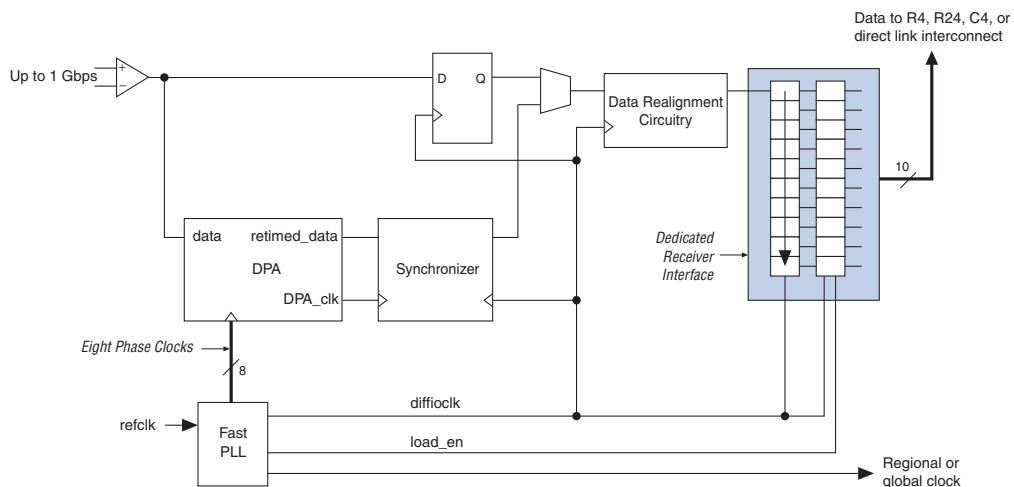
Stratix II devices contain dedicated circuitry for supporting differential standards at speeds up to 1 Gbps. The LVDS and HyperTransport differential I/O standards are supported in the Stratix II device. In addition, the LVPECL I/O standard is supported on input and output clock pins on the top and bottom I/O banks.

The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- Parallel RapidIO
- HyperTransport technology

There are four dedicated high-speed PLLs in the EP2S15 to EP2S30 devices and eight dedicated high-speed PLLs in the EP2S60 to EP2S180 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Tables 2–21 through 2–26 show the number of channels that each fast PLL can clock in each of the Stratix II devices. In Tables 2–21 through 2–26 the first row for each transmitter or receiver provides the number of channels driven directly by the PLL. The second row below it shows the maximum channels a PLL can drive if cross bank channels are used from the adjacent center PLL. For example, in the 484-pin FineLine BGA EP2S15

Figure 2–59. Stratix II Receiver Channel

An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the VCO can feed to the DPA circuitry.



For more information on the fast PLL, see the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of the channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Since every channel utilizing the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

IEEE Std. 1149.1 JTAG Boundary- Scan Support

All Stratix® II devices provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1. JTAG boundary-scan testing can be performed either before or after, but not during configuration. Stratix II devices can also use the JTAG port for configuration with the Quartus® II software or hardware using either Jam Files (.jam) or Jam Byte-Code Files (.jbc).

Stratix II devices support IOE I/O standard setting reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode through the `CONFIG_IO` instruction. You can use this capability for JTAG testing before configuration when some of the Stratix II pins drive or receive from other devices on the board using voltage-referenced standards. Because the Stratix II device may not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming those I/O standards via JTAG allows you to fully test I/O connections to other devices.

A device operating in JTAG mode uses four required pins, TDI, TDO, TMS, and TCK, and one optional pin, TRST. The TCK pin has an internal weak pull-down resistor, while the TDI, TMS and TRST pins have weak internal pull-ups. The JTAG input pins are powered by the 3.3-V `VCCPD` pins. The TDO output pin is powered by the `VCCIO` power supply of bank 4.

Stratix II devices also use the JTAG port to monitor the logic operation of the device with the SignalTap® II embedded logic analyzer. Stratix II devices support the JTAG instructions shown in [Table 3-1](#).



Stratix II, Stratix, Cyclone® II, and Cyclone devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix II, Stratix, Cyclone II, or Cyclone devices are in the 18th or further position, they fail configuration. This does not affect SignalTap II.

The Stratix II device instruction register length is 10 bits and the `USERCODE` register length is 32 bits. [Tables 3-2](#) and [3-3](#) show the boundary-scan register length and device `IDCODE` information for Stratix II devices.

The PLL_ENA pin and the configuration input pins (Table 3–4) have a dual buffer design: a 3.3-V/2.5-V input buffer and a 1.8-V/1.5-V input buffer. The VCCSEL input pin selects which input buffer is used. The 3.3-V/2.5-V input buffer is powered by V_{CCPD}, while the 1.8-V/1.5-V input buffer is powered by V_{CCIO}. Table 3–4 shows the pins affected by VCCSEL.

Table 3–4. Pins Affected by the Voltage Level at VCCSEL

Pin	VCCSEL = LOW (connected to GND)	VCCSEL = HIGH (connected to V _{CCPD})
nSTATUS (when used as an input)	3.3/2.5-V input buffer is selected. Input buffer is powered by V _{CCPD} .	1.8/1.5-V input buffer is selected. Input buffer is powered by V _{CCIO} of the I/O bank.
nCONFIG		
CONF_DONE (when used as an input)		
DATA[7..0]		
nCE		
DCLK (when used as an input)		
CS		
nWS		
nRS		
nCS		
CLKUSR		
DEV_OE		
DEV_CLRn		
RUnLU		
PLL_ENA		

VCCSEL is sampled during power-up. Therefore, the VCCSEL setting cannot change on the fly or during a reconfiguration. The VCCSEL input buffer is powered by V_{CCINT} and must be hardwired to V_{CCPD} or ground. A logic high VCCSEL connection selects the 1.8-V/1.5-V input buffer, and a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX[®] II/microprocessor.

If you need to support configuration input voltages of 3.3 V/2.5 V, you should set the VCCSEL to a logic low; you can set the V_{CCIO} of the I/O bank that contains the configuration inputs to any supported voltage. If

Configuring Stratix II FPGAs with the MicroBlaster Driver

The MicroBlaster™ software driver supports an RBF programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems. For more information on the MicroBlaster software driver, see the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *Configuring the MicroBlaster Passive Serial Software Driver White Paper* on the Altera web site (www.altera.com).

PLL Reconfiguration

The phase-locked loops (PLLs) in the Stratix II device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.



See the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information on Stratix II PLLs.

Temperature Sensing Diode (TSD)

Stratix II devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device. These devices steer bias current through the Stratix II diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus sign). The external device's output represents the junction temperature of the Stratix II device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix II device to connect to the external temperature-sensing device, as shown in [Figure 3-1](#). The temperature sensing diode is a passive element and therefore can be used before the Stratix II device is powered.

Operating Conditions

Stratix® II devices are offered in both commercial and industrial grades. Industrial devices are offered in -4 speed grades and commercial devices are offered in -3 (fastest), -4, -5 speed grades.

Tables 5–1 through 5–32 provide information about absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for Stratix II devices.

Absolute Maximum Ratings

Table 5–1 contains the absolute maximum ratings for the Stratix II device family.

Table 5–1. Stratix II Device Absolute Maximum Ratings <i>Notes (1), (2), (3)</i>					
Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Supply voltage	With respect to ground	–0.5	4.6	V
V_{CCPD}	Supply voltage	With respect to ground	–0.5	4.6	V
V_{CCA}	Analog power supply for PLLs	With respect to ground	–0.5	1.8	V
V_{CCD}	Digital power supply for PLLs	With respect to ground	–0.5	1.8	V
V_I	DC input voltage (4)		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_J	Junction temperature	BGA packages under bias	–55	125	°C

Notes to Tables 5–1

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Conditions beyond those listed in Table 5–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.
- (3) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.
- (4) During transitions, the inputs may overshoot to the voltage shown in Table 5–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 5–73. Stratix II I/O Input Delay for Column Pins (Part 3 of 3)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
1.2-V HSTL	t _{PI}	645	677	1194	1252	-	-	ps
	t _{PCOUT}	379	398	758	795	-	-	ps

Notes for Table 5–73:

- (1) These I/O standards are only supported on DQS pins.
- (2) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
- (3) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

Table 5–74. Stratix II I/O Input Delay for Row Pins (Part 1 of 2)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (1)	-3 Speed Grade (2)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
LVTTTL	t _{PI}	715	749	1287	1350	1477	1723	ps
	t _{PCOUT}	391	410	760	798	873	1018	ps
2.5 V	t _{PI}	726	761	1273	1335	1461	1704	ps
	t _{PCOUT}	402	422	746	783	857	999	ps
1.8 V	t _{PI}	788	827	1427	1497	1639	1911	ps
	t _{PCOUT}	464	488	900	945	1035	1206	ps
1.5 V	t _{PI}	792	830	1498	1571	1720	2006	ps
	t _{PCOUT}	468	491	971	1019	1116	1301	ps
LVCMOS	t _{PI}	715	749	1287	1350	1477	1723	ps
	t _{PCOUT}	391	410	760	798	873	1018	ps
SSTL-2 Class I	t _{PI}	547	573	879	921	1008	1176	ps
	t _{PCOUT}	223	234	352	369	404	471	ps
SSTL-2 Class II	t _{PI}	547	573	879	921	1008	1176	ps
	t _{PCOUT}	223	234	352	369	404	471	ps
SSTL-18 Class I	t _{PI}	577	605	960	1006	1101	1285	ps
	t _{PCOUT}	253	266	433	454	497	580	ps
SSTL-18 Class II	t _{PI}	577	605	960	1006	1101	1285	ps
	t _{PCOUT}	253	266	433	454	497	580	ps
1.5-V HSTL Class I	t _{PI}	602	631	1056	1107	1212	1413	ps
	t _{PCOUT}	278	292	529	555	608	708	ps

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 6 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
Differential SSTL-2 Class I	8 mA	t _{OP}	913	957	1715	1799	1971	2041	ps
		t _{DIP}	933	979	1781	1869	2047	2131	ps
	12 mA	t _{OP}	896	940	1672	1754	1921	1991	ps
		t _{DIP}	916	962	1738	1824	1997	2081	ps
Differential SSTL-2 Class II	16 mA	t _{OP}	876	918	1609	1688	1849	1918	ps
		t _{DIP}	896	940	1675	1758	1925	2008	ps
	20 mA	t _{OP}	877	919	1598	1676	1836	1905	ps
		t _{DIP}	897	941	1664	1746	1912	1995	ps
	24 mA	t _{OP}	872	915	1596	1674	1834	1903	ps
		t _{DIP}	892	937	1662	1744	1910	1993	ps
Differential SSTL-18 Class I	4 mA	t _{OP}	909	953	1690	1773	1942	2012	ps
		t _{DIP}	929	975	1756	1843	2018	2102	ps
	6 mA	t _{OP}	914	958	1656	1737	1903	1973	ps
		t _{DIP}	934	980	1722	1807	1979	2063	ps
	8 mA	t _{OP}	894	937	1640	1721	1885	1954	ps
		t _{DIP}	914	959	1706	1791	1961	2044	ps
	10 mA	t _{OP}	898	942	1638	1718	1882	1952	ps
		t _{DIP}	918	964	1704	1788	1958	2042	ps
	12 mA	t _{OP}	891	936	1626	1706	1869	1938	ps
		t _{DIP}	911	958	1692	1776	1945	2028	ps
Differential SSTL-18 Class II	8 mA	t _{OP}	883	925	1597	1675	1835	1904	ps
		t _{DIP}	903	947	1663	1745	1911	1994	ps
	16 mA	t _{OP}	894	937	1578	1655	1813	1882	ps
		t _{DIP}	914	959	1644	1725	1889	1972	ps
	18 mA	t _{OP}	890	933	1585	1663	1821	1890	ps
		t _{DIP}	910	955	1651	1733	1897	1980	ps
	20 mA	t _{OP}	890	933	1583	1661	1819	1888	ps
		t _{DIP}	910	955	1649	1731	1895	1978	ps

Table 5–80. Maximum DCD for Non-DDIO Output on Row I/O Pins (Part 2 of 2) *Note (1)*

Row I/O Output Standard	Maximum DCD for Non-DDIO Output		
	-3 Devices	-4 & -5 Devices	Unit
1.8 V	180	180	ps
1.5-V LVCMOS	165	195	ps
SSTL-2 Class I	115	145	ps
SSTL-2 Class II	95	125	ps
SSTL-18 Class I	55	85	ps
1.8-V HSTL Class I	80	100	ps
1.5-V HSTL Class I	85	115	ps
LVDS/ HyperTransport technology	55	80	ps

Note to Table 5–80:

- (1) The DCD specification is based on a no logic array noise condition.

Here is an example for calculating the DCD as a percentage for a non-DDIO output on a row I/O on a -3 device:

If the non-DDIO output I/O standard is SSTL-2 Class II, the maximum DCD is 95 ps (see Table 5–80). If the clock frequency is 267 MHz, the clock period T is:

$$T = 1 / f = 1 / 267 \text{ MHz} = 3.745 \text{ ns} = 3745 \text{ ps}$$

To calculate the DCD as a percentage:

$$(T/2 - \text{DCD}) / T = (3745\text{ps}/2 - 95\text{ps}) / 3745\text{ps} = 47.5\% \text{ (for low boundary)}$$

$$(T/2 + \text{DCD}) / T = (3745\text{ps}/2 + 95\text{ps}) / 3745\text{ps} = 52.5\% \text{ (for high boundary)}$$



6. Reference & Ordering Information

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Software

Stratix® II devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration. See the *Quartus II Handbook* for more information on the Quartus II software features.

The Quartus II software supports the Windows XP/2000/NT/98, Sun Solaris, Linux Red Hat v7.1 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

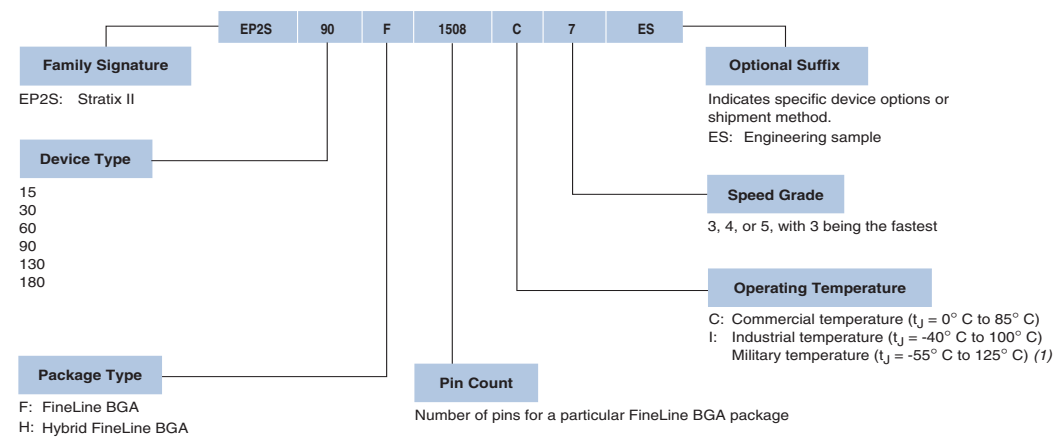
Device Pin-Outs

Device pin-outs for Stratix II devices are available on the Altera web site at (www.altera.com).

Ordering Information

Figure 6–1 describes the ordering codes for Stratix II devices. For more information on a specific package, refer to the *Package Information for Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

Figure 6–1. Stratix II Device Packaging Ordering Information



Note to Figure 6–1:
(1) Applicable to I4 devices. For more information, refer to the *Stratix II Military Temperature Range Support* technical brief.

Document Revision History Table 6–1 shows the revision history for this chapter.

Table 6–1. Document Revision History		
Date and Document Version	Changes Made	Summary of Changes
April 2011, v2.2	Updated Figure 6–1.	Added operating junction temperature for military use.
May 2007, v2.1	Moved the Document Revision History section to the end of the chapter.	—
January 2005, v2.0	Contact information was removed.	—
October 2004, v1.1	Updated Figure 6–1.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—