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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	6627
Number of Logic Elements/Cells	132540
Total RAM Bits	6747840
Number of I/O	534
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2s130f780c5n

About this Handbook

This handbook provides comprehensive information about the Altera® Stratix® II family of devices.

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Email	www.altera.com/literature
Altera literature services	Website	literature@altera.com
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

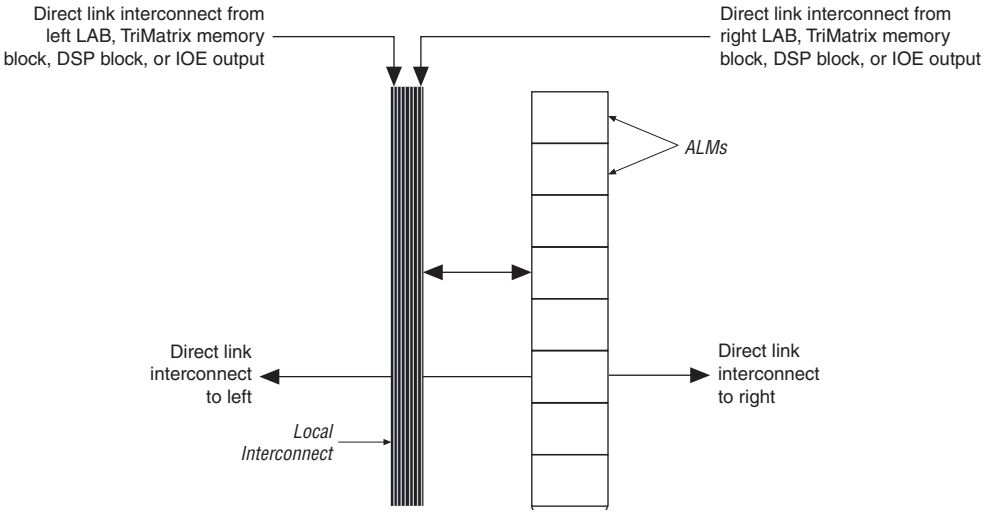
Note to table:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*

Figure 2–3. Direct Link Connection



LAB Control Signals

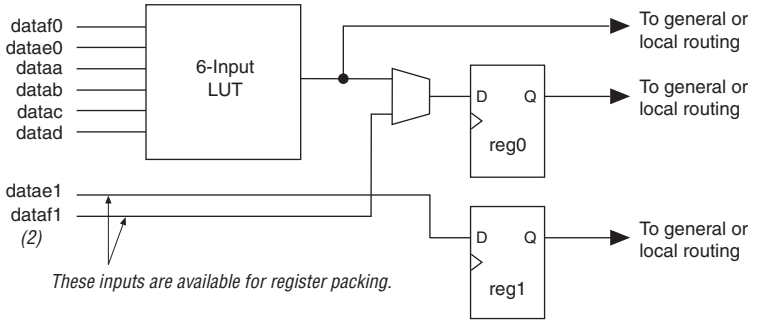
Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, and synchronous load control signals. This gives a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2–4. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. By default, the Quartus II software uses a `NOT` gate push-back technique to achieve preset. If you disable the `NOT` gate push-up option or assign a given register to power up high using the Quartus II software, the preset is achieved using the asynchronous load

datae1 and dataf1 are utilized, the output drives to register1 and/or bypasses register1 and drives to the interconnect using the bottom set of output drivers. The Quartus II Compiler automatically selects the inputs to the LUT. Asynchronous load data for the register comes from the datae or dataf input of the ALM. ALMs in normal mode support register packing.

Figure 2–9. 6-Input Function in Normal Mode *Notes (1), (2)*



Notes to Figure 2–9:

(1) If datae1 and dataf1 are used as inputs to the six-input function, then datae0 and dataf0 are available for register packing.

(2) The dataf1 input is available for register packing only if the six-input function is un-registered.

Extended LUT Mode

The extended LUT mode is used to implement a specific set of seven-input functions. The set must be a 2-to-1 multiplexer fed by two arbitrary five-input functions sharing four inputs. Figure 2–10 shows the template of supported seven-input functions utilizing extended LUT mode. In this mode, if the seven-input function is unregistered, the unused eighth input is available for register packing.

Functions that fit into the template shown in Figure 2–10 occur naturally in designs. These functions often appear in designs as "if-else" statements in Verilog HDL or VHDL code.

R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and Row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect. These column resources include:

- Shared arithmetic chain interconnects in an LAB
- Carry chain interconnects in an LAB and from LAB to LAB
- Register chain interconnects in an LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix II devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM to ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–17 shows the shared arithmetic chain, carry chain and register chain interconnects.

Table 2–3. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support		✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Output registers	Output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

Notes to Table 2–3:

(1) The M-RAM block does not support memory initializations. However, the M-RAM block can emulate a ROM function using a dual-port RAM bock. The Stratix II device must write to the dual-port memory once and then disable the write-enable ports afterwards.

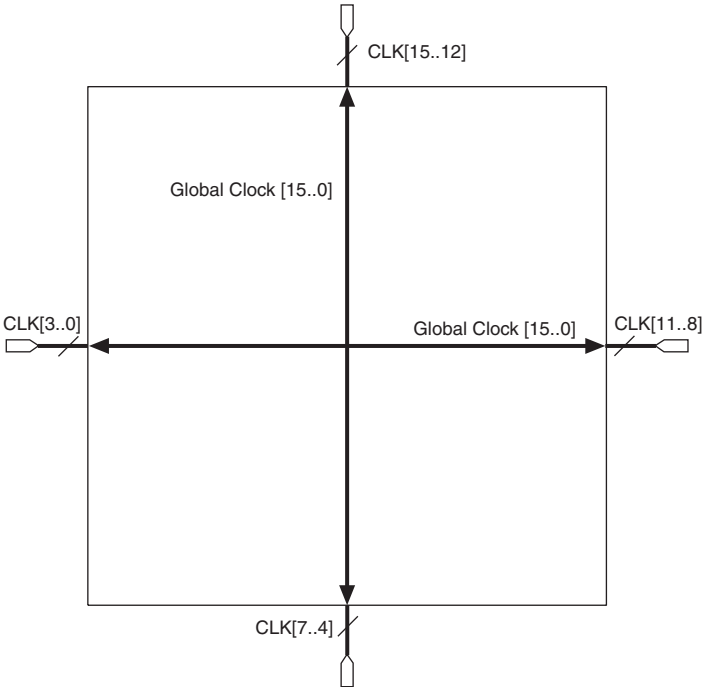
Memory Block Size

TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

When applied to input registers, the asynchronous clear signal for the TriMatrix embedded memory immediately clears the input registers. However, the output of the memory block does not show the effects until the next clock edge. When applied to output registers, the asynchronous clear signal clears the output registers and the effects are seen immediately.

global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–31 shows the 16 dedicated CLK pins driving global clock networks.

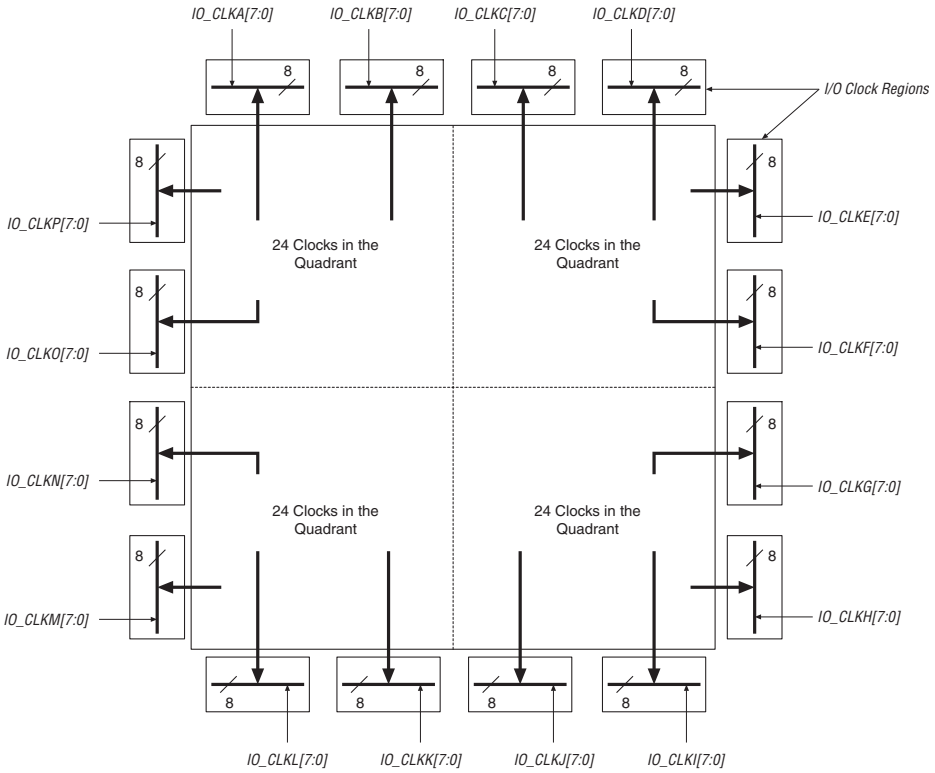
Figure 2–31. Global Clocking



Regional Clock Network

There are eight regional clock networks RCLK[7..0] in each quadrant of the Stratix II device that are driven by the dedicated CLK[15..0] input pins, by PLL outputs, or by internal logic. The regional clock networks provide the lowest clock delay and skew for logic contained in a single quadrant. The CLK clock pins symmetrically drive the RCLK networks in a particular quadrant, as shown in Figure 2–32.

Figure 2–36. EP2S60, EP2S90, EP2S130 & EP2S180 Device I/O Clock Groups



You can use the Quartus II software to control whether a clock input pin drives either a global, regional, or dual-regional clock network. The Quartus II software automatically selects the clocking resources if not specified.

Clock Control Block

Each global clock, regional clock, and PLL external clock output has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable/disable)

Each I/O bank has its own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different V_{CCIO} level independently. Each bank also has dedicated VREF pins to support the voltage-referenced standards (such as SSTL-2). The PLL banks utilize the adjacent VREF group when voltage-referenced standards are implemented. For example, if an SSTL input is implemented in PLL bank 10, the voltage level at VREFB7 is the reference voltage level for the SSTL input.

I/O pins that reside in PLL banks 9 through 12 are powered by the VCC_PLL<*5, 6, 11, or 12*>_OUT pins, respectively. The EP2S60F484, EP2S60F780, EP2S90H484, EP2S90F780, and EP2S130F780 devices do not support PLLs 11 and 12. Therefore, any I/O pins that reside in bank 11 are powered by the VCCIO3 pin, and any I/O pins that reside in bank 12 are powered by the VCCIO8 pin.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one V_{REF} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs.

On-Chip Termination

Stratix II devices provide differential (for the LVDS or HyperTransport technology I/O standard), series, and parallel on-chip termination to reduce reflections and maintain signal integrity. On-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections.

Stratix II devices provide four types of termination:

- Differential termination (R_D)
- Series termination (R_S) without calibration
- Series termination (R_S) with calibration
- Parallel termination (R_T) with calibration

Table 2–17. On-Chip Termination Support by I/O Banks (Part 2 of 2)

On-Chip Termination Support	I/O Standard Support	Top & Bottom Banks	Left & Right Banks
Series termination with calibration	3.3-V LVTTL	✓	
	3.3-V LVCMOS	✓	
	2.5-V LVTTL	✓	
	2.5-V LVCMOS	✓	
	1.8-V LVTTL	✓	
	1.8-V LVCMOS	✓	
	1.5-V LVTTL	✓	
	1.5-V LVCMOS	✓	
	SSTL-2 Class I and II	✓	
	SSTL-18 Class I and II	✓	
	1.8-V HSTL Class I	✓	
	1.8-V HSTL Class II	✓	
	1.5-V HSTL Class I	✓	
	1.2-V HSTL	✓	
Parallel termination with calibration	SSTL-2 Class I and II	✓	
	SSTL-18 Class I and II	✓	
	1.8-V HSTL Class I	✓	
	1.8-V HSTL Class II	✓	
	1.5-V HSTL Class I and II	✓	
	1.2-V HSTL	✓	
Differential termination *(1)*	LVDS		✓
	HyperTransport technology		✓

Note to Table 2–17:

(1) Clock pins `CLK1`, `CLK3`, `CLK9`, `CLK11`, and pins `FPLL[7..10]CLK` do not support differential on-chip termination. Clock pins `CLK0`, `CLK2`, `CLK8`, and `CLK10` do support differential on-chip termination. Clock pins in the top and bottom banks (`CLK[4..7, 12..15]`) do not support differential on-chip termination.

device, PLL 1 can drive a maximum of 10 transmitter channels in I/O bank 1 or a maximum of 19 transmitter channels in I/O banks 1 and 2. The Quartus II software may also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

Table 2–21. EP2S15 Device Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs			
			PLL 1	PLL 2	PLL 3	PLL 4
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21
672-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21

Table 2–22. EP2S30 Device Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs			
			PLL 1	PLL 2	PLL 3	PLL 4
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21
672-pin FineLine BGA	Transmitter	58 *(2)*	16	13	13	16
		(3)	29	29	29	29
	Receiver	62 *(2)*	17	14	14	17
		(3)	31	31	31	31

For more information on JTAG, see the following documents:

- The *IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing for Stratix II & Stratix II GX Devices* chapter of the *Stratix II Device Handbook, Volume 2* or the *Stratix II GX Device Handbook, Volume 2*
- Jam Programming & Test Language Specification

SignalTap II Embedded Logic Analyzer

Stratix II devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA® packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Stratix II architecture are configured with CMOS SRAM elements. Altera® FPGA devices are reconfigurable and every device is tested with a high coverage production test program so you do not have to perform fault testing and can instead focus on simulation and design verification.

Stratix II devices are configured at system power-up with data stored in an Altera configuration device or provided by an external controller (e.g., a MAX® II device or microprocessor). Stratix II devices can be configured using the fast passive parallel (FPP), active serial (AS), passive serial (PS), passive parallel asynchronous (PPA), and JTAG configuration schemes. The Stratix II device's optimized interface allows microprocessors to configure it serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat Stratix II devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy.

In addition to the number of configuration methods supported, Stratix II devices also offer the design security, decompression, and remote system upgrade features. The design security feature, using configuration bitstream encryption and AES technology, provides a mechanism to protect your designs. The decompression feature allows Stratix II FPGAs to receive a compressed configuration bitstream and decompress this data in real-time, reducing storage requirements and configuration time. The remote system upgrade feature allows real-time system upgrades from remote locations of your Stratix II designs. For more information, see "Configuration Schemes" on page 3–7.

Operating Modes

The Stratix II architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Stratix II devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

PORSEL is a dedicated input pin used to select POR delay times of 12 ms or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms; when the PORSEL pin is connected to V_{CC}, the POR time is 12 ms.

The nIO PULLUP pin is a dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose configuration I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[2..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLR) are on or off before and during configuration. A logic high (1.5, 1.8, 2.5, 3.3 V) turns off the weak internal pull-ups, while a logic low turns them on.

Stratix II devices also offer a new power supply, V_{CCPD}, which must be connected to 3.3 V in order to power the 3.3-V/2.5-V buffer available on the configuration input pins and JTAG pins. V_{CCPD} applies to all the JTAG input pins (TCK, TMS, TDI, and TRST) and the configuration input pins when VCCSEL is connected to ground. See Table 3–4 for more information on the pins affected by VCCSEL.

The VCCSEL pin allows the V_{CCIO} setting (of the banks where the configuration inputs reside) to be independent of the voltage required by the configuration inputs. Therefore, when selecting the V_{CCIO}, the V_{IL} and V_{IH} levels driven to the configuration inputs do not have to be a concern.

Table 5–14. 3.3-V PCI Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low-level input voltage		–0.3		$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–15. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.30		$0.35 \times V_{CCIO}$	V
V_{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–16. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Reference voltage		0.855	0.900	0.945	V
V_{TT}	Termination voltage		$V_{REF} – 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{IH} (DC)	High-level DC input voltage		$V_{REF} + 0.125$			V
V_{IL} (DC)	Low-level DC input voltage				$V_{REF} – 0.125$	V
V_{IH} (AC)	High-level AC input voltage		$V_{REF} + 0.25$			V
V_{IL} (AC)	Low-level AC input voltage				$V_{REF} – 0.25$	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	$V_{TT} + 0.475$			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*			$V_{TT} – 0.475$	V

Note to Table 5–16:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–31. Series & Differential On-Chip Termination Specification for Left & Right I/O Banks

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25-Ω R_S 3.3/2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	±30	%
50-Ω R_S 3.3/2.5/1.8	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5/1.8 V	±30	±30	%
50-Ω R_S 1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±36	±36	%
R_D	Internal differential termination for LVDS or HyperTransport technology (100-Ω setting)	V_{CCIO} = 2.5 V	±20	±25	%

Pin Capacitance

Table 5–32 shows the Stratix II device family pin capacitance.

Table 5–32. Stratix II Device Capacitance *Note (1)*

Symbol	Parameter	Typical	Unit
C_{IOTB}	Input capacitance on I/O pins in I/O banks 3, 4, 7, and 8.	5.0	pF
C_{IOLR}	Input capacitance on I/O pins in I/O banks 1, 2, 5, and 6, including high-speed differential receiver and transmitter pins.	6.1	pF
C_{CLKTB}	Input capacitance on top/bottom clock input pins: `CLK[4..7]` and `CLK[12..15]`.	6.0	pF
C_{CLKLR}	Input capacitance on left/right clock inputs: `CLK0`, `CLK2`, `CLK8`, `CLK10`.	6.1	pF
C_{CLKLR+}	Input capacitance on left/right clock inputs: `CLK1`, `CLK3`, `CLK9`, and `CLK11`.	3.3	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins in PLL banks 9, 10, 11, and 12.	6.7	pF

Note to Table 5–32:

(1) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within ±0.5pF

Table 5–34. Output Timing Measurement Methodology for Output Pins *Notes (1), (2), (3)*

I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
LVTTL *(4)*				3.135		0	1.5675
LVCMOS *(4)*				3.135		0	1.5675
2.5 V *(4)*				2.375		0	1.1875
1.8 V *(4)*				1.710		0	0.855
1.5 V *(4)*				1.425		0	0.7125
PCI *(5)*				2.970		10	1.485
PCI-X *(5)*				2.970		10	1.485
SSTL-2 Class I	25		50	2.325	1.123	0	1.1625
SSTL-2 Class II	25		25	2.325	1.123	0	1.1625
SSTL-18 Class I	25		50	1.660	0.790	0	0.83
SSTL-18 Class II	25		25	1.660	0.790	0	0.83
1.8-V HSTL Class I	50		50	1.660	0.790	0	0.83
1.8-V HSTL Class II	25		25	1.660	0.790	0	0.83
1.5-V HSTL Class I	50		50	1.375	0.648	0	0.6875
1.5-V HSTL Class II			25	1.375	0.648	0	0.6875
1.2-V HSTL with OCT	50			1.140		0	0.570
Differential SSTL-2 Class I	50		50	2.325	1.123	0	1.1625
Differential SSTL-2 Class II	25		25	2.325	1.123	0	1.1625
Differential SSTL-18 Class I	50		50	1.660	0.790	0	0.83
Differential SSTL-18 Class II	25		25	1.660	0.790	0	0.83
1.5-V Differential HSTL Class I	50		50	1.375	0.648	0	0.6875
1.5-V Differential HSTL Class II			25	1.375	0.648	0	0.6875
1.8-V Differential HSTL Class I	50		50	1.660	0.790	0	0.83
1.8-V Differential HSTL Class II	25		25	1.660	0.790	0	0.83
LVDS		100		2.325		0	1.1625
HyperTransport		100		2.325		0	1.1625
LVPECL		100		3.135		0	1.5675

Notes to Table 5–34:

(1) Input measurement point at internal node is $0.5 \times V_{CCINT}$.

(2) Output measuring point for V_{MEAS} at buffer output is $0.5 \times V_{CCIO}$.

(3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.

(4) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple

(5) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V

Table 5–38. IOE Internal Timing Microparameters

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min (3)	Max	Min (3)	Max	Min (4)	Max	Min (3)	Max	
t_{SU}	IOE input and output register setup time before clock	122		128		140 140		163		ps
t_{H}	IOE input and output register hold time after clock	72		75		82 82		96		ps
t_{CO}	IOE input and output register clock-to-output delay	101	169	101	177	97 101	194	101	226	ps
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinational output	410	760	410	798	391 410	873	410	1,018	ps
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinational output	428	787	428	825	408 428	904	428	1,054	ps
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinational output pin	1,101	2,026	1,101	2,127	1,049 1,101	2,329	1,101	2,439	ps
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinational output pin	991	1,854	991	1,946	944 991	2,131	991	2,246	ps
t_{CLR}	Minimum clear pulse width	200		210		229 229		268		ps
t_{PRE}	Minimum preset pulse width	200		210		229 229		268		ps
t_{CLKL}	Minimum clock low time	600		630		690 690		804		ps
t_{CLKH}	Minimum clock high time	600		630		690 690		804		ps

Notes to Table 5–38:

(1) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.

(2) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

(3) For the -3 and -5 speed grades, the minimum timing is for the commercial temperature grade. Only -4 speed grade devices offer the industrial temperature grade.

(4) For the -4 speed grade, the first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.

Table 5–39. DSP Block Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade *(1)*		-3 Speed Grade *(2)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min *(3)*	Max	Min *(3)*	Max	Min *(4)*	Max	Min *(3)*	Max	
t_{SU}	Input, pipeline, and output register setup time before clock	50		52		57 57		67		ps
t_{H}	Input, pipeline, and output register hold time after clock	180		189		206 206		241		ps
t_{CO}	Input, pipeline, and output register clock-to-output delay	0	0	0	0	0 0	0	0	0	ps
$t_{INREG2PIPE9}$	Input register to DSP block pipeline register in 9 × 9-bit mode	1,312	2,030	1,312	2,030	1,250 1,312	2,334	1,312	2,720	ps
$t_{INREG2PIPE18}$	Input register to DSP block pipeline register in 18 × 18-bit mode	1,302	2,010	1,302	2,110	1,240 1,302	2,311	1,302	2,693	ps
$t_{INREG2PIPE36}$	Input register to DSP block pipeline register in 36 × 36-bit mode	1,302	2,010	1,302	2,110	1,240 1,302	2,311	1,302	2,693	ps
$t_{PIPE2OUTREG2ADD}$	DSP block pipeline register to output register delay in two-multipliers adder mode	924	1,450	924	1,522	880 924	1,667	924	1,943	ps
$t_{PIPE2OUTREG4ADD}$	DSP block pipeline register to output register delay in four-multipliers adder mode	1,134	1,850	1,134	1,942	1,080 1,134	2,127	1,134	2,479	ps
t_{PD9}	Combinational input to output delay for 9 × 9	2,100	2,880	2,100	3,024	2,000 2,100	3,312	2,100	3,859	ps
t_{PD18}	Combinational input to output delay for 18 × 18	2,110	2,990	2,110	3,139	2,010 2,110	3,438	2,110	4,006	ps
t_{PD36}	Combinational input to output delay for 36 × 36	2,939	4,450	2,939	4,672	2,800 2,939	5,117	2,939	5,962	ps
t_{CLR}	Minimum clear pulse width	2,212		2,322		2,543 2,543		2,964		ps

Table 5–42. M-RAM Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min (4)	Max	Min (4)	Max	Min (5)	Max	Min (4)	Max	
$t_{MEGACLKH}$	Minimum clock high time	1,250		1,312		1,437 1,437		1,675		ps
$t_{MEGACLR}$	Minimum clear pulse width	144		151		165 165		192		ps

Notes to Table 5–42:

(1) F_{MAX} of M-RAM Block obtained using the Quartus II software does not necessarily equal to 1/TMEGARC.
(2) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(3) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.
(4) For the -3 and -5 speed grades, the minimum timing is for the commercial temperature grade. Only -4 speed grade devices offer the industrial temperature grade.
(5) For the -4 speed grade, the first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.

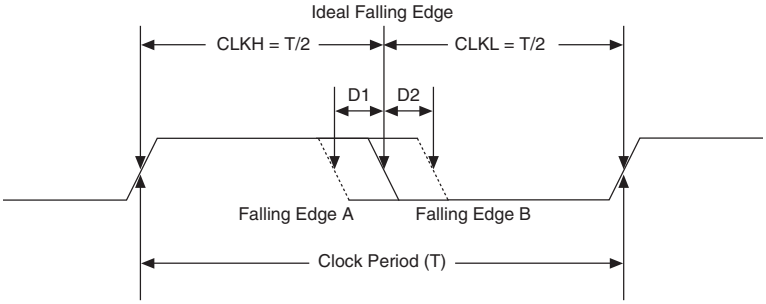
Stratix II Clock Timing Parameters

See Tables 5–43 through 5–67 for Stratix II clock timing parameters.

Table 5–43. Stratix II Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL `inclk` pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL `inclk` pad to I/O output register

Figure 5–7. Duty Cycle Distortion



DCD expressed in absolution derivation, for example, D1 or D2 in Figure 5–7, is clock-period independent. DCD can also be expressed as a percentage, and the percentage number is clock-period dependent. DCD as a percentage is defined as

(T/2 – D1) / T (the low percentage boundary)

(T/2 + D2) / T (the high percentage boundary)

DCD Measurement Techniques

DCD is measured at an FPGA output pin driven by registers inside the corresponding I/O element (IOE) block. When the output is a single data rate signal (non-DDIO), only one edge of the register input clock (positive or negative) triggers output transitions (Figure 5–8). Therefore, any DCD present on the input clock signal or caused by the clock input buffer or different input I/O standard does not transfer to the output signal.

Figure 5–8. DCD Measurement Technique for Non-DDIO (Single-Data Rate) Outputs

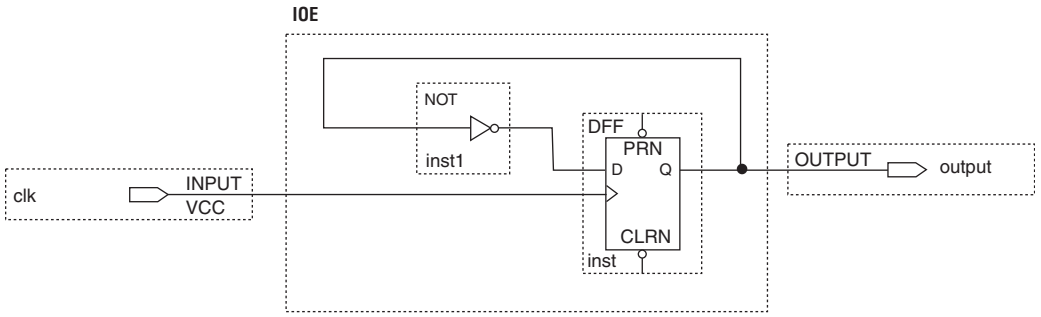


Table 5–80. Maximum DCD for Non-DDIO Output on Row I/O Pins (Part 2 of 2) *Note (1)*

Row I/O Output Standard	Maximum DCD for Non-DDIO Output		
	-3 Devices	-4 & -5 Devices	Unit
1.8 V	180	180	ps
1.5-V LVCMOS	165	195	ps
SSTL-2 Class I	115	145	ps
SSTL-2 Class II	95	125	ps
SSTL-18 Class I	55	85	ps
1.8-V HSTL Class I	80	100	ps
1.5-V HSTL Class I	85	115	ps
LVDS/ HyperTransport technology	55	80	ps

Note to Table 5–80:
(1) The DCD specification is based on a no logic array noise condition.

Here is an example for calculating the DCD as a percentage for a non-DDIO output on a row I/O on a -3 device:

If the non-DDIO output I/O standard is SSTL-2 Class II, the maximum DCD is 95 ps (see Table 5–80). If the clock frequency is 267 MHz, the clock period T is:

T = 1/ f = 1 / 267 MHz = 3.745 ns = 3745 ps

To calculate the DCD as a percentage:

(T/2 – DCD) / T = (3745ps/2 – 95ps) / 3745ps = 47.5% (for low boundary)

(T/2 + DCD) / T = (3745ps/2 + 95ps) / 3745ps = 52.5% (for high boundary)