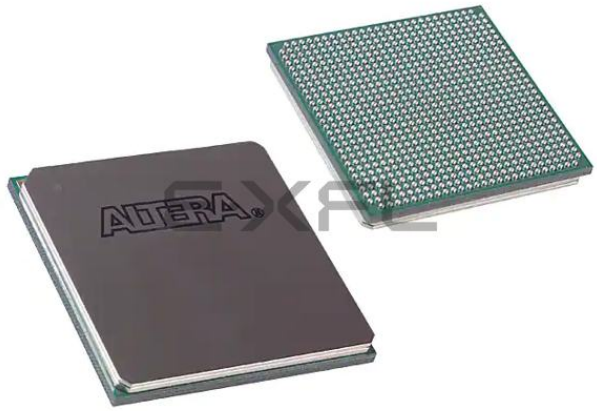

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6627
Number of Logic Elements/Cells	132540
Total RAM Bits	6747840
Number of I/O	534
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s130f780i4n

Stratix II devices are available in space-saving FineLine BGA® packages (see Tables 1–2 and 1–3).

Table 1–2. Stratix II Package Options & I/O Pin Counts *Notes (1), (2)*

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	342		366			
EP2S30	342		500			
EP2S60 *(3)*	334		492		718	
EP2S90 *(3)*		308		534	758	902
EP2S130 *(3)*				534	742	1,126
EP2S180 *(3)*					742	1,170

Notes to Table 1–2:

(1) All I/O pin counts include eight dedicated clock input pins (`clk1p`, `clk1n`, `clk3p`, `clk3n`, `clk9p`, `clk9n`, `clk11p`, and `clk11n`) that can be used for data inputs.

(2) The Quartus II software I/O pin counts include one additional pin, `PLL_ENA`, which is not available as general-purpose I/O pins. The `PLL_ENA` pin can only be used to enable the PLLs within the device.

(3) The I/O pin counts for the EP2S60, EP2S90, EP2S130, and EP2S180 devices in the 1020-pin and 1508-pin packages include eight dedicated fast PLL clock inputs (`FPLL7CLKp/n`, `FPLL8CLKp/n`, `FPLL9CLKp/n`, and `FPLL10CLKp/n`) that can be used for data inputs.

Table 1–3. Stratix II FineLine BGA Package Sizes

Dimension	484 Pin	484-Pin Hybrid	672 Pin	780 Pin	1,020 Pin	1,508 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00
Area (mm2)	529	729	729	841	1,089	1,600
Length × width (mm × mm)	23 × 23	27 × 27	27 × 27	29 × 29	33 × 33	40 × 40

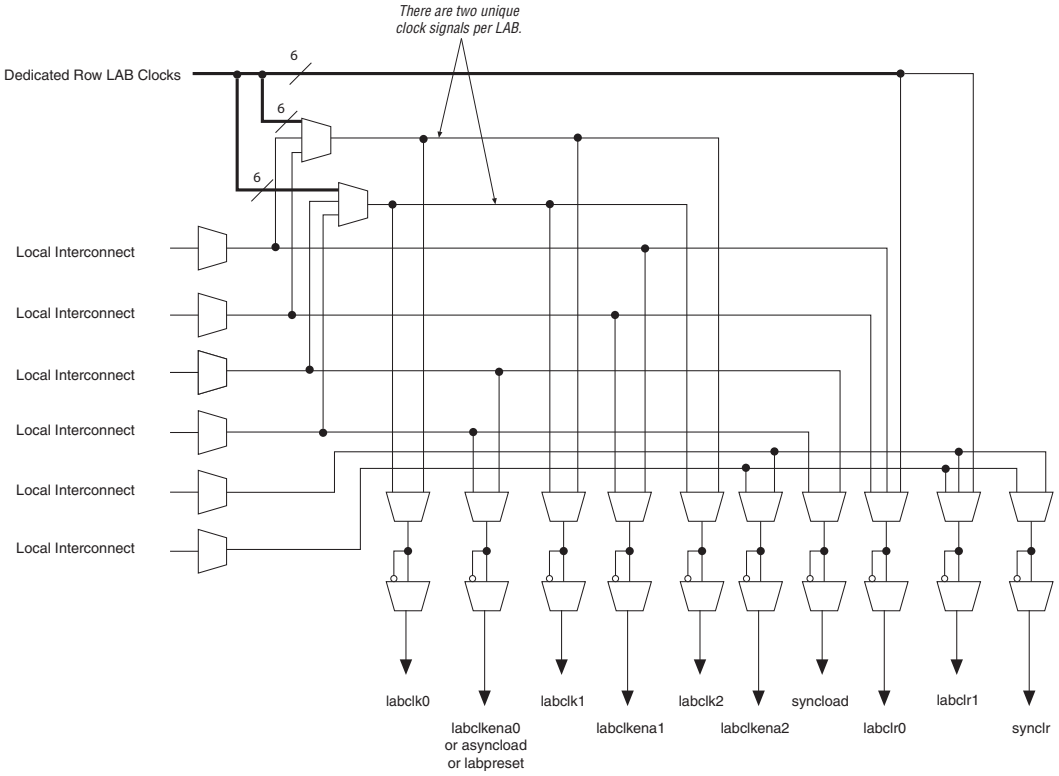
All Stratix II devices support vertical migration within the same package (for example, you can migrate between the EP2S15, EP2S30, and EP2S60 devices in the 672-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

To ensure that a board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus II software (Assignments menu > Device > Migration Devices).

signal with asynchronous load data input tied high. When the asynchronous load/preset signal is used, the `labclkena0` signal is no longer available.

The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–4 shows the LAB control signal generation circuit.

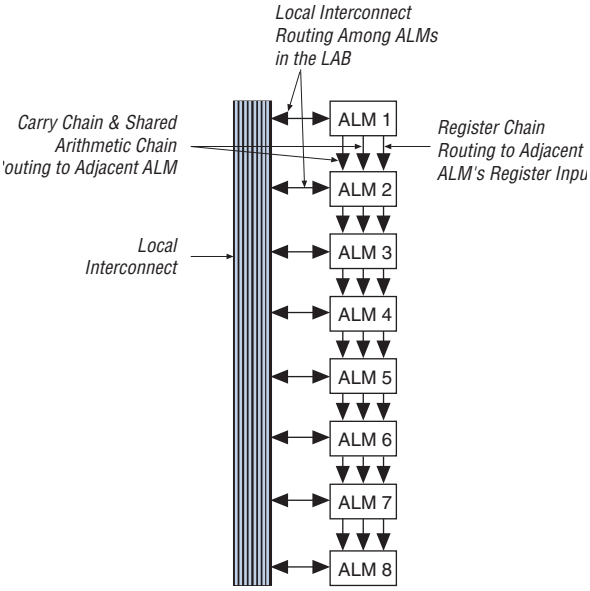
Figure 2–4. LAB-Wide Control Signals



Adaptive Logic Modules

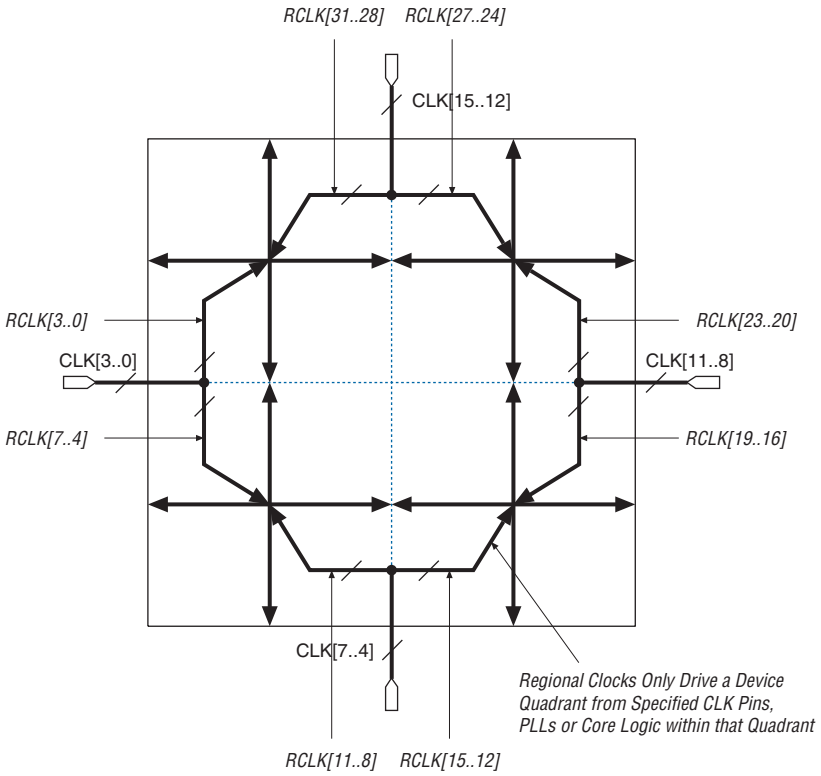
The basic building block of logic in the Stratix II architecture, the adaptive logic module (ALM), provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be

Figure 2–17. Shared Arithmetic Chain, Carry Chain & Register Chain Interconnects



The C4 interconnects span four LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–18 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2–32. Regional Clocks



Dual-Regional Clock Network

A single source (CLK pin or PLL output) can generate a dual-regional clock by driving two regional clock network lines in adjacent quadrants (one from each quadrant). This allows logic that spans multiple quadrants to utilize the same low skew clock. The routing of this clock signal on an entire side has approximately the same speed but slightly higher clock skew when compared with a clock signal that drives a single quadrant. Internal logic-array routing can also drive a dual-regional clock. Clock pins and enhanced PLL outputs on the top and bottom can drive horizontal dual-regional clocks. Clock pins and fast PLL outputs on the left and right can drive vertical dual-regional clocks, as shown in Figure 2–33. Corner PLLs cannot drive dual-regional clocks.

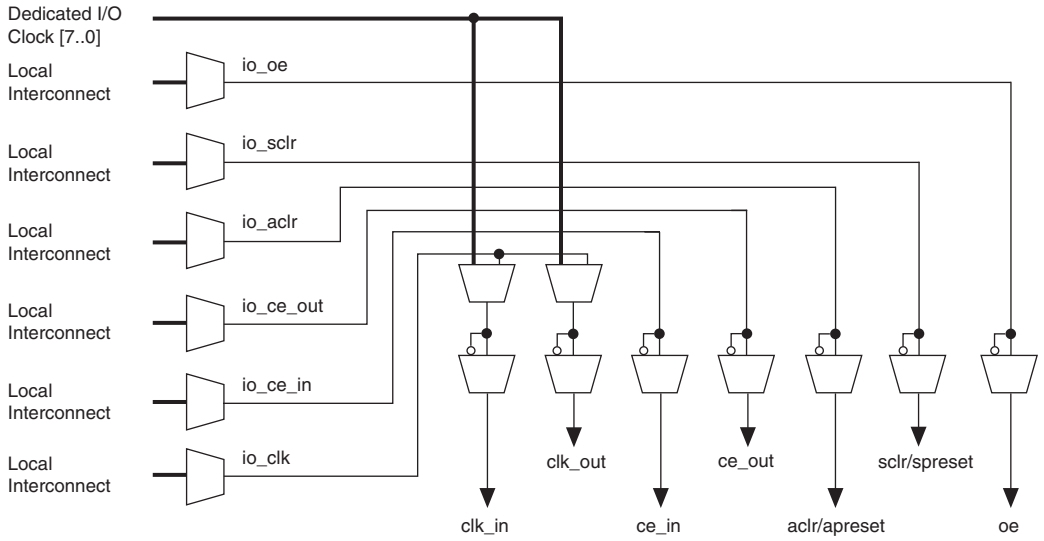
Table 2–11. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs (Part 2 of 2)

Top Side Global & Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
c4	✓					✓		✓		✓		✓	
c5	✓						✓		✓		✓		✓
Enhanced PLL 11 outputs													
c0		✓	✓			✓				✓			
c1		✓	✓				✓				✓		
c2				✓	✓			✓				✓	
c3				✓	✓				✓				✓
c4						✓		✓		✓		✓	
c5							✓		✓		✓		✓

Table 2–12. Global & Regional Clock Connections from Bottom Clock Pins & Enhanced PLL Outputs (Part 1 of 2)

Bottom Side Global & Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
Clock pins													
CLK4p	✓	✓	✓			✓				✓			
CLK5p	✓	✓	✓				✓				✓		
CLK6p	✓			✓	✓			✓				✓	
CLK7p	✓			✓	✓				✓				✓
CLK4n		✓				✓				✓			
CLK5n			✓				✓				✓		
CLK6n				✓				✓				✓	
CLK7n					✓				✓				✓
Drivers from internal logic													
GCLKDRV0		✓											
GCLKDRV1			✓										
GCLKDRV2				✓									

Figure 2–50. Control Signal Selection per IOE



Notes to Figure 2–50:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects.

- 1.5-V HSTL Class I and II
- 1.8-V HSTL Class I and II
- 1.2-V HSTL
- SSTL-2 Class I and II
- SSTL-18 Class I and II

Table 2–16 describes the I/O standards supported by Stratix II devices.

Table 2–16. Stratix II Supported I/O Standards (Part 1 of 2)

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	-	3.3	-
LVCMOS	Single-ended	-	3.3	-
2.5 V	Single-ended	-	2.5	-
1.8 V	Single-ended	-	1.8	-
1.5-V LVCMOS	Single-ended	-	1.5	-
3.3-V PCI	Single-ended	-	3.3	-
3.3-V PCI-X mode 1	Single-ended	-	3.3	-
LVDS	Differential	-	2.5 *(3)*	-
LVPECL *(1)*	Differential	-	3.3	-
HyperTransport technology	Differential	-	2.5	-
Differential 1.5-V HSTL Class I and II *(2)*	Differential	0.75	1.5	0.75
Differential 1.8-V HSTL Class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-18 Class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-2 Class I and II *(2)*	Differential	1.25	2.5	1.25
1.2-V HSTL*(4)*	Voltage-referenced	0.6	1.2	0.6
1.5-V HSTL Class I and II	Voltage-referenced	0.75	1.5	0.75
1.8-V HSTL Class I and II	Voltage-referenced	0.9	1.8	0.9
SSTL-18 Class I and II	Voltage-referenced	0.90	1.8	0.90

Configuring Stratix II FPGAs with the MicroBlaster Driver

The MicroBlaster™ software driver supports an RBF programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems. For more information on the MicroBlaster software driver, see the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *Configuring the MicroBlaster Passive Serial Software Driver White Paper* on the Altera web site (**www.altera.com**).

PLL Reconfiguration

The phase-locked loops (PLLs) in the Stratix II device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.

See the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information on Stratix II PLLs.

Temperature Sensing Diode (TSD)

Stratix II devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device. These devices steer bias current through the Stratix II diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus sign). The external device's output represents the junction temperature of the Stratix II device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix II device to connect to the external temperature-sensing device, as shown in Figure 3–1. The temperature sensing diode is a passive element and therefore can be used before the Stratix II device is powered.

Document Revision History

Table 4–1 shows the revision history for this chapter.

Table 4–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007, v3.2	Moved the Document Revision History section to the end of the chapter.	—
April 2006, v3.1	• Updated "Signal Pins Do Not Drive the VCCIO, VCCINT or VCCPD Power Supplies" section.	• Updated hot socketing AC specification.
May 2005, v3.0	• Updated "Signal Pins Do Not Drive the VCCIO, VCCINT or VCCPD Power Supplies" section. • Removed information on ESD protection.	—
January 2005, v2.1	Updated input rise and fall time.	—
January 2005, v2.0	Updated the "Hot Socketing Feature Implementation in Stratix II Devices", "ESD Protection", and "Power-On Reset Circuitry" sections.	—
July 2004, v1.1	• Updated all tables. • Added tables.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

Figure 5–1. Receiver Input Waveforms for Differential I/O Standards

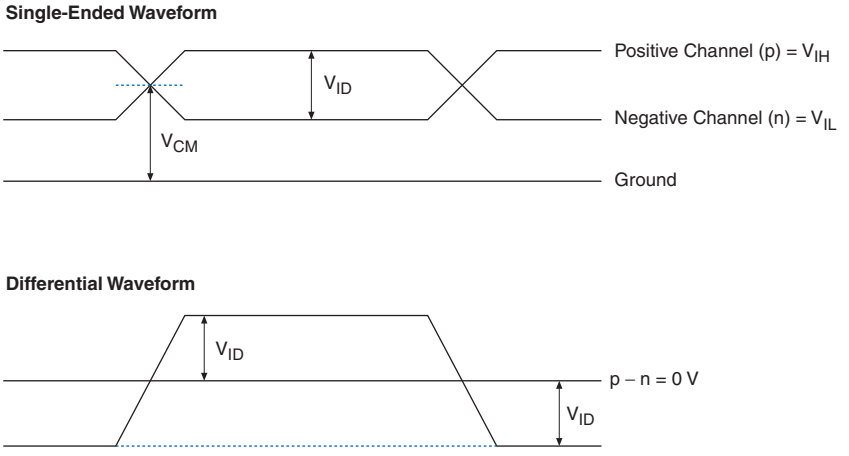
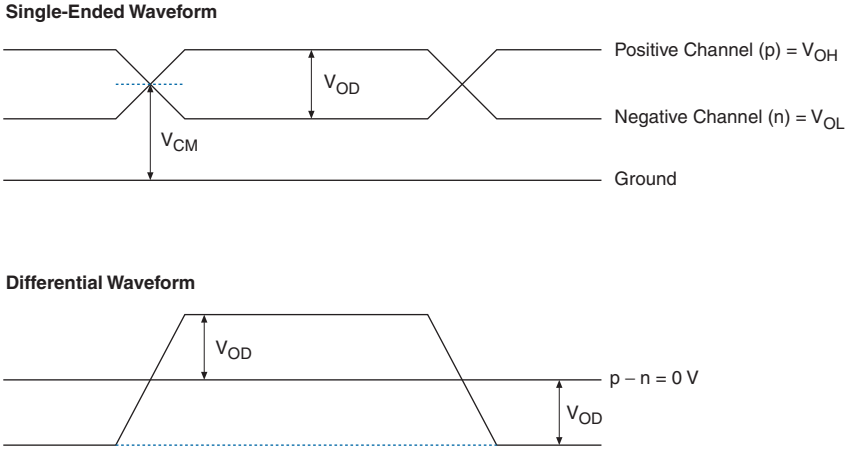


Figure 5–2. Transmitter Output Waveforms for Differential I/O Standards

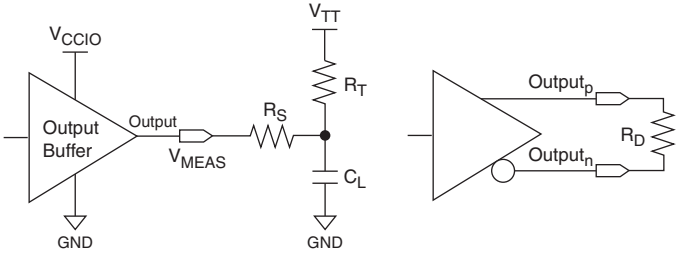


4. Record the time to V_{MEAS}.

5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-output) of the PCB trace.

The Quartus II software reports the timing with the conditions shown in Table 5–34 using the above equation. Figure 5–4 shows the model of the circuit that is represented by the output timing of the Quartus II software.

Figure 5–4. Output Delay Timing Reporting Setup Modeled by Quartus II



Notes to Figure 5–4:

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.

(2) V_{CCPD} is 3.085 V unless otherwise specified.

(3) V_{CCINT} is 1.12 V unless otherwise specified.

Figures 5–5 and 5–6 show the measurement setup for output disable and output enable timing.

Table 5–34. Output Timing Measurement Methodology for Output Pins *Notes (1), (2), (3)*

I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
LVTTL *(4)*				3.135		0	1.5675
LVCMOS *(4)*				3.135		0	1.5675
2.5 V *(4)*				2.375		0	1.1875
1.8 V *(4)*				1.710		0	0.855
1.5 V *(4)*				1.425		0	0.7125
PCI *(5)*				2.970		10	1.485
PCI-X *(5)*				2.970		10	1.485
SSTL-2 Class I	25		50	2.325	1.123	0	1.1625
SSTL-2 Class II	25		25	2.325	1.123	0	1.1625
SSTL-18 Class I	25		50	1.660	0.790	0	0.83
SSTL-18 Class II	25		25	1.660	0.790	0	0.83
1.8-V HSTL Class I	50		50	1.660	0.790	0	0.83
1.8-V HSTL Class II	25		25	1.660	0.790	0	0.83
1.5-V HSTL Class I	50		50	1.375	0.648	0	0.6875
1.5-V HSTL Class II			25	1.375	0.648	0	0.6875
1.2-V HSTL with OCT	50			1.140		0	0.570
Differential SSTL-2 Class I	50		50	2.325	1.123	0	1.1625
Differential SSTL-2 Class II	25		25	2.325	1.123	0	1.1625
Differential SSTL-18 Class I	50		50	1.660	0.790	0	0.83
Differential SSTL-18 Class II	25		25	1.660	0.790	0	0.83
1.5-V Differential HSTL Class I	50		50	1.375	0.648	0	0.6875
1.5-V Differential HSTL Class II			25	1.375	0.648	0	0.6875
1.8-V Differential HSTL Class I	50		50	1.660	0.790	0	0.83
1.8-V Differential HSTL Class II	25		25	1.660	0.790	0	0.83
LVDS		100		2.325		0	1.1625
HyperTransport		100		2.325		0	1.1625
LVPECL		100		3.135		0	1.5675

Notes to Table 5–34:

(1) Input measurement point at internal node is $0.5 \times V_{CCINT}$.

(2) Output measuring point for V_{MEAS} at buffer output is $0.5 \times V_{CCIO}$.

(3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.

(4) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple

(5) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V

Table 5–39. DSP Block Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade *(1)*		-3 Speed Grade *(2)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min *(3)*	Max	Min *(3)*	Max	Min *(4)*	Max	Min *(3)*	Max	
t_{SU}	Input, pipeline, and output register setup time before clock	50		52		57 57		67		ps
t_{H}	Input, pipeline, and output register hold time after clock	180		189		206 206		241		ps
t_{CO}	Input, pipeline, and output register clock-to-output delay	0	0	0	0	0 0	0	0	0	ps
$t_{INREG2PIPE9}$	Input register to DSP block pipeline register in 9 × 9-bit mode	1,312	2,030	1,312	2,030	1,250 1,312	2,334	1,312	2,720	ps
$t_{INREG2PIPE18}$	Input register to DSP block pipeline register in 18 × 18-bit mode	1,302	2,010	1,302	2,110	1,240 1,302	2,311	1,302	2,693	ps
$t_{INREG2PIPE36}$	Input register to DSP block pipeline register in 36 × 36-bit mode	1,302	2,010	1,302	2,110	1,240 1,302	2,311	1,302	2,693	ps
$t_{PIPE2OUTREG2ADD}$	DSP block pipeline register to output register delay in two-multipliers adder mode	924	1,450	924	1,522	880 924	1,667	924	1,943	ps
$t_{PIPE2OUTREG4ADD}$	DSP block pipeline register to output register delay in four-multipliers adder mode	1,134	1,850	1,134	1,942	1,080 1,134	2,127	1,134	2,479	ps
t_{PD9}	Combinational input to output delay for 9 × 9	2,100	2,880	2,100	3,024	2,000 2,100	3,312	2,100	3,859	ps
t_{PD18}	Combinational input to output delay for 18 × 18	2,110	2,990	2,110	3,139	2,010 2,110	3,438	2,110	4,006	ps
t_{PD36}	Combinational input to output delay for 36 × 36	2,939	4,450	2,939	4,672	2,800 2,939	5,117	2,939	5,962	ps
t_{CLR}	Minimum clear pulse width	2,212		2,322		2,543 2,543		2,964		ps

Table 5–42. M-RAM Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min (4)	Max	Min (4)	Max	Min (5)	Max	Min (4)	Max	
$t_{MEGACLKH}$	Minimum clock high time	1,250		1,312		1,437 1,437		1,675		ps
$t_{MEGACLR}$	Minimum clear pulse width	144		151		165 165		192		ps

Notes to Table 5–42:

(1) F_{MAX} of M-RAM Block obtained using the Quartus II software does not necessarily equal to 1/TMEGARC.
(2) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(3) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.
(4) For the -3 and -5 speed grades, the minimum timing is for the commercial temperature grade. Only -4 speed grade devices offer the industrial temperature grade.
(5) For the -4 speed grade, the first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.

Stratix II Clock Timing Parameters

See Tables 5–43 through 5–67 for Stratix II clock timing parameters.

Table 5–43. Stratix II Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL `inclk` pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL `inclk` pad to I/O output register

EP2S90 Clock Timing Parameters

Tables 5–56 through 5–59 show the maximum clock timing parameters for EP2S90 devices.

Table 5–56. EP2S90 Column Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.768	1.850	3.033	3.473	4.040	ns
t_{COUT}	1.611	1.685	2.791	3.195	3.716	ns
t_{PLLCIN}	-0.127	-0.117	0.125	0.129	0.144	ns
$t_{PLLCOUT}$	-0.284	-0.282	-0.117	-0.149	-0.18	ns

Table 5–57. EP2S90 Column Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.783	1.868	3.058	3.502	4.070	ns
t_{COUT}	1.626	1.703	2.816	3.224	3.746	ns
t_{PLLCIN}	-0.137	-0.127	0.115	0.119	0.134	ns
$t_{PLLCOUT}$	-0.294	-0.292	-0.127	-0.159	-0.19	ns

Table 5–58. EP2S90 Row Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.566	1.638	2.731	3.124	3.632	ns
t_{COUT}	1.571	1.643	2.727	3.120	3.627	ns
t_{PLLCIN}	-0.326	-0.326	-0.178	-0.218	-0.264	ns
$t_{PLLCOUT}$	-0.321	-0.321	-0.182	-0.222	-0.269	ns

Table 5–59. EP2S90 Row Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.585	1.658	2.757	3.154	3.665	ns
t_{COUT}	1.590	1.663	2.753	3.150	3.660	ns
t_{PLLCIN}	-0.341	-0.341	-0.193	-0.235	-0.278	ns
$t_{PLLCOUT}$	-0.336	-0.336	-0.197	-0.239	-0.283	ns

EP2S130 Clock Timing Parameters

Tables 5–60 through 5–63 show the maximum clock timing parameters for EP2S130 devices.

Table 5–60. EP2S130 Column Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.889	1.981	3.405	3.722	4.326	ns
t_{COUT}	1.732	1.816	3.151	3.444	4.002	ns
t_{PLLCIN}	0.105	0.106	0.226	0.242	0.277	ns
$t_{PLLCOUT}$	-0.052	-0.059	-0.028	-0.036	-0.047	ns

Table 5–61. EP2S130 Column Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.907	1.998	3.420	3.740	4.348	ns
t_{COUT}	1.750	1.833	3.166	3.462	4.024	ns
t_{PLLCIN}	0.134	0.136	0.276	0.296	0.338	ns
$t_{PLLCOUT}$	-0.023	-0.029	0.022	0.018	0.014	ns

I/O Delays

See Tables 5–72 through 5–76 for I/O delays.

Table 5–72. I/O Delay Parameters

Symbol	Parameter
t_{DIP}	Delay from I/O datain to output pad
t_{OP}	Delay from I/O output register to output pad
t_{PCOUT}	Delay from input pad to I/O dataout to core
t_{PI}	Delay from input pad to I/O input register

Table 5–73. Stratix II I/O Input Delay for Column Pins (Part 1 of 3)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
LVTTL	t_{PI}	674	707	1223	1282	1405	1637	ps
	t_{PCOUT}	408	428	787	825	904	1054	ps
2.5 V	t_{PI}	684	717	1210	1269	1390	1619	ps
	t_{PCOUT}	418	438	774	812	889	1036	ps
1.8 V	t_{PI}	747	783	1366	1433	1570	1829	ps
	t_{PCOUT}	481	504	930	976	1069	1246	ps
1.5 V	t_{PI}	749	786	1436	1506	1650	1922	ps
	t_{PCOUT}	483	507	1000	1049	1149	1339	ps
LVCMOS	t_{PI}	674	707	1223	1282	1405	1637	ps
	t_{PCOUT}	408	428	787	825	904	1054	ps
SSTL-2 Class I	t_{PI}	507	530	818	857	939	1094	ps
	t_{PCOUT}	241	251	382	400	438	511	ps
SSTL-2 Class II	t_{PI}	507	530	818	857	939	1094	ps
	t_{PCOUT}	241	251	382	400	438	511	ps
SSTL-18 Class I	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
SSTL-18 Class II	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.5-V HSTL Class I	t_{PI}	560	587	993	1041	1141	1329	ps
	t_{PCOUT}	294	308	557	584	640	746	ps

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 3 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
1.8 V	2 mA	t_{OP}	1042	1093	2904	3048	3338	3472	ps
		t_{DIP}	1062	1115	2970	3118	3414	3562	ps
	4 mA	t_{OP}	1047	1098	2248	2359	2584	2698	ps
		t_{DIP}	1067	1120	2314	2429	2660	2788	ps
	6 mA	t_{OP}	974	1022	2024	2124	2326	2434	ps
		t_{DIP}	994	1044	2090	2194	2402	2524	ps
	8 mA	t_{OP}	976	1024	1947	2043	2238	2343	ps
		t_{DIP}	996	1046	2013	2113	2314	2433	ps
	10 mA	t_{OP}	933	978	1882	1975	2163	2266	ps
		t_{DIP}	953	1000	1948	2045	2239	2356	ps
	12 mA (1)	t_{OP}	934	979	1833	1923	2107	2209	ps
		t_{DIP}	954	1001	1899	1993	2183	2299	ps
1.5 V	2 mA	t_{OP}	1023	1073	2505	2629	2879	3002	ps
		t_{DIP}	1043	1095	2571	2699	2955	3092	ps
	4 mA	t_{OP}	963	1009	2023	2123	2325	2433	ps
		t_{DIP}	983	1031	2089	2193	2401	2523	ps
	6 mA	t_{OP}	966	1012	1923	2018	2210	2315	ps
		t_{DIP}	986	1034	1989	2088	2286	2405	ps
	8 mA (1)	t_{OP}	926	971	1878	1970	2158	2262	ps
		t_{DIP}	946	993	1944	2040	2234	2352	ps
SSTL-2 Class I	8 mA	t_{OP}	913	957	1715	1799	1971	2041	ps
		t_{DIP}	933	979	1781	1869	2047	2131	ps
	12 mA (1)	t_{OP}	896	940	1672	1754	1921	1991	ps
		t_{DIP}	916	962	1738	1824	1997	2081	ps
SSTL-2 Class II	16 mA	t_{OP}	876	918	1609	1688	1849	1918	ps
		t_{DIP}	896	940	1675	1758	1925	2008	ps
	20 mA	t_{OP}	877	919	1598	1676	1836	1905	ps
		t_{DIP}	897	941	1664	1746	1912	1995	ps
	24 mA (1)	t_{OP}	872	915	1596	1674	1834	1903	ps
		t_{DIP}	892	937	1662	1744	1910	1993	ps

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 2 of 5) *Note (1)*

I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
SSTL-18 Class I	4 mA	200	150	150	200	150	150	200	150	150
	6 mA	350	250	200	350	250	200	350	250	200
	8 mA	450	300	300	450	300	300	450	300	300
	10 mA	500	400	400	500	400	400	500	400	400
	12 mA	700	550	400	-	-	-	650	550	400
SSTL-18 Class II	8 mA	200	200	150	-	-	-	200	200	150
	16 mA	400	350	350	-	-	-	400	350	350
	18 mA	450	400	400	-	-	-	450	400	400
	20 mA	550	500	450	-	-	-	550	500	450
1.8-V HSTL Class I	4 mA	300	300	300	300	300	300	300	300	300
	6 mA	500	450	450	500	450	450	500	450	450
	8 mA	650	600	600	650	600	600	650	600	600
	10 mA	700	650	600	700	650	600	700	650	600
	12 mA	700	700	650	700	700	650	700	700	650
1.8-V HSTL Class II	16 mA	500	500	450	-	-	-	500	500	450
	18 mA	550	500	500	-	-	-	550	500	500
	20 mA	650	550	550	-	-	-	550	550	550
1.5-V HSTL Class I	4 mA	350	300	300	350	300	300	350	300	300
	6 mA	500	500	450	500	500	450	500	500	450
	8 mA	700	650	600	700	650	600	700	650	600
	10 mA	700	700	650	-	-	-	700	700	650
	12 mA	700	700	700	-	-	-	700	700	700
1.5-V HSTL Class II	16 mA	600	600	550	-	-	-	600	600	550
	18 mA	650	600	600	-	-	-	650	600	600
	20 mA	700	650	600	-	-	-	700	650	600
Differential SSTL-2 Class I *(3)*	8 mA	400	300	300	400	300	300	400	300	300
	12 mA	400	400	350	400	400	350	400	400	350
Differential SSTL-2 Class II *(3)*	16 mA	350	350	300	350	350	300	350	350	300
	20 mA	400	350	350	350	350	297	400	350	350
	24 mA	400	400	350	-	-	-	400	400	350