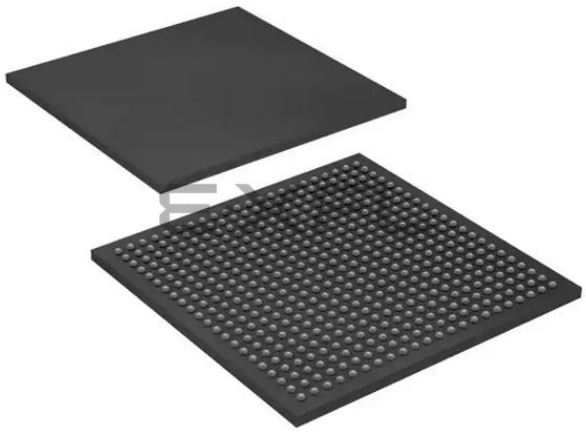

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	780
Number of Logic Elements/Cells	15600
Total RAM Bits	419328
Number of I/O	342
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s15f484c4n

Contents

Section I. Stratix II Device Family Data Sheet

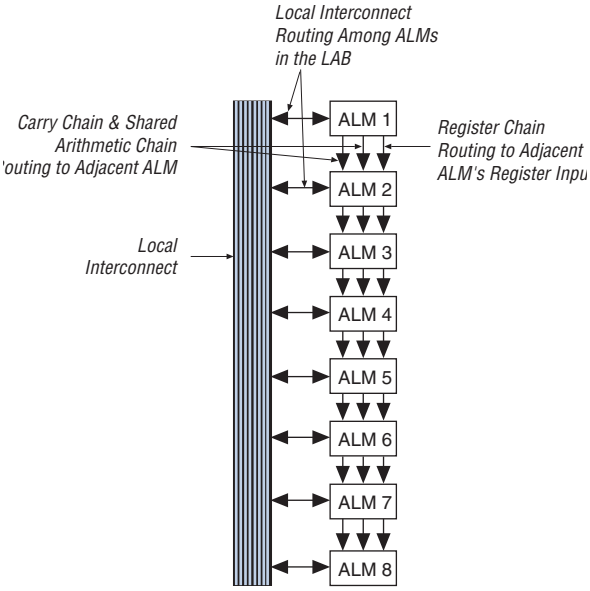
This section provides the data sheet specifications for Stratix® II devices. This section contains feature definitions of the internal architecture, configuration and JTAG boundary-scan testing information, DC operating conditions, AC timing parameters, a reference to power consumption, and ordering information for Stratix II devices.

This section contains the following chapters:

Revision History

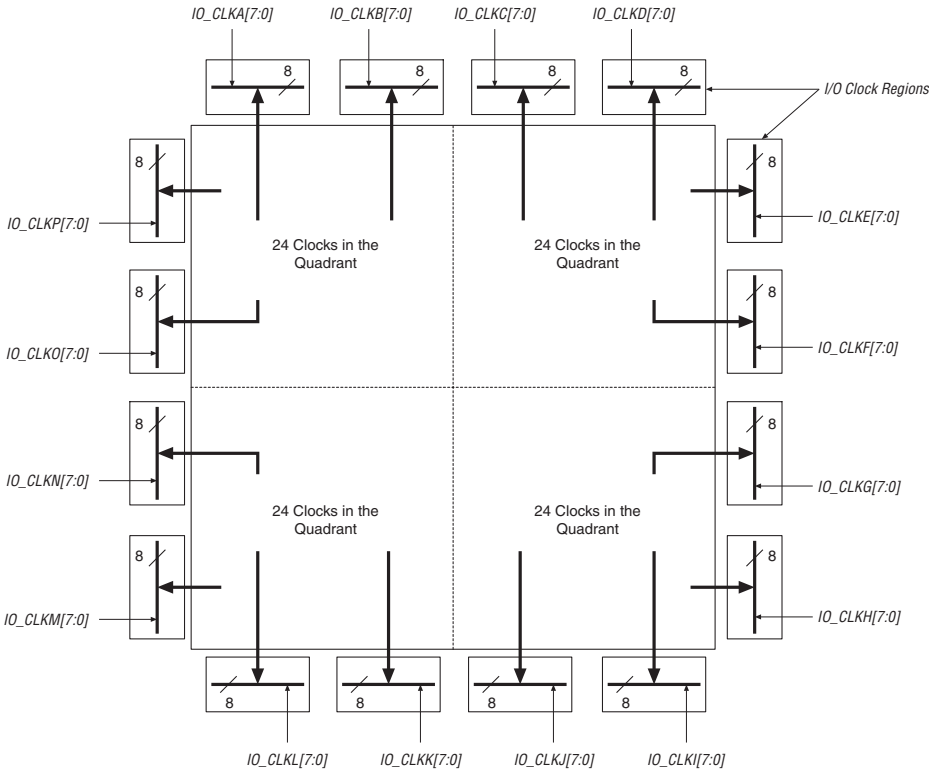
Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

Figure 2–17. Shared Arithmetic Chain, Carry Chain & Register Chain Interconnects



The C4 interconnects span four LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–18 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2–36. EP2S60, EP2S90, EP2S130 & EP2S180 Device I/O Clock Groups



You can use the Quartus II software to control whether a clock input pin drives either a global, regional, or dual-regional clock network. The Quartus II software automatically selects the clocking resources if not specified.

Clock Control Block

Each global clock, regional clock, and PLL external clock output has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable/disable)

Table 2–20. Supported TDO/TDI Voltage Combinations (Part 2 of 2)

Device	TDI Input Buffer Power	Stratix II TDO V_{CCIO} Voltage Level in I/O Bank 4				
		V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V	V_{CCIO} = 1.2 V
Non-Stratix II	VCC = 3.3 V	✓ (1)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 2.5 V	✓ (1), (4)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 1.8 V	✓ (1), (4)	✓ (2), (5)	✓	Level shifter required	Level shifter required
	VCC = 1.5 V	✓ (1), (4)	✓ (2), (5)	✓ (6)	✓	✓

Notes to Table 2–20:

(1) The TDO output buffer meets V_{OH} (MIN) = 2.4 V.
(2) The TDO output buffer meets V_{OH} (MIN) = 2.0 V.
(3) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.
(4) Input buffer must be 3.3-V tolerant.
(5) Input buffer must be 2.5-V tolerant.
(6) Input buffer must be 1.8-V tolerant.

High-Speed Differential I/O with DPA Support

Stratix II devices contain dedicated circuitry for supporting differential standards at speeds up to 1 Gbps. The LVDS and HyperTransport differential I/O standards are supported in the Stratix II device. In addition, the LVPECL I/O standard is supported on input and output clock pins on the top and bottom I/O banks.

The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- Parallel RapidIO
- HyperTransport technology

There are four dedicated high-speed PLLs in the EP2S15 to EP2S30 devices and eight dedicated high-speed PLLs in the EP2S60 to EP2S180 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Tables 2–21 through 2–26 show the number of channels that each fast PLL can clock in each of the Stratix II devices. In Tables 2–21 through 2–26 the first row for each transmitter or receiver provides the number of channels driven directly by the PLL. The second row below it shows the maximum channels a PLL can drive if cross bank channels are used from the adjacent center PLL. For example, in the 484-pin FineLine BGA EP2S15

3. Configuration & Testing

SII51003-4.2

IEEE Std. 1149.1 JTAG Boundary-Scan Support

All Stratix® II devices provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1. JTAG boundary-scan testing can be performed either before or after, but not during configuration. Stratix II devices can also use the JTAG port for configuration with the Quartus® II software or hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**).

Stratix II devices support IOE I/O standard setting reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode through the `CONFIG_IO` instruction. You can use this capability for JTAG testing before configuration when some of the Stratix II pins drive or receive from other devices on the board using voltage-referenced standards. Because the Stratix II device may not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming those I/O standards via JTAG allows you to fully test I/O connections to other devices.

A device operating in JTAG mode uses four required pins, `TDI`,`TDO`, `TMS`, and `TCK`, and one optional pin, `TRST`. The `TCK` pin has an internal weak pull-down resistor, while the `TDI`,`TMS` and `TRST` pins have weak internal pull-ups. The JTAG input pins are powered by the 3.3-V `VCCPD` pins. The TDO output pin is powered by the V_{CCIO} power supply of bank 4.

Stratix II devices also use the JTAG port to monitor the logic operation of the device with the SignalTap® II embedded logic analyzer. Stratix II devices support the JTAG instructions shown in Table 3–1.

Stratix II, Stratix, Cyclone® II, and Cyclone devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix II, Stratix, Cyclone II, or Cyclone devices are in the 18th of further position, they fail configuration. This does not affect SignalTap II.

The Stratix II device instruction register length is 10 bits and the `USERCODE` register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device `IDCODE` information for Stratix II devices.

The Quartus II software has an Auto Usercode feature where you can choose to use the checksum value of a programming file as the JTAG user code. If selected, the checksum is automatically loaded to the USERCODE register. Turn on the **Auto Usercode** option by clicking **Device & Pin Options**, then **General,** in the **Settings** dialog box (Assignments menu).

Table 3–2. Stratix II Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP2S15	1,140
EP2S30	1,692
EP2S60	2,196
EP2S90	2,748
EP2S130	3,420
EP2S180	3,948

Table 3–3. 32-Bit Stratix II Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP2S15	0000	0010 0000 1001 0001	000 0110 1110	1
EP2S30	0000	0010 0000 1001 0010	000 0110 1110	1
EP2S60	0001	0010 0000 1001 0011	000 0110 1110	1
EP2S90	0000	0010 0000 1001 0100	000 0110 1110	1
EP2S130	0000	0010 0000 1001 0101	000 0110 1110	1
EP2S180	0000	0010 0000 1001 0110	000 0110 1110	1

Notes to Table 3–3:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Stratix, Stratix II, Cyclone, and Cyclone II devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix, Stratix II, Cyclone, and Cyclone II devices are in the 18th or after they fail configuration. This does not affect SignalTap II.

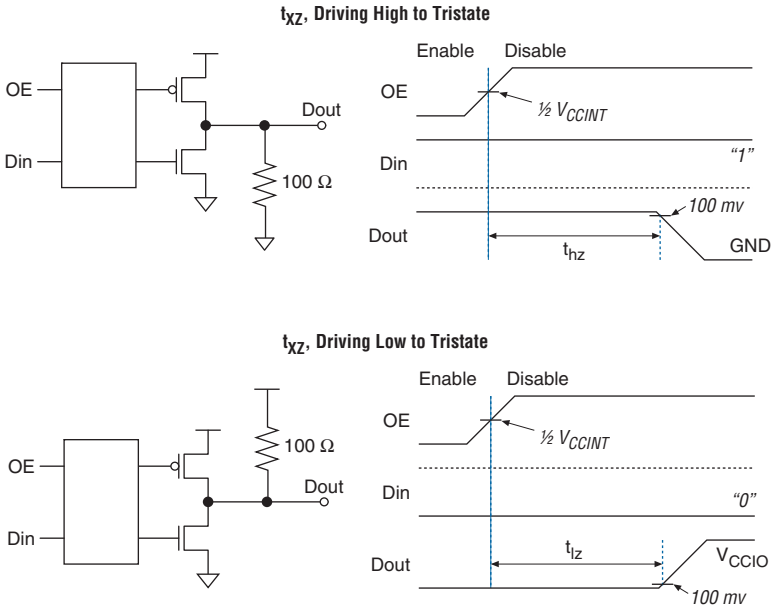
Document Revision History

Table 4–1 shows the revision history for this chapter.

Table 4–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007, v3.2	Moved the Document Revision History section to the end of the chapter.	—
April 2006, v3.1	• Updated "Signal Pins Do Not Drive the VCCIO, VCCINT or VCCPD Power Supplies" section.	• Updated hot socketing AC specification.
May 2005, v3.0	• Updated "Signal Pins Do Not Drive the VCCIO, VCCINT or VCCPD Power Supplies" section. • Removed information on ESD protection.	—
January 2005, v2.1	Updated input rise and fall time.	—
January 2005, v2.0	Updated the "Hot Socketing Feature Implementation in Stratix II Devices", "ESD Protection", and "Power-On Reset Circuitry" sections.	—
July 2004, v1.1	• Updated all tables. • Added tables.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

Figure 5–5. Measurement Setup for t_{xz} *Note (1)*



Note to Figure 5–5:
(1) V_{CCINT} is 1.12 V for this measurement.

Table 5–42. M-RAM Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min (4)	Max	Min (4)	Max	Min (5)	Max	Min (4)	Max	
$t_{MEGACLKH}$	Minimum clock high time	1,250		1,312		1,437 1,437		1,675		ps
$t_{MEGACLR}$	Minimum clear pulse width	144		151		165 165		192		ps

Notes to Table 5–42:

(1) F_{MAX} of M-RAM Block obtained using the Quartus II software does not necessarily equal to 1/TMEGARC.
(2) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(3) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.
(4) For the -3 and -5 speed grades, the minimum timing is for the commercial temperature grade. Only -4 speed grade devices offer the industrial temperature grade.
(5) For the -4 speed grade, the first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.

Stratix II Clock Timing Parameters

See Tables 5–43 through 5–67 for Stratix II clock timing parameters.

Table 5–43. Stratix II Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL `inclk` pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL `inclk` pad to I/O output register

Table 5–74. Stratix II I/O Input Delay for Row Pins (Part 2 of 2)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (1)	-3 Speed Grade (2)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
1.5-V HSTL Class II	t_{PI}	602	631	1056	1107	1212	1413	ps
	t_{PCOUT}	278	292	529	555	608	708	ps
1.8-V HSTL Class I	t_{PI}	577	605	960	1006	1101	1285	ps
	t_{PCOUT}	253	266	433	454	497	580	ps
1.8-V HSTL Class II	t_{PI}	577	605	960	1006	1101	1285	ps
	t_{PCOUT}	253	266	433	454	497	580	ps
LVDS	t_{PI}	515	540	948	994	1088	1269	ps
	t_{PCOUT}	191	201	421	442	484	564	ps
HyperTransport	t_{PI}	515	540	948	994	1088	1269	ps
	t_{PCOUT}	191	201	421	442	484	564	ps

Notes for Table 5–74:
(1) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(2) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 1 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
LVTTL	4 mA	t_{OP}	1178	1236	2351	2467	2702	2820	ps
		t_{DIP}	1198	1258	2417	2537	2778	2910	ps
	8 mA	t_{OP}	1041	1091	2036	2136	2340	2448	ps
		t_{DIP}	1061	1113	2102	2206	2416	2538	ps
	12 mA	t_{OP}	976	1024	2036	2136	2340	2448	ps
		t_{DIP}	996	1046	2102	2206	2416	2538	ps
	16 mA	t_{OP}	951	998	1893	1986	2176	2279	ps
		t_{DIP}	971	1020	1959	2056	2252	2369	ps
	20 mA	t_{OP}	931	976	1787	1875	2054	2154	ps
		t_{DIP}	951	998	1853	1945	2130	2244	ps
	24 mA (1)	t_{OP}	924	969	1788	1876	2055	2156	ps
		t_{DIP}	944	991	1854	1946	2131	2246	ps

Table 5–80. Maximum DCD for Non-DDIO Output on Row I/O Pins (Part 2 of 2) *Note (1)*

Row I/O Output Standard	Maximum DCD for Non-DDIO Output		
	-3 Devices	-4 & -5 Devices	Unit
1.8 V	180	180	ps
1.5-V LVCMOS	165	195	ps
SSTL-2 Class I	115	145	ps
SSTL-2 Class II	95	125	ps
SSTL-18 Class I	55	85	ps
1.8-V HSTL Class I	80	100	ps
1.5-V HSTL Class I	85	115	ps
LVDS/ HyperTransport technology	55	80	ps

Note to Table 5–80:
(1) The DCD specification is based on a no logic array noise condition.

Here is an example for calculating the DCD as a percentage for a non-DDIO output on a row I/O on a -3 device:

If the non-DDIO output I/O standard is SSTL-2 Class II, the maximum DCD is 95 ps (see Table 5–80). If the clock frequency is 267 MHz, the clock period T is:

T = 1/ f = 1 / 267 MHz = 3.745 ns = 3745 ps

To calculate the DCD as a percentage:

(T/2 – DCD) / T = (3745ps/2 – 95ps) / 3745ps = 47.5% (for low boundary)

(T/2 + DCD) / T = (3745ps/2 + 95ps) / 3745ps = 52.5% (for high boundary)

Table 5–85. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -4 & -5 Devices (Part 2 of 2) *Notes (1), (2)*

DDIO Column Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)				Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	
SSTL-18 Class I	335	390	65	65	ps
SSTL-18 Class II	320	375	70	80	ps
1.8-V HSTL Class I	330	385	60	70	ps
1.8-V HSTL Class II	330	385	60	70	ps
1.5-V HSTL Class I	330	390	60	70	ps
1.5-V HSTL Class II	330	360	90	100	ps
1.2-V HSTL	420	470	155	165	ps
LVPECL	180	180	180	180	ps

Notes to Table 5–85:
(1) Table 5–85 assumes the input clock has zero DCD.
(2) The DCD specification is based on a no logic array noise condition.

Table 5–86. Maximum DCD for DDIO Output on Row I/O Pins with PLL in the Clock Path (Part 1 of 2) *Note (1)*

Row DDIO Output I/O Standard	Maximum DCD (PLL Output Clock Feeding DDIO Clock Port)		Unit
	-3 Device	-4 & -5 Device	
3.3-V LVTTL	110	105	ps
3.3-V LVCMOS	65	75	ps
2.5V	75	90	ps
1.8V	85	100	ps
1.5-V LVCMOS	105	100	ps
SSTL-2 Class I	65	75	ps
SSTL-2 Class II	60	70	ps
SSTL-18 Class I	50	65	ps
1.8-V HSTL Class I	50	70	ps
1.5-V HSTL Class I	55	70	ps

High-Speed I/O Specifications

Table 5–88 provides high-speed timing specifications definitions.

Table 5–88. High-Speed Timing Specifications & Definitions

High-Speed Timing Specifications	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
J	Deserialization factor (width of parallel data bus).
W	PLL multiplication factor.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter	Peak-to-peak input jitter on high-speed PLLs.
Output jitter	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Table 5–89 shows the high-speed I/O timing specifications for -3 speed grade Stratix II devices.

Table 5–89. High-Speed I/O Specifications for -3 Speed Grade (Part 1 of 2) *Notes (1), (2)*

Symbol	Conditions	-3 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (clock frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*	16		520	MHz
	W = 1 (SERDES bypass, LVDS only)	16		500	MHz
	W = 1 (SERDES used, LVDS only)	150		717	MHz

Table 5–90 shows the high-speed I/O timing specifications for -4 speed grade Stratix II devices.

Table 5–90. High-Speed I/O Specifications for -4 Speed Grade *Notes (1), (2)*

Symbol	Conditions	-4 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (clock frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*	16		520	MHz
	W = 1 (SERDES bypass, LVDS only)	16		500	MHz
	W = 1 (SERDES used, LVDS only)	150		717	MHz
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150		1,040	Mbps
	J = 2 (LVDS, HyperTransport technology)	*(4)*		760	Mbps
	J = 1 (LVDS only)	*(4)*		500	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150		1,040	Mbps
TCCS	All differential standards	-		200	ps
SW	All differential standards	330		-	ps
Output jitter				190	ps
Output t_{RISE}	All differential I/O standards			160	ps
Output t_{FALL}	All differential I/O standards			180	ps
t_{DUTY}		45	50	55	%
DPA run length				6,400	UI
DPA jitter tolerance	Data channel peak-to-peak jitter	0.44			UI
DPA lock time	**Standard** / **Training Pattern** / **Transition Density**				Number of repetitions
	SPI-4 / 0000000000 1111111111 / 10%	256			
	Parallel Rapid I/O / 00001111 / 25%	256			
	Parallel Rapid I/O / 10010000 / 50%	256			
	Miscellaneous / 10101010 / 100%	256			
	Miscellaneous / 01010101 /	256			

Notes to Table 5–90:

(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤ input clock frequency × W ≤ 1,040.

(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.

Table 5–91 shows the high-speed I/O timing specifications for -5 speed grade Stratix II devices.

Table 5–91. High-Speed I/O Specifications for -5 Speed Grade *Notes (1), (2)*

Symbol	Conditions			-5 Speed Grade			Unit
				Min	Typ	Max	
f_{HSCLK} (clock frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*			16		420	MHz
	W = 1 (SERDES bypass, LVDS only)			16		500	MHz
	W = 1 (SERDES used, LVDS only)			150		640	MHz
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		840	Mbps
	J = 2 (LVDS, HyperTransport technology)			*(4)*		700	Mbps
	J = 1 (LVDS only)			*(4)*		500	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		840	Mbps
TCCS	All differential I/O standards			-		200	ps
SW	All differential I/O standards			440		-	ps
Output jitter						190	ps
Output t_{RISE}	All differential I/O standards					290	ps
Output t_{FALL}	All differential I/O standards					290	ps
t_{DUTY}				45	50	55	%
DPA run length						6,400	UI
DPA jitter tolerance	Data channel peak-to-peak jitter			0.44			UI
DPA lock time	**Standard**	**Training Pattern**	**Transition Density**				Number of repetitions
	SPI-4	0000000000 1111111111	10%	256			
	Parallel Rapid I/O	00001111	25%	256			
		10010000	50%	256			
	Miscellaneous	10101010	100%	256			
		01010101		256			

Notes to Table 5–91:

(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤ input clock frequency × W ≤ 1,040.

(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.

PLL Timing Specifications

Tables 5–92 and 5–93 describe the Stratix II PLL specifications when operating in both the commercial junction temperature range (0 to 85 °C) and the industrial junction temperature range (–40 to 100 °C).

Table 5–92. Enhanced PLL Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	2		500	MHz
f_{INPFD}	Input frequency to the PFD	2		420	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$f_{EINDUTY}$	External feedback input clock duty cycle	40		60	%
$t_{INJITTER}$	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth ≤ 0.85 MHz		0.5		ns (p-p)
	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth > 0.85 MHz		1.0		ns (p-p)
$t_{OUTJITTER}$	Dedicated clock output period jitter			250 ps for ≥ 100 MHz `outclk` 25 mUI for < 100 MHz `outclk`	ps or mUI (p-p)
t_{FCOMP}	External feedback compensation time			10	ns
f_{OUT}	Output frequency for internal global or regional clock	1.5 *(2)*		550.0	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%).	45	50	55	%
$f_{SCANCLK}$	Scanclk frequency			100	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for enhanced PLLs		$174/f_{SCANCLK}$		ns
f_{OUT_EXT}	PLL external clock output frequency	1.5 *(2)*		550.0 *(1)*	MHz

Table 5–93. Fast PLL Specifications

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (for -3 and -4 speed grade devices)	16.08		717	MHz
	Input clock frequency (for -5 speed grade devices)	16.08		640	MHz
f_{INPFD}	Input frequency to the PFD	16.08		500	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$t_{INJITTER}$	Input clock jitter tolerance in terms of period jitter. Bandwidth ≤ 2 MHz		0.5		ns (p-p)
	Input clock jitter tolerance in terms of period jitter. Bandwidth > 2 MHz		1.0		ns (p-p)
f_{VCO}	Upper VCO frequency range for –3 and –4 speed grades	300		1,040	MHz
	Upper VCO frequency range for –5 speed grades	300		840	MHz
	Lower VCO frequency range for –3 and –4 speed grades	150		520	MHz
	Lower VCO frequency range for –5 speed grades	150		420	MHz
f_{OUT}	PLL output frequency to GCLK or RCLK	4.6875		550	MHz
	PLL output frequency to LVDS or DPA clock	150		1,040	MHz
f_{OUT_IO}	PLL clock output frequency to regular I/O pin	4.6875		*(1)*	MHz
$f_{SCANCLK}$	Scanclk frequency			100	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for fast PLLs		$75/f_{SCANCLK}$		ns
f_{CLBW}	PLL closed-loop bandwidth	1.16	5.00	28.00	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of the device configuration		0.03	1.00	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift			±15	ps
t_{ARESET}	Minimum pulse width on areset signal.	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scandone goes high.	500			ns

Note to Table 5–93:
(1) Limited by I/O f_{MAX}. See Table 5–77 on page 5–67 for the maximum.

Table 5–103. Document Revision History (Part 2 of 3)

Date and Document Version	Changes Made	Summary of Changes
August, 2006, v4.2	Updated Table 5–73, Table 5–75, Table 5–77, Table 5–78, Table 5–79, Table 5–81, Table 5–85, and Table 5–87.	—
April 2006, v4.1	• Updated Table 5–3. • Updated Table 5–11. • Updated Figures 5–8 and 5–9. • Added parallel on-chip termination information to "On-Chip Termination Specifications" section. • Updated Tables 5–28, 5–30,5–31, and 5–34. • Updated Table 5–78, Tables 5–81 through 5–90, and Tables 5–92, 5–93, and 5–98. • Updated "PLL Timing Specifications" section. • Updated "External Memory Interface Specifications" section. • Added Tables 5–95 and 5–101. • Updated "JTAG Timing Specifications" section, including Figure 5–10 and Table 5–102.	• Changed 0.2 MHz to 2 MHz in Table 5–93. • Added new spec for half period jitter (Table 5–101). • Added support for PLL clock switchover for industrial temperature range. • Changed f_{INPFD} (min) spec from 4 MHz to 2 MHz in Table 5–92. • Fixed typo in $t_{OUTJITTER}$ specification in Table 5–92. • Updated V_{DIF} AC & DC max specifications in Table 5–28. • Updated minimum values for t_{JCH}, t_{JCL}, and t_{JPSU} in Table 5–102. • Update maximum values for t_{JPCO}, t_{JPZX}, and t_{JPXZ} in Table 5–102.
December 2005, v4.0	• Updated "External Memory Interface Specifications" section. • Updated timing numbers throughout chapter.	—
July 2005, v3.1	• Updated HyperTransport technology information in Table 5–13. • Updated "Timing Model" section. • Updated "PLL Timing Specifications" section. • Updated "External Memory Interface Specifications" section.	—
May 2005, v3.0	• Updated tables throughout chapter. • Updated "Power Consumption" section. • Added various tables. • Replaced "Maximum Input & Output Clock Rate" section with "Maximum Input & Output Clock Toggle Rate" section. • Added "Duty Cycle Distortion" section. • Added "External Memory Interface Specifications" section.	—
March 2005, v2.2	Updated tables in "Internal Timing Parameters" section.	—
January 2005, v2.1	Updated input rise and fall time.	—