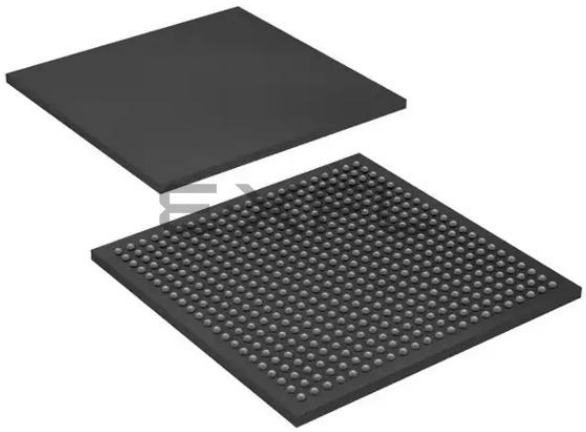


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

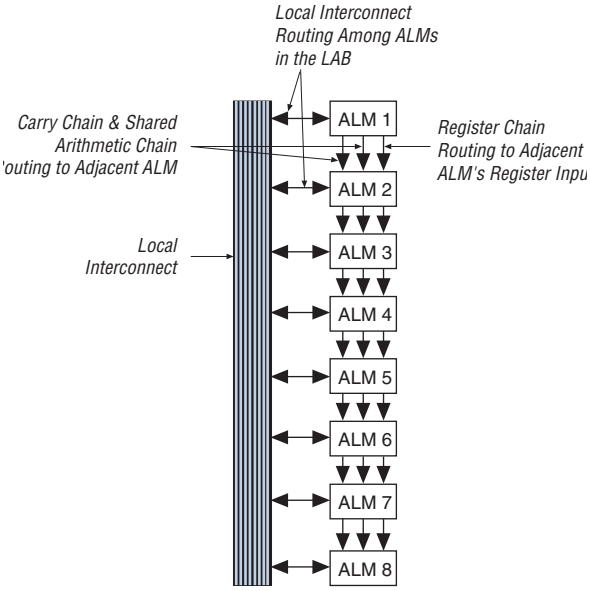
Details	
Product Status	Obsolete
Number of LABs/CLBs	780
Number of Logic Elements/Cells	15600
Total RAM Bits	419328
Number of I/O	342
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s15f484i4n

Chapter 3. Configuration & Testing

Chapter 4. Hot Socketing & Power-On Reset

Chapter 5. DC & Switching Characteristics

Figure 2–17. Shared Arithmetic Chain, Carry Chain & Register Chain Interconnects



The C4 interconnects span four LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–18 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Digital Signal Processing Block

The most commonly used DSP functions are FIR filters, complex FIR filters, IIR filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these use the multiplier as the fundamental building block. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix II devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix II device has from two to four columns of DSP blocks to efficiently implement DSP functions faster than ALM-based implementations. Stratix II devices have up to 24 DSP blocks per column (see Table 2–5). Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

As indicated, the Stratix II DSP block can support one 36 × 36-bit multiplier in a single DSP block. This is true for any combination of signed, unsigned, or mixed sign multiplications.

This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Figure 2–28. DSP Block Diagram for 18 × 18-Bit Configuration

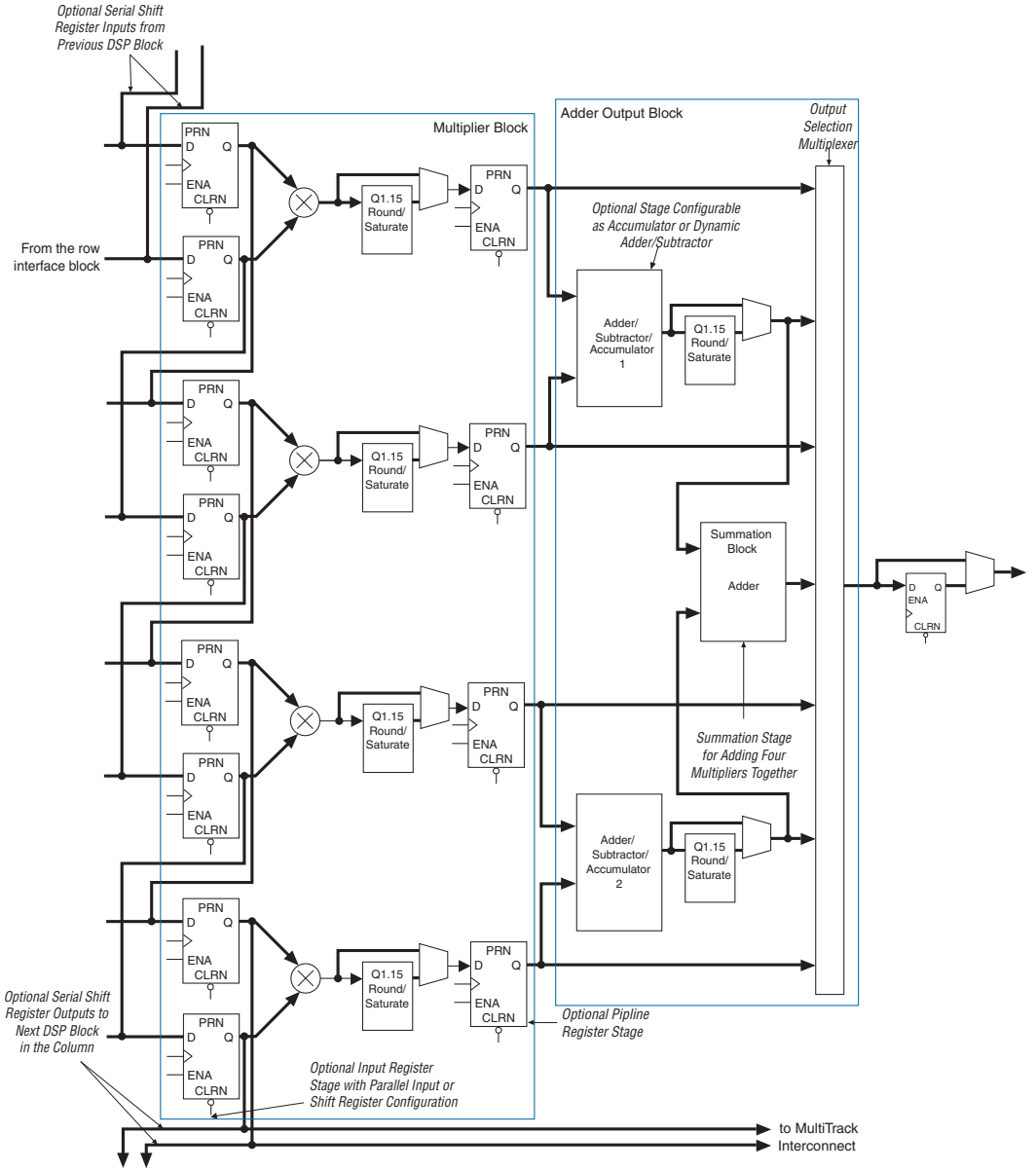
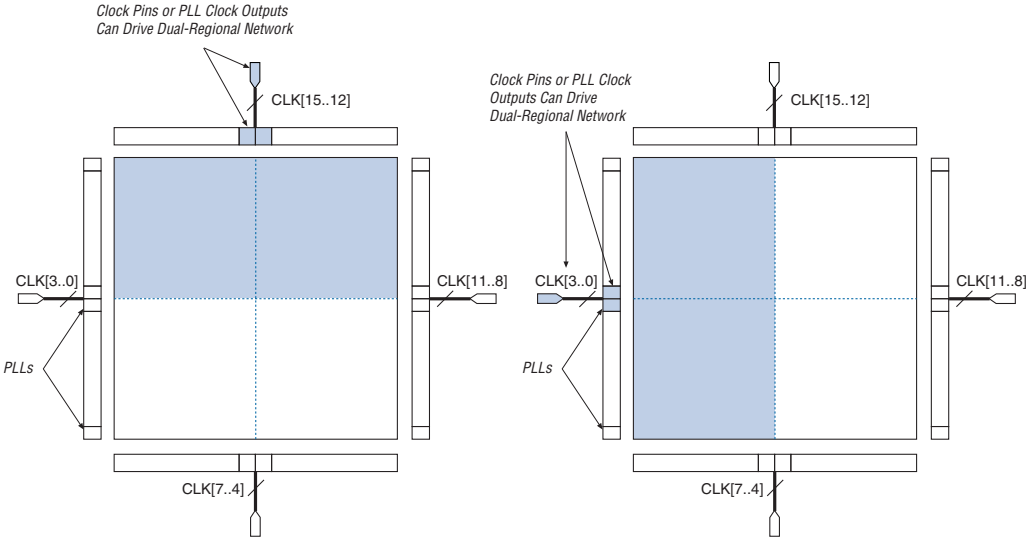


Figure 2–33. Dual-Regional Clocks



Combined Resources

Within each quadrant, there are 24 distinct dedicated clocking resources consisting of 16 global clock lines and eight regional clock lines. Multiplexers are used with these clocks to form busses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer is used at the LAB level to select three of the six row clocks to feed the ALM registers in the LAB (see Figure 2–34).

Figure 2–34. Hierarchical Clock Networks Per Quadrant

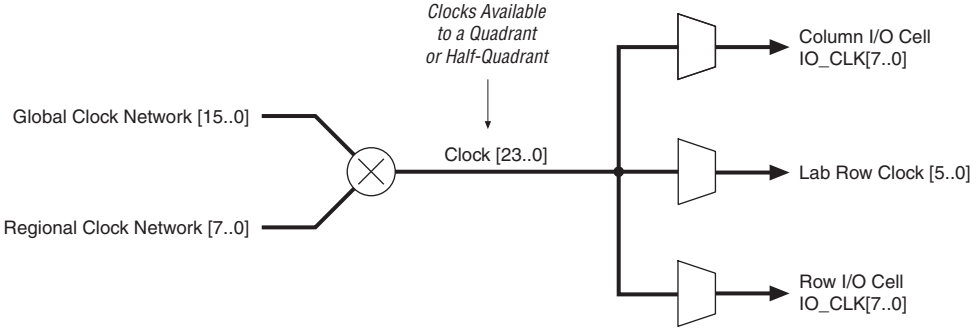
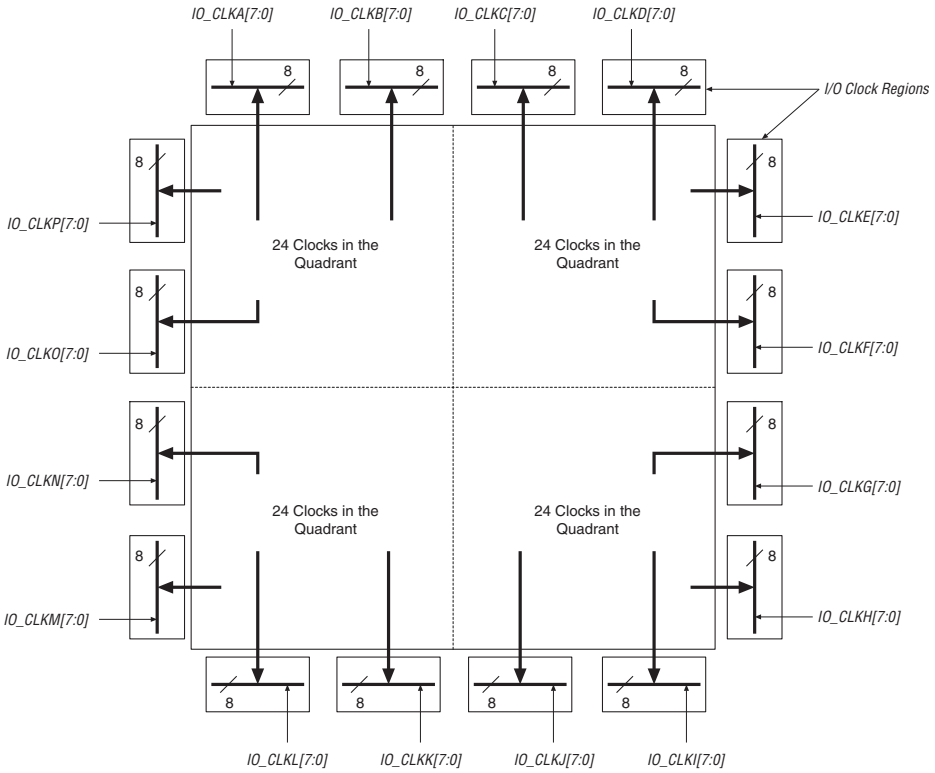


Figure 2–36. EP2S60, EP2S90, EP2S130 & EP2S180 Device I/O Clock Groups



You can use the Quartus II software to control whether a clock input pin drives either a global, regional, or dual-regional clock network. The Quartus II software automatically selects the clocking resources if not specified.

Clock Control Block

Each global clock, regional clock, and PLL external clock output has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable/disable)

Table 2–11. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs (Part 1 of 2)

Top Side Global & Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Clock pins													
CLK12p	✓	✓	✓			✓				✓			
CLK13p	✓	✓	✓				✓						✓
CLK14p	✓			✓	✓			✓				✓	
CLK15p	✓			✓	✓				✓		✓		
CLK12n		✓				✓				✓			
CLK13n			✓				✓						✓
CLK14n				✓				✓				✓	
CLK15n					✓				✓		✓		
Drivers from internal logic													
GCLKDRV0		✓											
GCLKDRV1			✓										
GCLKDRV2				✓									
GCLKDRV3					✓								
RCLKDRV0						✓				✓			
RCLKDRV1							✓				✓		
RCLKDRV2								✓				✓	
RCLKDRV3									✓				✓
RCLKDRV4						✓				✓			
RCLKDRV5							✓				✓		
RCLKDRV6								✓				✓	
RCLKDRV7									✓				✓
Enhanced PLL 5 outputs													
c0	✓	✓	✓			✓				✓			
c1	✓	✓	✓				✓				✓		
c2	✓			✓	✓			✓				✓	
c3	✓			✓	✓				✓				✓

Table 2–11. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs (Part 2 of 2)

Top Side Global & Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
c4	✓					✓		✓		✓		✓	
c5	✓						✓		✓		✓		✓
Enhanced PLL 11 outputs													
c0		✓	✓			✓				✓			
c1		✓	✓				✓				✓		
c2				✓	✓			✓				✓	
c3				✓	✓				✓				✓
c4						✓		✓		✓		✓	
c5							✓		✓		✓		✓

Table 2–12. Global & Regional Clock Connections from Bottom Clock Pins & Enhanced PLL Outputs (Part 1 of 2)

Bottom Side Global & Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
Clock pins													
CLK4p	✓	✓	✓			✓				✓			
CLK5p	✓	✓	✓				✓				✓		
CLK6p	✓			✓	✓			✓				✓	
CLK7p	✓			✓	✓				✓				✓
CLK4n		✓				✓				✓			
CLK5n			✓				✓				✓		
CLK6n				✓				✓				✓	
CLK7n					✓				✓				✓
Drivers from internal logic													
GCLKDRV0		✓											
GCLKDRV1			✓										
GCLKDRV2				✓									

Operating Modes

The Stratix II architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Stratix II devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

PORSEL is a dedicated input pin used to select POR delay times of 12 ms or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms; when the PORSEL pin is connected to V_{CC}, the POR time is 12 ms.

The nIO PULLUP pin is a dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose configuration I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[2..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLR) are on or off before and during configuration. A logic high (1.5, 1.8, 2.5, 3.3 V) turns off the weak internal pull-ups, while a logic low turns them on.

Stratix II devices also offer a new power supply, V_{CCPD}, which must be connected to 3.3 V in order to power the 3.3-V/2.5-V buffer available on the configuration input pins and JTAG pins. V_{CCPD} applies to all the JTAG input pins (TCK, TMS, TDI, and TRST) and the configuration input pins when VCCSEL is connected to ground. See Table 3–4 for more information on the pins affected by VCCSEL.

The VCCSEL pin allows the V_{CCIO} setting (of the banks where the configuration inputs reside) to be independent of the voltage required by the configuration inputs. Therefore, when selecting the V_{CCIO}, the V_{IL} and V_{IH} levels driven to the configuration inputs do not have to be a concern.

Configuring Stratix II FPGAs with the MicroBlaster Driver

The MicroBlaster™ software driver supports an RBF programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems. For more information on the MicroBlaster software driver, see the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *Configuring the MicroBlaster Passive Serial Software Driver White Paper* on the Altera web site (**www.altera.com**).

PLL Reconfiguration

The phase-locked loops (PLLs) in the Stratix II device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.

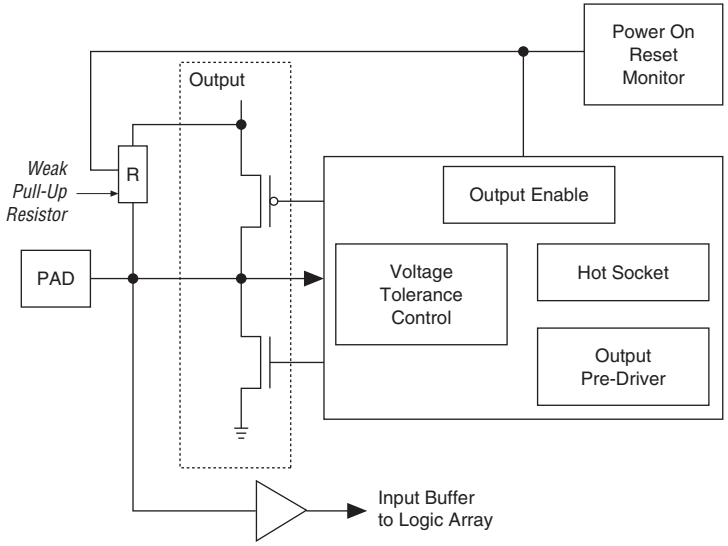
See the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information on Stratix II PLLs.

Temperature Sensing Diode (TSD)

Stratix II devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device. These devices steer bias current through the Stratix II diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus sign). The external device's output represents the junction temperature of the Stratix II device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix II device to connect to the external temperature-sensing device, as shown in Figure 3–1. The temperature sensing diode is a passive element and therefore can be used before the Stratix II device is powered.

Figure 4–1. Hot Socketing Circuit Block Diagram for Stratix II Devices



The POR circuit monitors V_{CCINT} voltage level and keeps I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} is present to keep the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} and/or V_{CCPD} are powered, and it prevents the I/O pins from driving out when the device is not in user mode. The hot socket circuit prevents I/O pins from internally powering V_{CCIO}, V_{CCINT}, and V_{CCPD} when driven by external signals before the device is powered.

Figure 4–2 shows a transistor level cross section of the Stratix II device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot insertion. There is no current path from signal I/O pins to V_{CCINT} or V_{CCIO} or V_{CCPD} during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

Table 5–3. Stratix II Device Recommended Operating Conditions (Part 2 of 2) Note (1)					
Symbol	**Parameter**	**Conditions**	**Minimum**	**Maximum**	**Unit**
T_J	Operating junction temperature	For commercial use	0	85	°C
		For industrial use	–40	100	°C
		For military use *(7)*	–55	125	°C

Notes to Table 5–3:

(1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

(2) During transitions, the inputs may overshoot to the voltage shown in Table 5–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically from ground to V_{CC}.

(4) V_{CCPD} must ramp-up from 0 V to 3.3 V within 100 µs to 100 ms. If V_{CCPD} is not ramped up within this specified time, your Stratix II device does not configure successfully. If your system does not allow for a V_{CCPD} ramp-up time of 100 ms or less, you must hold `nCONFIG` low until all power supplies are reliable.

(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT}, V_{CCPD}, and V_{CCIO} are powered.

(6) V_{CCIO} maximum and minimum conditions for PCI and PCI-X are shown in parentheses.

(7) For more information, refer to the *Stratix II Military Temperature Range Support* technical brief.

DC Electrical Characteristics

Table 5–4 shows the Stratix II device family DC electrical characteristics.

Table 5–4. Stratix II Device DC Operating Conditions (Part 1 of 2) Note (1)							
Symbol	**Parameter**	**Conditions**		**Minimum**	**Typical**	**Maximum**	**Unit**
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(2)*		–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(2)*		–10		10	µA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25° C	EP2S15		0.25	*(3)*	A
			EP2S30		0.30	*(3)*	A
			EP2S60		0.50	*(3)*	A
			EP2S90		0.62	*(3)*	A
			EP2S130		0.82	*(3)*	A
			EP2S180		1.12	*(3)*	A
I_{CCPD0}	V_{CCPD} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25° C, V_{CCPD} = 3.3V	EP2S15		2.2	*(3)*	mA
			EP2S30		2.7	*(3)*	mA
			EP2S60		3.6	*(3)*	mA
			EP2S90		4.3	*(3)*	mA
			EP2S130		5.4	*(3)*	mA
			EP2S180		6.8	*(3)*	mA

Table 5–19. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.500	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.188	1.250	1.313	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.18		3.00	V
V_{IL} (DC)	Low-level DC input voltage		–0.30		V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.35			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} - 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(1)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(1)*			V_{TT} – 0.57	V

Note to Table 5–19:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–20. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.500	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.188	1.250	1.313	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.18		V_{CCIO} + 0.30	V
V_{IL} (DC)	Low-level DC input voltage		–0.30		V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.35			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} - 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(1)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(1)*			V_{TT} – 0.76	V

Note to Table 5–20:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–25. 1.5-V HSTL Class I & II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.425	1.500	1.575	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.90	V
V_{DIF} (AC)	AC differential input voltage		0.4			V
V_{OX} (AC)	AC differential cross point voltage		0.68		0.90	V

Table 5–26. 1.8-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Input reference voltage		0.85	0.90	0.95	V
V_{TT}	Termination voltage		0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 5–26:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–41. M4K Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min (4)	Max	Min (4)	Max	Min (5)	Max	Min (4)	Max	
$t_{M4KDATAASU}$	A port data setup time before clock	22		23		25 25		29		ps
$t_{M4KDATAAH}$	A port data hold time after clock	203		213		233 233		272		ps
$t_{M4KADDRASU}$	A port address setup time before clock	22		23		25 25		29		ps
$t_{M4KADDRAH}$	A port address hold time after clock	203		213		233 233		272		ps
$t_{M4KDATABSU}$	B port data setup time before clock	22		23		25 25		29		ps
$t_{M4KDATABH}$	B port data hold time after clock	203		213		233 233		272		ps
$t_{M4KRADDRBSU}$	B port address setup time before clock	22		23		25 25		29		ps
$t_{M4KRADDRBH}$	B port address hold time after clock	203		213		233 233		272		ps
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers	334	524	334	549	319 334	601	334	701	ps
$t_{M4KDATACO2}$ (6)	Clock-to-output delay without output registers	1,616	2,453	1,616	2,574	1,540 1,616	2,820	1,616	3,286	ps
$t_{M4KCLKH}$	Minimum clock high time	1,250		1,312		1,437 1,437		1,675		ps
$t_{M4KCLKL}$	Minimum clock low time	1,250		1,312		1,437 1,437		1,675		ps
t_{M4KCLR}	Minimum clear pulse width	144		151		165 165		192		ps

Notes to Table 5–41:

(1) F_{MAX} of M4K Block obtained using the Quartus II software does not necessarily equal to 1/TM4KRC.
(2) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(3) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.
(4) For the -3 and -5 speed grades, the minimum timing is for the commercial temperature grade. Only -4 speed grade devices offer the industrial temperature grade.
(5) For the -4 speed grade, the first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.
(6) Numbers apply to unpacked memory modes, true dual-port memory modes, and simple dual-port memory modes that use locally routed or non-identical sources for the A and B port registers.

Table 5–53. EP2S60 Column Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.658	1.739	2.920	3.350	3.899	ns
t_{COUT}	1.501	1.574	2.678	3.072	3.575	ns
t_{PLLCIN}	0.06	0.057	0.278	0.304	0.355	ns
$t_{PLLCOUT}$	-0.097	-0.108	0.036	0.026	0.031	ns

Table 5–54. EP2S60 Row Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.463	1.532	2.591	2.972	3.453	ns
t_{COUT}	1.468	1.537	2.587	2.968	3.448	ns
t_{PLLCIN}	-0.153	-0.167	-0.079	-0.099	-0.128	ns
$t_{PLLCOUT}$	-0.148	-0.162	-0.083	-0.103	-0.133	ns

Table 5–55. EP2S60 Row Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.439	1.508	2.562	2.940	3.421	ns
t_{COUT}	1.444	1.513	2.558	2.936	3.416	ns
t_{PLLCIN}	-0.161	-0.174	-0.083	-0.107	-0.126	ns
$t_{PLLCOUT}$	-0.156	-0.169	-0.087	-0.111	-0.131	ns

EP2S90 Clock Timing Parameters

Tables 5–56 through 5–59 show the maximum clock timing parameters for EP2S90 devices.

Table 5–56. EP2S90 Column Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.768	1.850	3.033	3.473	4.040	ns
t_{COUT}	1.611	1.685	2.791	3.195	3.716	ns
t_{PLLCIN}	-0.127	-0.117	0.125	0.129	0.144	ns
$t_{PLLCOUT}$	-0.284	-0.282	-0.117	-0.149	-0.18	ns

Table 5–57. EP2S90 Column Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.783	1.868	3.058	3.502	4.070	ns
t_{COUT}	1.626	1.703	2.816	3.224	3.746	ns
t_{PLLCIN}	-0.137	-0.127	0.115	0.119	0.134	ns
$t_{PLLCOUT}$	-0.294	-0.292	-0.127	-0.159	-0.19	ns

Table 5–58. EP2S90 Row Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.566	1.638	2.731	3.124	3.632	ns
t_{COUT}	1.571	1.643	2.727	3.120	3.627	ns
t_{PLLCIN}	-0.326	-0.326	-0.178	-0.218	-0.264	ns
$t_{PLLCOUT}$	-0.321	-0.321	-0.182	-0.222	-0.269	ns

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 2 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
LVCMOS	4 mA	t_{OP}	1041	1091	2036	2136	2340	2448	ps
		t_{DIP}	1061	1113	2102	2206	2416	2538	ps
	8 mA	t_{OP}	952	999	1786	1874	2053	2153	ps
		t_{DIP}	972	1021	1852	1944	2129	2243	ps
	12 mA	t_{OP}	926	971	1720	1805	1977	2075	ps
		t_{DIP}	946	993	1786	1875	2053	2165	ps
	16 mA	t_{OP}	933	978	1693	1776	1946	2043	ps
		t_{DIP}	953	1000	1759	1846	2022	2133	ps
	20 mA	t_{OP}	921	965	1677	1759	1927	2025	ps
		t_{DIP}	941	987	1743	1829	2003	2115	ps
	24 mA (1)	t_{OP}	909	954	1659	1741	1906	2003	ps
		t_{DIP}	929	976	1725	1811	1982	2093	ps
2.5 V	4 mA	t_{OP}	1004	1053	2063	2165	2371	2480	ps
		t_{DIP}	1024	1075	2129	2235	2447	2570	ps
	8 mA	t_{OP}	955	1001	1841	1932	2116	2218	ps
		t_{DIP}	975	1023	1907	2002	2192	2308	ps
	12 mA	t_{OP}	934	980	1742	1828	2002	2101	ps
		t_{DIP}	954	1002	1808	1898	2078	2191	ps
	16 mA (1)	t_{OP}	918	962	1679	1762	1929	2027	ps
		t_{DIP}	938	984	1745	1832	2005	2117	ps

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 5 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVTTL	OCT 50 Ω	133	152	152	133	152	152	147	152	152
2.5-V LVTTL	OCT 50 Ω	207	274	274	207	274	274	235	274	274
1.8-V LVTTL	OCT 50 Ω	151	165	165	151	165	165	153	165	165
3.3-V LVCMOS	OCT 50 Ω	300	316	316	300	316	316	263	316	316
1.5-V LVCMOS	OCT 50 Ω	157	171	171	157	171	171	174	171	171
SSTL-2 Class I	OCT 50 Ω	121	134	134	121	134	134	77	134	134
SSTL-2 Class II	OCT 25 Ω	56	101	101	56	101	101	58	101	101
SSTL-18 Class I	OCT 50 Ω	100	123	123	100	123	123	106	123	123
SSTL-18 Class II	OCT 25 Ω	61	110	110	-	-	-	59	110	110
1.2-V HSTL *(2)*	OCT 50 Ω	95	-	-	-	-	-	-	-	95

Notes to Table 5–79:

(1) For LVDS and HyperTransport technology output on row I/O pins, the toggle rate derating factors apply to loads larger than 5 pF. In the derating calculation, subtract 5 pF from the intended load value in pF for the correct result. For a load less than or equal to 5 pF, refer to Table 5–78 for output toggle rates.
(2) 1.2-V HSTL is only supported on column I/O pins in I/O banks 4,7, and 8.
(3) Differential HSTL and SSTL is only supported on column clock and DQS outputs.
(4) LVPECL is only supported on column clock outputs.

Duty Cycle Distortion

Duty cycle distortion (DCD) describes how much the falling edge of a clock is off from its ideal position. The ideal position is when both the clock high time (CLKH) and the clock low time (CLKL) equal half of the clock period (T), as shown in Figure 5–7. DCD is the deviation of the non-ideal falling edge from the ideal falling edge, such as D1 for the falling edge A and D2 for the falling edge B (Figure 5–7). The maximum DCD for a clock is the larger value of D1 and D2.

Table 5–103. Document Revision History (Part 3 of 3)

Date and Document Version	Changes Made	Summary of Changes
January 2005, v2.0	• Updated the "Power Consumption" section. • Added the "High-Speed I/O Specifications" and "On-Chip Termination Specifications" sections. • Removed the ESD Protection Specifications section. • Updated Tables 5–3 through 5–13, 5–16 through 5–18, 5–21, 5–35, 5–39, and 5–40. • Updated tables in "Timing Model" section. • Added Tables 5–30 and 5–31.	—
October 2004, v1.2	• Updated Table 5–3. • Updated introduction text in the "PLL Timing Specifications" section.	—
July 2004, v1.1	• Re-organized chapter. • Added typical values and C_{OUTFB} to Table 5–32. • Added undershoot specification to Note (4) for Tables 5–1 through 5–9. • Added Note (1) to Tables 5–5 and 5–6. • Added V_{ID} and V_{ICM} to Table 5–10. • Added "I/O Timing Measurement Methodology" section. • Added Table 5–72. • Updated Tables 5–1 through 5–2 and Tables 5–24 through 5–29.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—