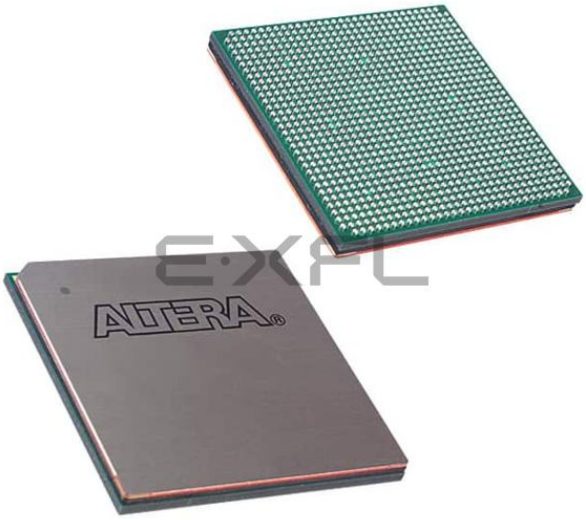
Intel - EP2S180F1020C3 Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8970
Number of Logic Elements/Cells	179400
Total RAM Bits	9383040
Number of I/O	742
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s180f1020c3

Stratix II devices are available in space-saving FineLine BGA® packages (see Tables 1–2 and 1–3).

Table 1–2. Stratix II Package Options & I/O Pin Counts *Notes (1), (2)*

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	342		366			
EP2S30	342		500			
EP2S60 *(3)*	334		492		718	
EP2S90 *(3)*		308		534	758	902
EP2S130 *(3)*				534	742	1,126
EP2S180 *(3)*					742	1,170

Notes to Table 1–2:

(1) All I/O pin counts include eight dedicated clock input pins (`clk1p`, `clk1n`, `clk3p`, `clk3n`, `clk9p`, `clk9n`, `clk11p`, and `clk11n`) that can be used for data inputs.

(2) The Quartus II software I/O pin counts include one additional pin, `PLL_ENA`, which is not available as general-purpose I/O pins. The `PLL_ENA` pin can only be used to enable the PLLs within the device.

(3) The I/O pin counts for the EP2S60, EP2S90, EP2S130, and EP2S180 devices in the 1020-pin and 1508-pin packages include eight dedicated fast PLL clock inputs (`FPLL7CLKp/n`, `FPLL8CLKp/n`, `FPLL9CLKp/n`, and `FPLL10CLKp/n`) that can be used for data inputs.

Table 1–3. Stratix II FineLine BGA Package Sizes

Dimension	484 Pin	484-Pin Hybrid	672 Pin	780 Pin	1,020 Pin	1,508 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00
Area (mm2)	529	729	729	841	1,089	1,600
Length × width (mm × mm)	23 × 23	27 × 27	27 × 27	29 × 29	33 × 33	40 × 40

All Stratix II devices support vertical migration within the same package (for example, you can migrate between the EP2S15, EP2S30, and EP2S60 devices in the 672-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

To ensure that a board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus II software (Assignments menu > Device > Migration Devices).

The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column.

To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only utilize either the top half or the bottom half of the LAB before connecting to the next LAB. This leaves the other half of the ALMs in the LAB available for implementing narrower fan-in functions in normal mode. Carry chains that use the top four ALMs in the first LAB carry into the top half of the ALMs in the next LAB within the column. Carry chains that use the bottom four ALMs in the first LAB carry into the bottom half of the ALMs in the next LAB within the column. Every other column of LABs is top-half bypassable, while the other LAB columns are bottom-half bypassable.

See the "MultiTrack Interconnect" on page 2–22 section for more information on carry chain interconnect.

Shared Arithmetic Mode

In shared arithmetic mode, the ALM can implement a three-input add. In this mode, the ALM is configured with four 4-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder (either to `adder1` in the same ALM or to `adder0` of the next ALM in the LAB) via a dedicated connection called the shared arithmetic chain. This shared arithmetic chain can significantly improve the performance of an adder tree by reducing the number of summation stages required to implement an adder tree. Figure 2–13 shows the ALM in shared arithmetic mode.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly.

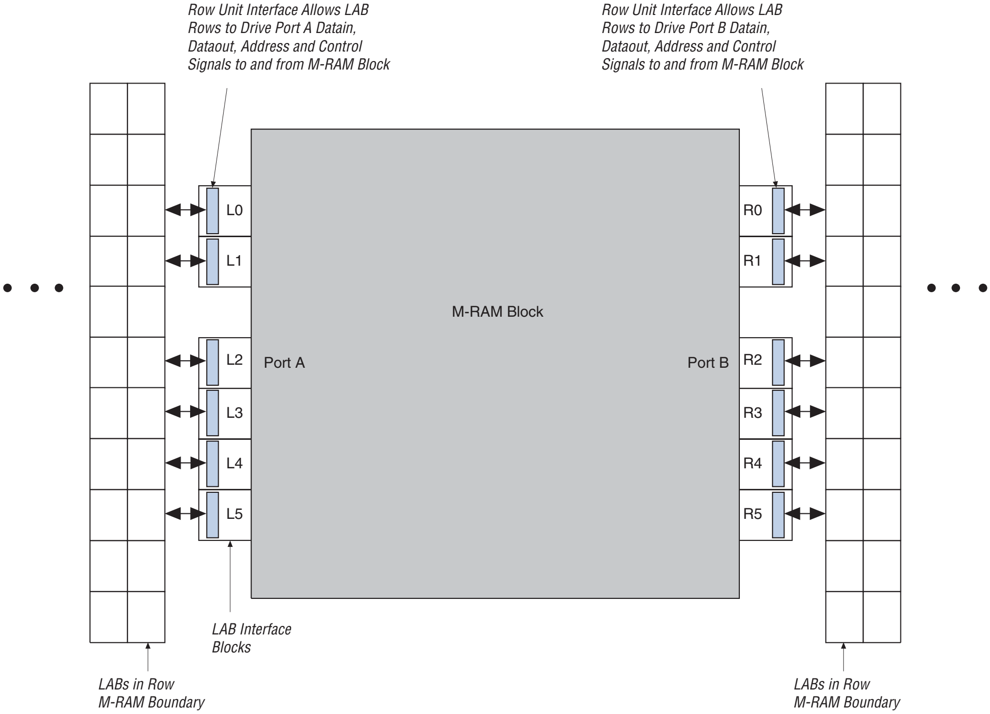
All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (that is, TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[5..0]`.

Table 2–2 shows the Stratix II device's routing scheme.

Table 2–2. Stratix II Device Routing Scheme (Part 1 of 2)

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Shared arithmetic chain										✓						
Carry chain										✓						
Register chain										✓						
Local interconnect										✓	✓	✓	✓	✓	✓	✓
Direct link interconnect				✓												
R4 interconnect				✓		✓	✓	✓	✓							
R24 interconnect						✓	✓	✓	✓							
C4 interconnect				✓		✓		✓								
C16 interconnect						✓	✓	✓	✓							
ALM	✓	✓	✓	✓	✓	✓		✓								
M512 RAM block				✓	✓	✓		✓								
M4K RAM block				✓	✓	✓		✓								
M-RAM block					✓	✓	✓	✓								
DSP blocks					✓	✓		✓								

Figure 2–25. M-RAM Block LAB Row Interface *Note (1)*



Note to Figure 2–25:

(1) Only R24 and C16 interconnects cross the M-RAM block boundaries.

IOE clocks have row and column block regions that are clocked by eight I/O clock signals chosen from the 24 quadrant clock resources. Figures 2–35 and 2–36 show the quadrant relationship to the I/O clock regions.

Figure 2–35. EP2S15 & EP2S30 Device I/O Clock Groups

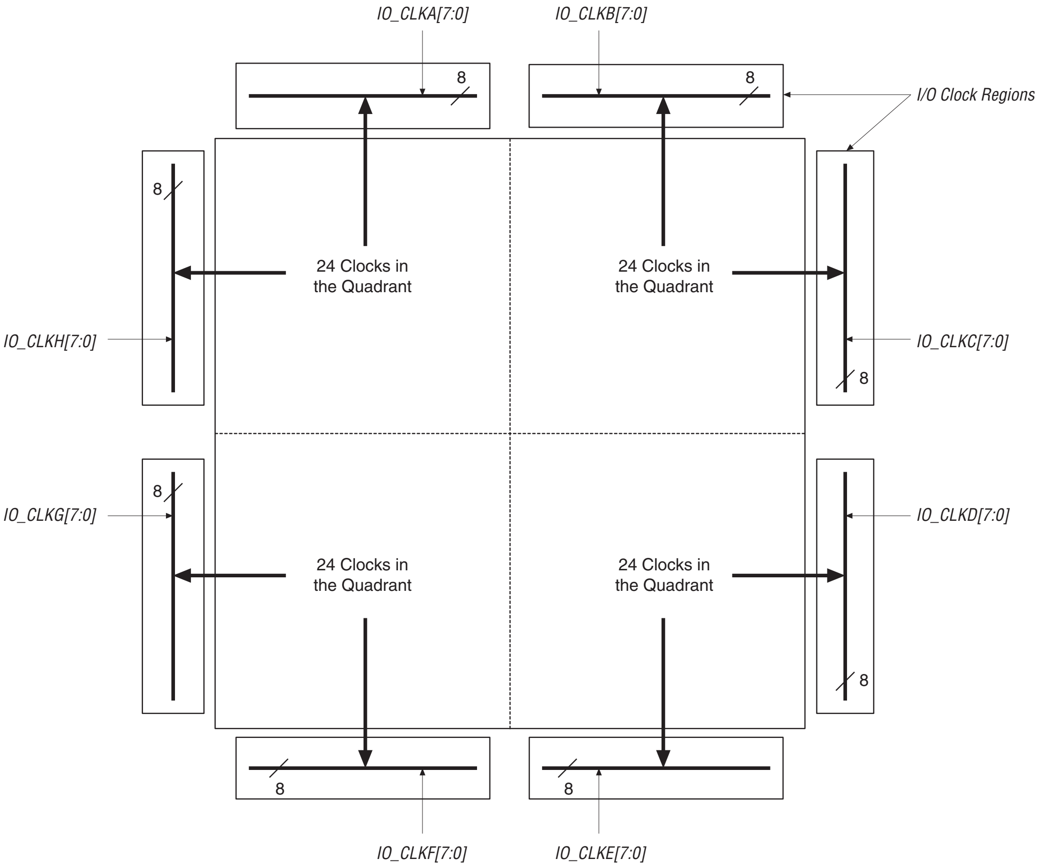
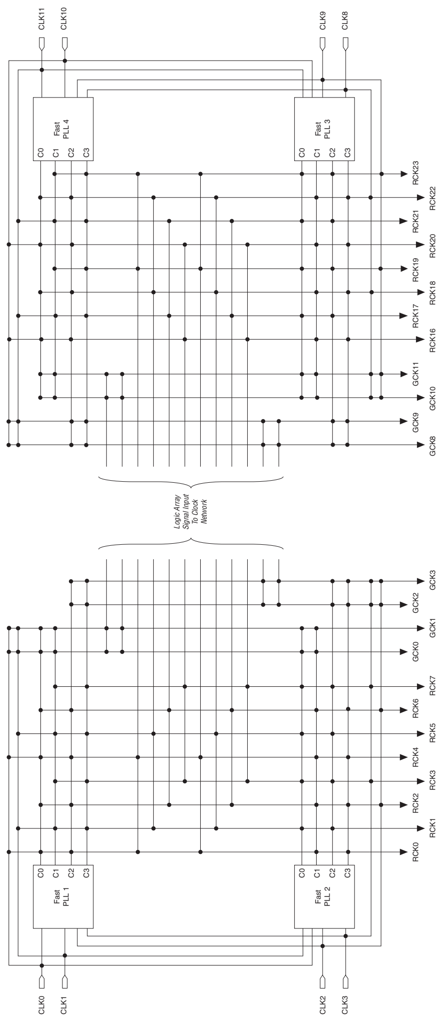


Figure 2–41. Global & Regional Clock Connections from Center Clock Pins & Fast PLL Outputs *Note (1)*

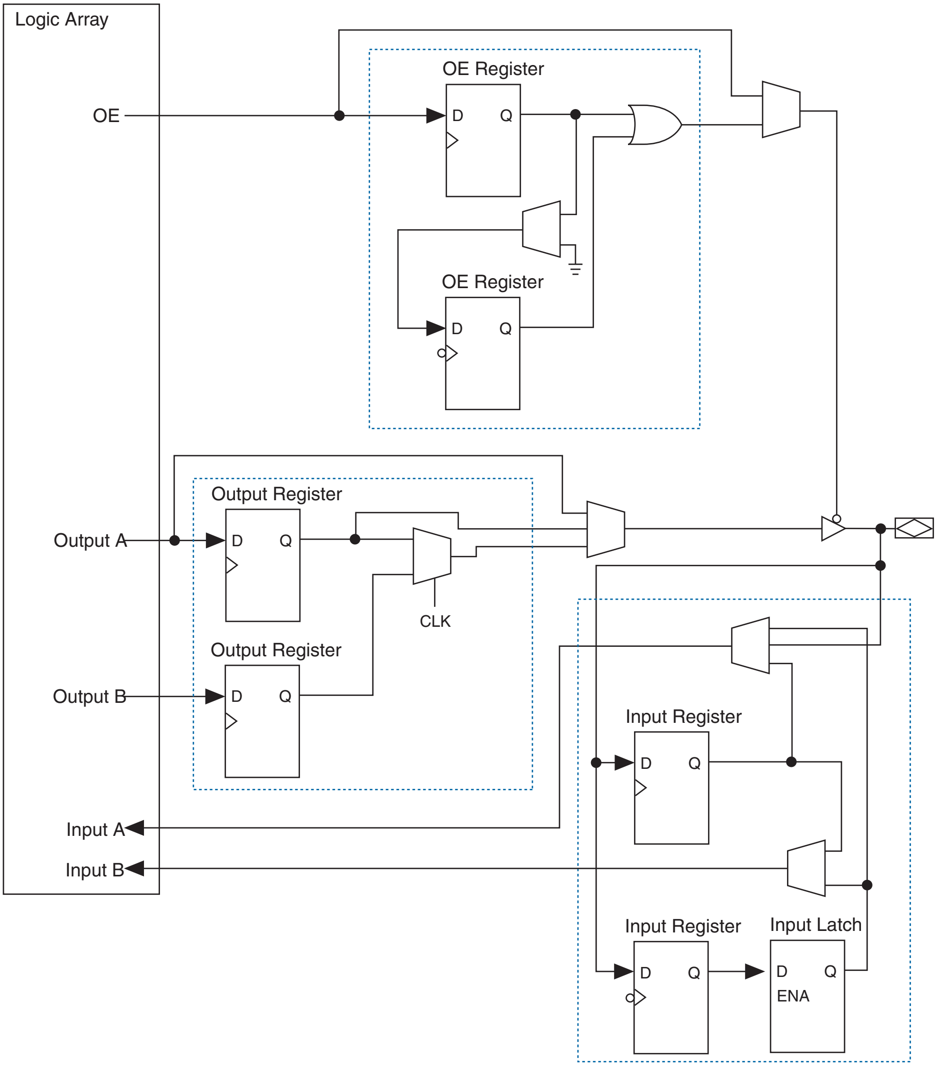


Notes to Figure 2–41:

(1) EP2S15 and EP2S30 devices only have four fast PLLs (1, 2, 3, and 4), but the connectivity from these four PLLs to the global and regional clock networks remains the same as shown.

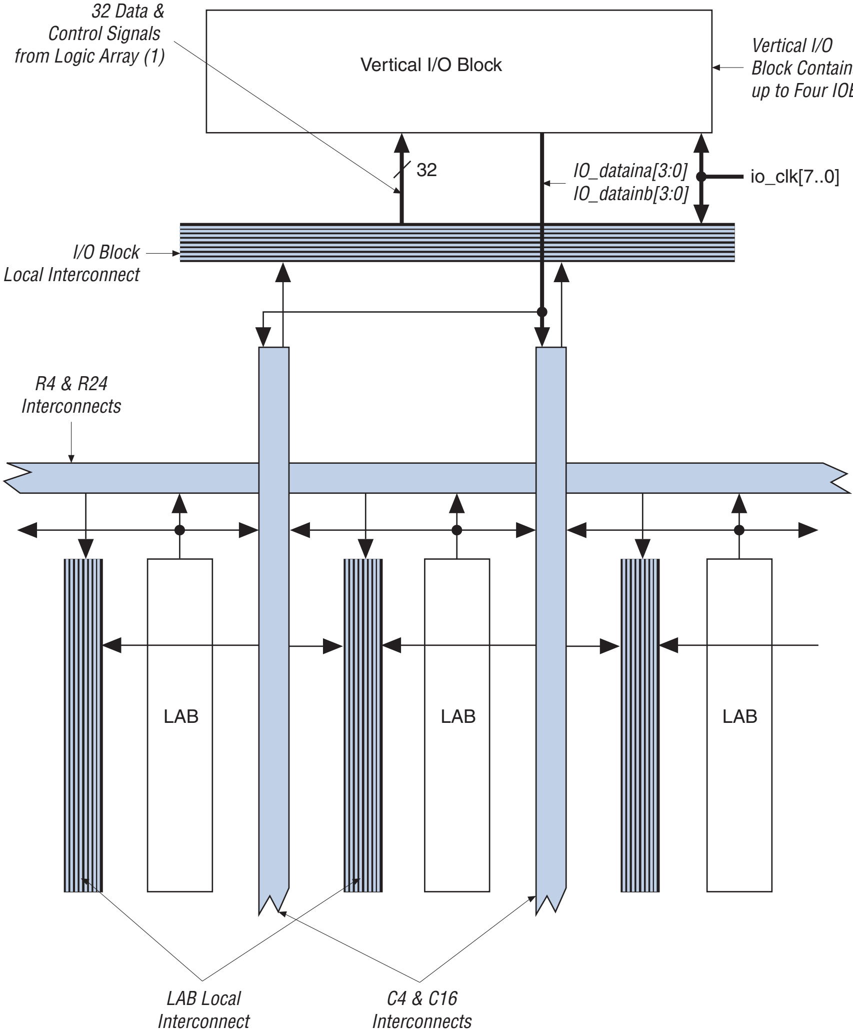
(2) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

Figure 2–46. Stratix II IOE Structure



The IOEs are located in I/O blocks around the periphery of the Stratix II device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 2–47 shows how a row I/O block connects to the logic array. Figure 2–48 shows how a column I/O block connects to the logic array.

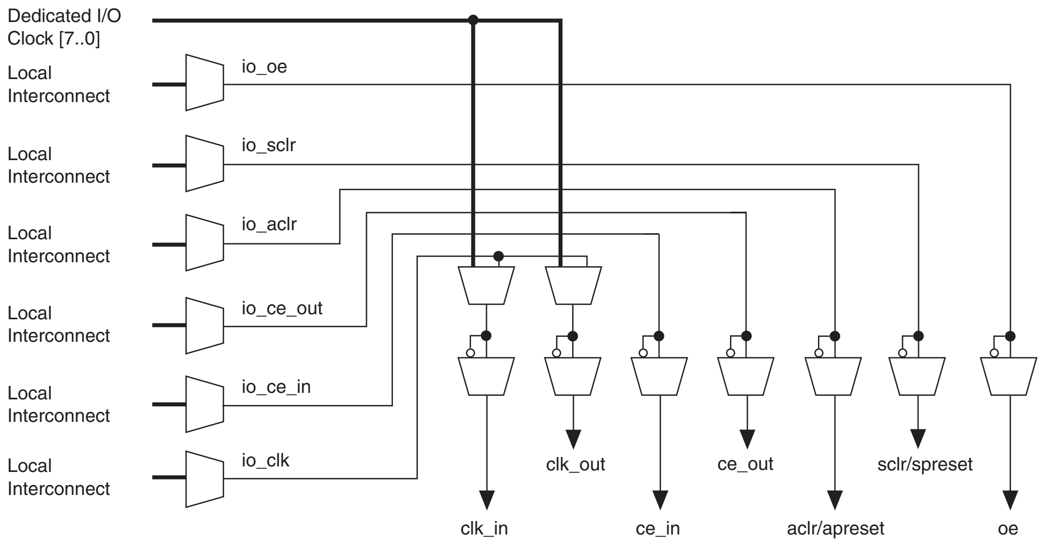
Figure 2–48. Column I/O Block Connection to the Interconnect *Note (1)*



Note to Figure 2–48:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

Figure 2–50. Control Signal Selection per IOE



Notes to Figure 2–50:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects.

Table 2–23. EP2S60 Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs				Corner Fast PLLs *(4)*			
			PLL 1	PLL 2	PLL 3	PLL 4	PLL 7	PLL 8	PLL 9	PLL 10
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10	10	9	9	10
		(3)	19	19	19	19	-	-	-	-
	Receiver	42 *(2)*	11	10	10	11	11	10	10	11
		(3)	21	21	21	21	-	-	-	-
672-pin FineLine BGA	Transmitter	58 *(2)*	16	13	13	16	16	13	13	16
		(3)	29	29	29	29	-	-	-	-
	Receiver	62 *(2)*	17	14	14	17	17	14	14	17
		(3)	31	31	31	31	-	-	-	-
1,020-pin FineLine BGA	Transmitter	84 *(2)*	21	21	21	21	21	21	21	21
		(3)	42	42	42	42	-	-	-	-
	Receiver	84 *(2)*	21	21	21	21	21	21	21	21
		(3)	42	42	42	42	-	-	-	-

Table 2–24. EP2S90 Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs				Corner Fast PLLs *(4)*			
			PLL 1	PLL 2	PLL 3	PLL 4	PLL 7	PLL 8	PLL 9	PLL 10
484-pin Hybrid FineLine BGA	Transmitter	38 *(2)*	10	9	9	10	-	-	-	-
		(3)	19	19	19	19	-	-	-	-
	Receiver	42 *(2)*	11	10	10	11	-	-	-	-
		(3)	21	21	21	21	-	-	-	-
780-pin FineLine BGA	Transmitter	64 *(2)*	16	16	16	16	-	-	-	
		(3)	32	32	32	32	-	-	-	-
	Receiver	68 *(2)*	17	17	17	17	-	-	-	-
		(3)	34	34	34	34	-	-	-	
1,020-pin FineLine BGA	Transmitter	90 *(2)*	23	22	22	23	23	22	22	23
		(3)	45	45	45	45	-	-	-	-
	Receiver	94 *(2)*	23	24	24	23	23	24	24	23
		(3)	46	46	46	46	-	-	-	-
1,508-pin FineLine BGA	Transmitter	118 *(2)*	30	29	29	30	30	29	29	30
		(3)	59	59	59	59	-	-	-	-
	Receiver	118 *(2)*	30	29	29	30	30	29	29	30
		(3)	59	59	59	59	-	-	-	-

Table 2–25. EP2S130 Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs				Corner Fast PLLs *(4)*			
			PLL 1	PLL 2	PLL 3	PLL 4	PLL 7	PLL 8	PLL 9	PLL 10
780-pin FineLine BGA	Transmitter	64 *(2)*	16	16	16	16	-	-	-	
		(3)	32	32	32	32	-	-	-	-
	Receiver	68 *(2)*	17	17	17	17	-	-	-	-
		(3)	34	34	34	34	-	-	-	
1,020-pin FineLine BGA	Transmitter	88 *(2)*	22	22	22	22	22	22	22	22
		(3)	44	44	44	44	-	-	-	-
	Receiver	92 *(2)*	23	23	23	23	23	23	23	23
		(3)	46	46	46	46	-	-	-	-
1,508-pin FineLine BGA	Transmitter	156 *(2)*	37	41	41	37	37	41	41	37
		(3)	78	78	78	78	-	-	-	-
	Receiver	156 *(2)*	37	41	41	37	37	41	41	37
		(3)	78	78	78	78	-	-	-	-

Table 2–26. EP2S180 Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs				Corner Fast PLLs *(4)*			
			PLL 1	PLL 2	PLL 3	PLL 4	PLL 7	PLL 8	PLL 9	PLL 10
1,020-pin FineLine BGA	Transmitter	88 *(2)*	22	22	22	22	22	22	22	22
		(3)	44	44	44	44	-	-	-	-
	Receiver	92 *(2)*	23	23	23	23	23	23	23	23
		(3)	46	46	46	46	-	-	-	-
1,508-pin FineLine BGA	Transmitter	156 *(2)*	37	41	41	37	37	41	41	37
		(3)	78	78	78	78	-	-	-	-
	Receiver	156 *(2)*	37	41	41	37	37	41	41	37
		(3)	78	78	78	78	-	-	-	-

Notes to Tables 2–21 to 2–26:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

(2) This is the maximum number of channels the PLLs can directly drive.

(3) This is the maximum number of channels if the device uses cross bank channels from the adjacent center PLL.

(4) The channels accessible by the center fast PLL overlap with the channels accessible by the corner fast PLL. Therefore, the total number of channels is not the addition of the number of channels accessible by PLLs 1, 2, 3, and 4 with the number of channels accessible by PLLs 7, 8, 9, and 10.

Table 3–1. Stratix II JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring a Stratix II device via the JTAG port with a USB Blaster, MasterBlaster™, ByteBlasterMV™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Notes to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information on using the CONFIG_IO instruction, see the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper*.

Table 5–2. Maximum Duty Cycles in Voltage Transitions				
Symbol	**Parameter**	**Condition**	**Maximum Duty Cycles**	**Unit**
V_I	Maximum duty cycles in voltage transitions	V_I = 4.0 V	100	%
		V_I = 4.1 V	90	%
		V_I = 4.2 V	50	%
		V_I = 4.3 V	30	%
		V_I = 4.4 V	17	%
		V_I = 4.5 V	10	%

Recommended Operating Conditions

Table 5–3 contains the Stratix II device family recommended operating conditions.

Table 5–3. Stratix II Device Recommended Operating Conditions (Part 1 of 2) Note (1)					
Symbol	**Parameter**	**Conditions**	**Minimum**	**Maximum**	**Unit**
V_{CCINT}	Supply voltage for internal logic	100 μs ≤ risetime ≤ 100 ms *(3)*	1.15	1.25	V
V_{CCIO}	Supply voltage for input and output buffers, 3.3-V operation	100 μs ≤ risetime ≤ 100 ms *(3)*, *(6)*	3.135 (3.00)	3.465 (3.60)	V
	Supply voltage for input and output buffers, 2.5-V operation	100 μs ≤ risetime ≤ 100 ms *(3)*	2.375	2.625	V
	Supply voltage for input and output buffers, 1.8-V operation	100 μs ≤ risetime ≤ 100 ms *(3)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	100 μs ≤ risetime ≤ 100 ms *(3)*	1.425	1.575	V
	Supply voltage for input and output buffers, 1.2-V operation	100 μs ≤ risetime ≤ 100 ms *(3)*	1.14	1.26	V
V_{CCPD}	Supply voltage for pre-drivers as well as configuration and JTAG I/O buffers.	100 μs ≤ risetime ≤ 100 ms *(4)*	3.135	3.465	V
V_{CCA}	Analog power supply for PLLs	100 μs ≤ risetime ≤ 100 ms *(3)*	1.15	1.25	V
V_{CCD}	Digital power supply for PLLs	100 μs ≤ risetime ≤ 100 ms *(3)*	1.15	1.25	V
V_I	Input voltage (see Table 5–2)	*(2)*, *(5)*	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		1.71	1.89	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	2.25	V
V_{IL}	Low-level input voltage		–0.30	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OH} = -2$ mA *(2)*	$V_{CCIO} - 0.45$		V
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA *(2)*		0.45	V

Table 5–8. 1.8-V I/O Specifications

Notes to Table 5–8:

(1) The Stratix II device family's V_{CCIO} voltage level support of 1.8 ± -5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–9. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		1.425	1.575	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.30$	V
V_{IL}	Low-level input voltage		–0.30	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OH} = -2$ mA *(2)*	$0.75 \times V_{CCIO}$		V
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA *(2)*		$0.25 \times V_{CCIO}$	V

Notes to Table 5–9:

(1) The Stratix II device family's V_{CCIO} voltage level support of 1.5 ± -5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Figures 5–1 and 5–2 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS, LVPECL, and HyperTransport technology).

Table 5–23. 1.5-V HSTL Class I Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 5–23:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–24. 1.5-V HSTL Class II Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Note to Table 5–24:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–30. Series On-Chip Termination Specification for Top & Bottom I/O Banks (Part 2 of 2) *Notes (1), 2*

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	**Industrial Max**	**Unit**
50-Ω R_S 3.3/2.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	±30	%
50-Ω R_T 2.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
25-Ω R_S 1.8	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_S 1.8	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_T 1.8	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±10	±15	%
50–Ω R_S 1.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±36	±36	%
50-Ω R_T 1.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±10	±15	%
50–Ω R_S 1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±50	±50	%
50-Ω R_T 1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±10	±15	%

Notes for Table 5–30:

(1) The resistance tolerances for calibrated SOCT and POCT are for the moment of calibration. If the temperature or voltage changes over time, the tolerance may also change.

(2) On-chip parallel termination with calibration is only supported for input pins.

Table 5–53. EP2S60 Column Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.658	1.739	2.920	3.350	3.899	ns
t_{COUT}	1.501	1.574	2.678	3.072	3.575	ns
t_{PLLCIN}	0.06	0.057	0.278	0.304	0.355	ns
$t_{PLLCOUT}$	-0.097	-0.108	0.036	0.026	0.031	ns

Table 5–54. EP2S60 Row Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.463	1.532	2.591	2.972	3.453	ns
t_{COUT}	1.468	1.537	2.587	2.968	3.448	ns
t_{PLLCIN}	-0.153	-0.167	-0.079	-0.099	-0.128	ns
$t_{PLLCOUT}$	-0.148	-0.162	-0.083	-0.103	-0.133	ns

Table 5–55. EP2S60 Row Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.439	1.508	2.562	2.940	3.421	ns
t_{COUT}	1.444	1.513	2.558	2.936	3.416	ns
t_{PLLCIN}	-0.161	-0.174	-0.083	-0.107	-0.126	ns
$t_{PLLCOUT}$	-0.156	-0.169	-0.087	-0.111	-0.131	ns

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 2 of 8)									
I/O Standard	**Drive Strength**	**Parameter**	**Minimum Timing**		**-3 Speed Grade** *(3)*	**-3 Speed Grade** *(4)*	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
			Industrial	**Commercial**					
LVCMOS	4 mA	t_{OP}	1041	1091	2036	2136	2340	2448	ps
		t_{DIP}	1061	1113	2102	2206	2416	2538	ps
	8 mA	t_{OP}	952	999	1786	1874	2053	2153	ps
		t_{DIP}	972	1021	1852	1944	2129	2243	ps
	12 mA	t_{OP}	926	971	1720	1805	1977	2075	ps
		t_{DIP}	946	993	1786	1875	2053	2165	ps
	16 mA	t_{OP}	933	978	1693	1776	1946	2043	ps
		t_{DIP}	953	1000	1759	1846	2022	2133	ps
	20 mA	t_{OP}	921	965	1677	1759	1927	2025	ps
		t_{DIP}	941	987	1743	1829	2003	2115	ps
	24 mA *(1)*	t_{OP}	909	954	1659	1741	1906	2003	ps
		t_{DIP}	929	976	1725	1811	1982	2093	ps
2.5 V	4 mA	t_{OP}	1004	1053	2063	2165	2371	2480	ps
		t_{DIP}	1024	1075	2129	2235	2447	2570	ps
	8 mA	t_{OP}	955	1001	1841	1932	2116	2218	ps
		t_{DIP}	975	1023	1907	2002	2192	2308	ps
	12 mA	t_{OP}	934	980	1742	1828	2002	2101	ps
		t_{DIP}	954	1002	1808	1898	2078	2191	ps
	16 mA *(1)*	t_{OP}	918	962	1679	1762	1929	2027	ps
		t_{DIP}	938	984	1745	1832	2005	2117	ps

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 7 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
1.8-V Differential HSTL Class I	4 mA	t_{OP}	912	956	1608	1687	1848	1943	ps
		t_{DIP}	932	978	1674	1757	1924	2033	ps
	6 mA	t_{OP}	917	962	1595	1673	1833	1928	ps
		t_{DIP}	937	984	1661	1743	1909	2018	ps
	8 mA	t_{OP}	896	940	1586	1664	1823	1917	ps
		t_{DIP}	916	962	1652	1734	1899	2007	ps
	10 mA	t_{OP}	900	944	1591	1669	1828	1923	ps
		t_{DIP}	920	966	1657	1739	1904	2013	ps
	12 mA	t_{OP}	892	936	1585	1663	1821	1916	ps
		t_{DIP}	912	958	1651	1733	1897	2006	ps
1.8-V Differential HSTL Class II	16 mA	t_{OP}	877	919	1385	1453	1591	1680	ps
		t_{DIP}	897	941	1451	1523	1667	1770	ps
	18 mA	t_{OP}	879	921	1394	1462	1602	1691	ps
		t_{DIP}	899	943	1460	1532	1678	1781	ps
	20 mA	t_{OP}	879	921	1402	1471	1611	1700	ps
		t_{DIP}	899	943	1468	1541	1687	1790	ps
1.5-V Differential HSTL Class I	4 mA	t_{OP}	912	956	1607	1686	1847	1942	ps
		t_{DIP}	932	978	1673	1756	1923	2032	ps
	6 mA	t_{OP}	917	961	1588	1666	1825	1920	ps
		t_{DIP}	937	983	1654	1736	1901	2010	ps
	8 mA	t_{OP}	899	943	1590	1668	1827	1922	ps
		t_{DIP}	919	965	1656	1738	1903	2012	ps
	10 mA	t_{OP}	900	943	1592	1670	1829	1924	ps
		t_{DIP}	920	965	1658	1740	1905	2014	ps
	12 mA	t_{OP}	893	937	1590	1668	1827	1922	
		t_{DIP}	913	959	1656	1738	1903	2012	

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 4 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
Differential SSTL-18 Class I *(3)*	4 mA	458	570	570	-	-	-	505	570	570
	6 mA	305	380	380	-	-	-	336	380	380
	8 mA	225	282	282	-	-	-	248	282	282
	10 mA	167	220	220	-	-	-	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175
Differential SSTL-18 Class II *(3)*	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
1.8-V Differential HSTL Class I *(3)*	4 mA	245	282	282	-	-	-	229	282	282
	6 mA	164	188	188	-	-	-	153	188	188
	8 mA	123	140	140	-	-	-	114	140	140
	10 mA	110	124	124	-	-	-	108	124	124
	12 mA	97	110	110	-	-	-	104	110	110
1.8-V Differential HSTL Class II *(3)*	16 mA	101	104	104	-	-	-	99	104	104
	18 mA	98	102	102	-	-	-	93	102	102
	20 mA	93	99	99	-	-	-	88	99	99
1.5-V Differential HSTL Class I *(3)*	4 mA	168	196	196	-	-	-	188	196	196
	6 mA	112	131	131	-	-	-	125	131	131
	8 mA	84	99	99	-	-	-	95	99	99
	10 mA	87	98	98	-	-	-	90	98	98
	12 mA	86	98	98	-	-	-	87	98	98
1.5-V Differential HSTL Class II *(3)*	16 mA	95	101	101	-	-	-	96	101	101
	18 mA	95	100	100	-	-	-	101	100	100
	20 mA	94	101	101	-	-	-	104	101	101
3.3-V PCI		134	177	177	-	-	-	143	177	177
3.3-V PCI-X		134	177	177	-	-	-	143	177	177
LVDS		-	-	-	155 *(1)*	155 *(1)*	155 *(1)*	134	134	134
HyperTransport technology		-	-	-	155 *(1)*	155 *(1)*	155 *(1)*	-	-	-
LVPECL *(4)*		-	-	-	-	-	-	134	134	134