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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8970
Number of Logic Elements/Cells	179400
Total RAM Bits	9383040
Number of I/O	742
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2s180f1020c5

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Each Stratix II device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with dedicated clocks, these registers provide exceptional performance and interface support with external memory devices such as DDR and DDR2 SDRAM, RLD RAM II, and QDR II SRAM devices. High-speed serial interface channels with dynamic phase alignment (DPA) support data transfer at up to 1 Gbps using LVDS or HyperTransport™ technology I/O standards.

Figure 2-1 shows an overview of the Stratix II device.

Figure 2-1. Stratix II Block Diagram

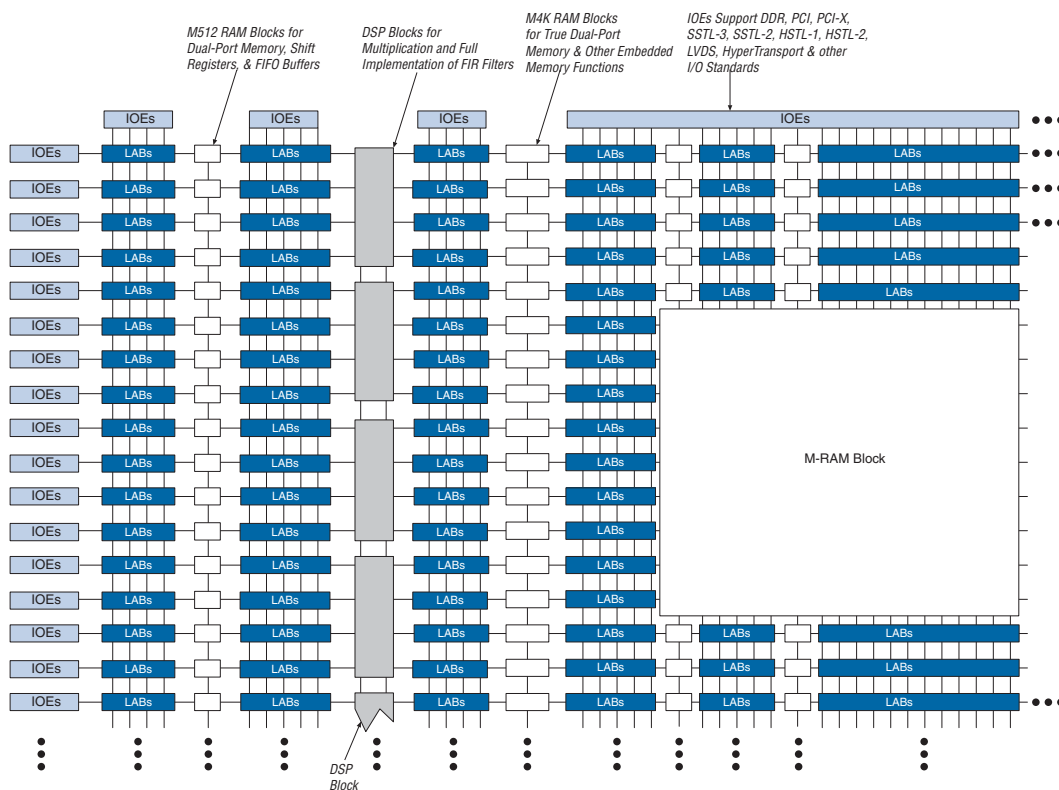
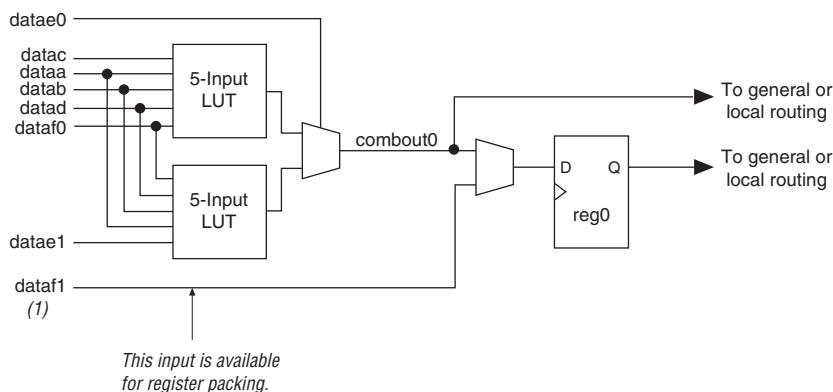


Figure 2–10. Template for Supported Seven-Input Functions in Extended LUT Mode**Note to Figure 2–10:**

- (1) If the seven-input function is unregistered, the unused eighth input is available for register packing. The second register, `reg1`, is not available.

Arithmetic Mode

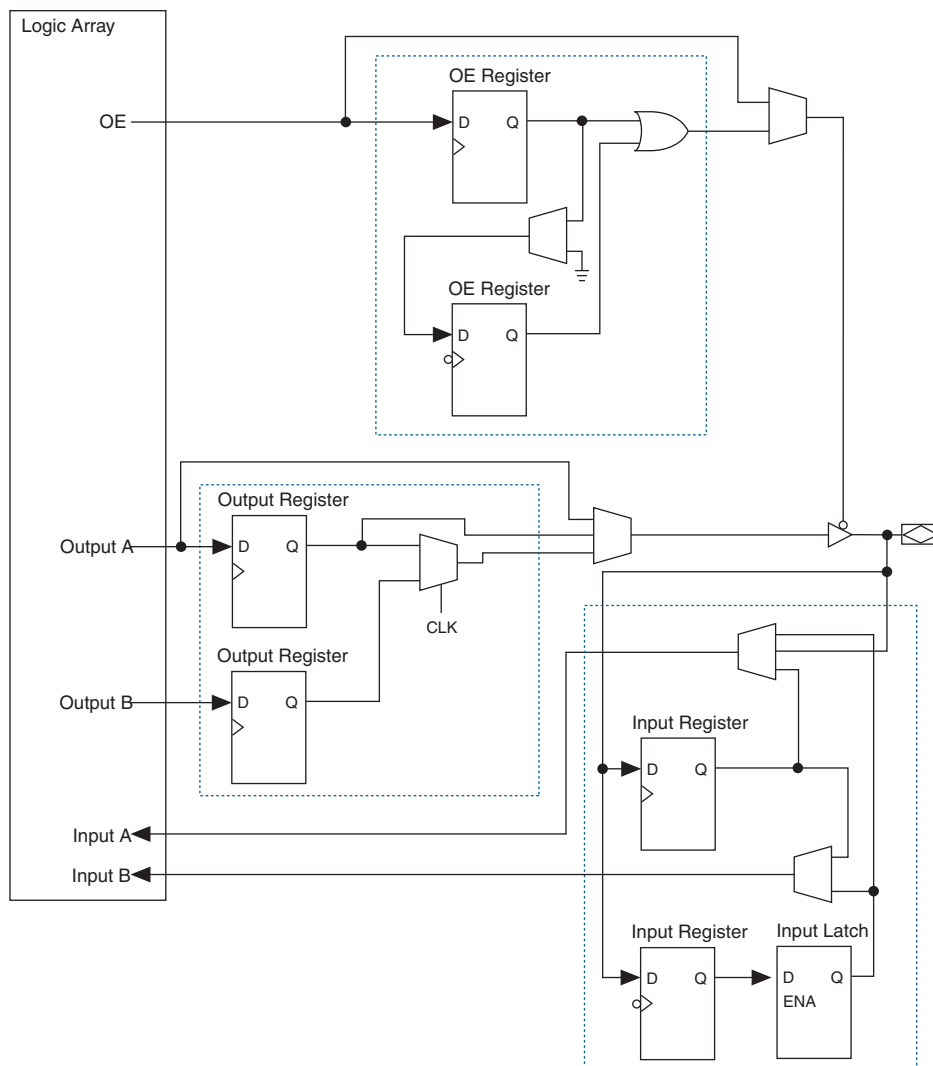
The arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An ALM in arithmetic mode uses two sets of two four-input LUTs along with two dedicated full adders. The dedicated adders allow the LUTs to be available to perform pre-adder logic; therefore, each adder can add the output of two four-input functions. The four LUTs share the `dataaa` and `datab` inputs. As shown in Figure 2–11, the carry-in signal feeds to `adder0`, and the carry-out from `adder0` feeds to carry-in of `adder1`. The carry-out from `adder1` drives to `adder0` of the next ALM in the LAB. ALMs in arithmetic mode can drive out registered and/or unregistered versions of the adder outputs.

The LAB row source for control signals, data inputs, and outputs is shown in [Table 2-7](#).

Table 2-7. DSP Block Signal Sources & Destinations			
LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1[17..0] B1[17..0]	OA[17..0] OB[17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2[17..0] B2[17..0]	OC[17..0] OD[17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3[17..0] B3[17..0]	OE[17..0] OF[17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4[17..0] B4[17..0]	OG[17..0] OH[17..0]



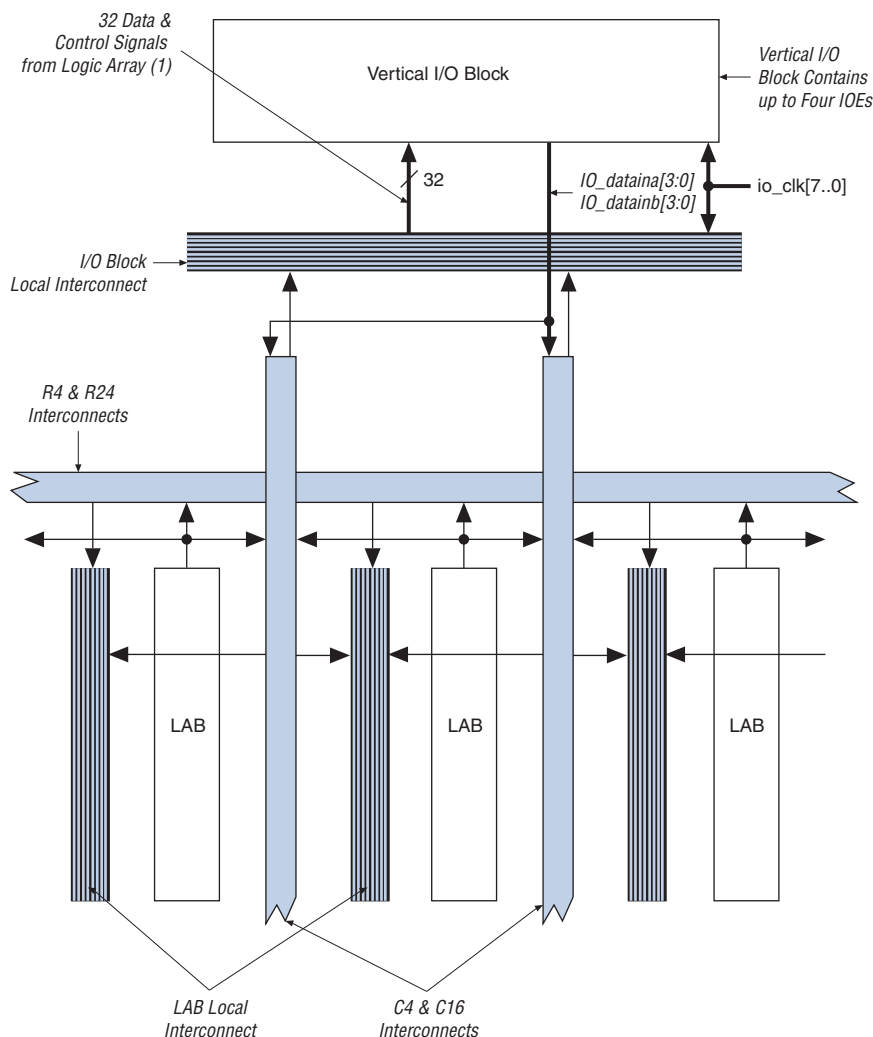
See the *DSP Blocks in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*, for more information on DSP blocks.

Figure 2–46. Stratix II IOE Structure

The IOEs are located in I/O blocks around the periphery of the Stratix II device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects.

Figure 2–47 shows how a row I/O block connects to the logic array.

Figure 2–48 shows how a column I/O block connects to the logic array.

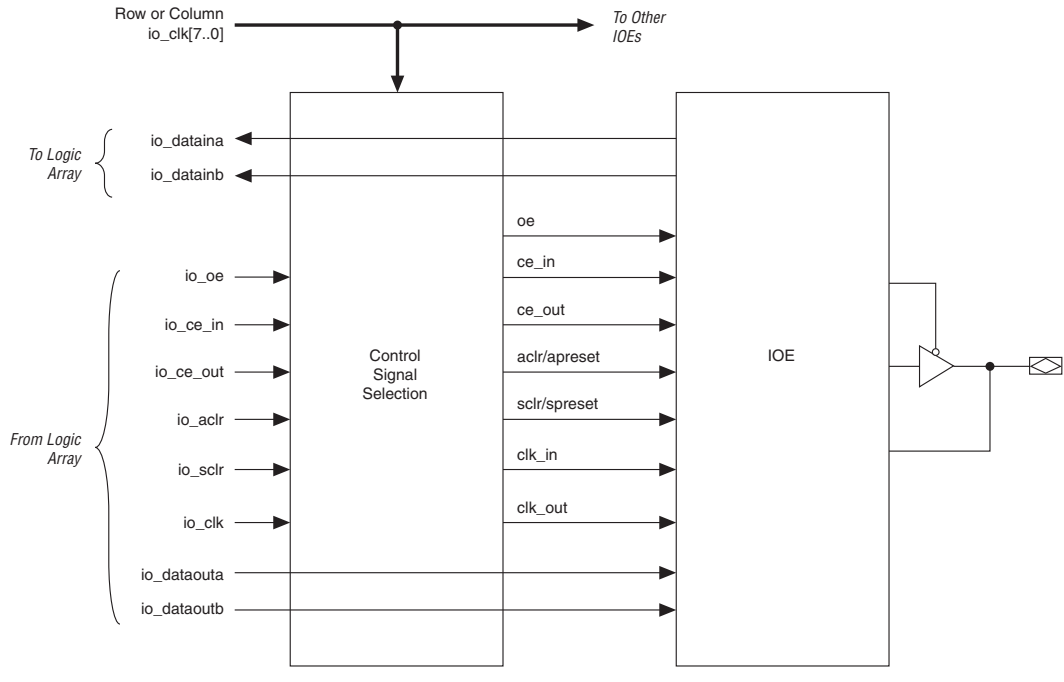
Figure 2–48. Column I/O Block Connection to the Interconnect *Note (1)***Note to Figure 2–48:**

- (1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks (see the “PLLs & Clock Networks” section).

Figure 2–49 illustrates the signal paths through the I/O block.

Figure 2–49. Signal Path through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–50 illustrates the control signal selection.

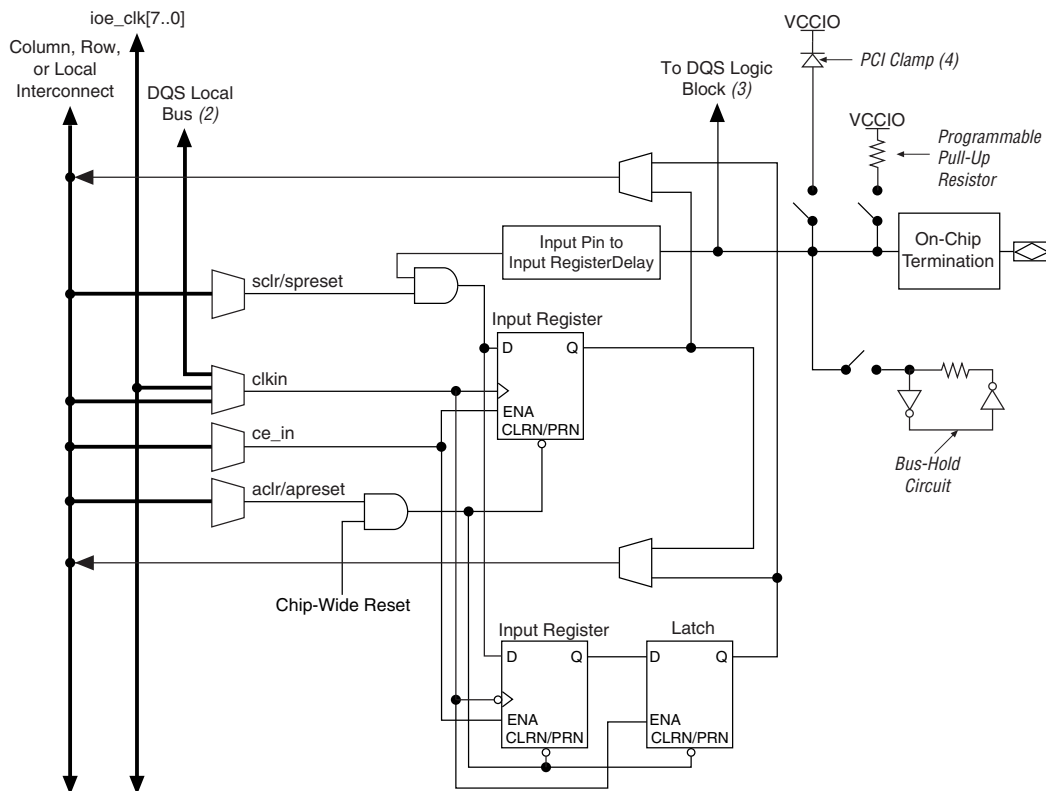


Table 2–15 shows the possible settings for the I/O standards with drive strength control.

Table 2–15. Programmable Drive Strength <i>Note (1)</i>		
I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins	I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins
3.3-V LVTTL	24, 20, 16, 12, 8, 4	12, 8, 4
3.3-V LVCMOS	24, 20, 16, 12, 8, 4	8, 4
2.5-V LVTTL/LVCMOS	16, 12, 8, 4	12, 8, 4
1.8-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.5-V LVCMOS	8, 6, 4, 2	4, 2
SSTL-2 Class I	12, 8	12, 8
SSTL-2 Class II	24, 20, 16	16
SSTL-18 Class I	12, 10, 8, 6, 4	10, 8, 6, 4
SSTL-18 Class II	20, 18, 16, 8	-
HSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
HSTL-18 Class II	20, 18, 16	-
HSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-15 Class II	20, 18, 16	-

Note to Table 2–15:

- (1) The Quartus II software default current setting is the maximum setting for each I/O standard.

Open-Drain Output

Stratix II devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write-enable signals) that can be asserted by any of several devices.

Bus Hold

Each Stratix II device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, you do not need an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated.

Differential On-Chip Termination

Stratix II devices support internal differential termination with a nominal resistance value of 100 Ω for LVDS or HyperTransport technology input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. Differential on-chip termination is supported across the full range of supported differential data rates as shown in the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*.



For more information on differential on-chip termination, refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.



For more information on tolerance specifications for differential on-chip termination, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*.

On-Chip Series Termination Without Calibration

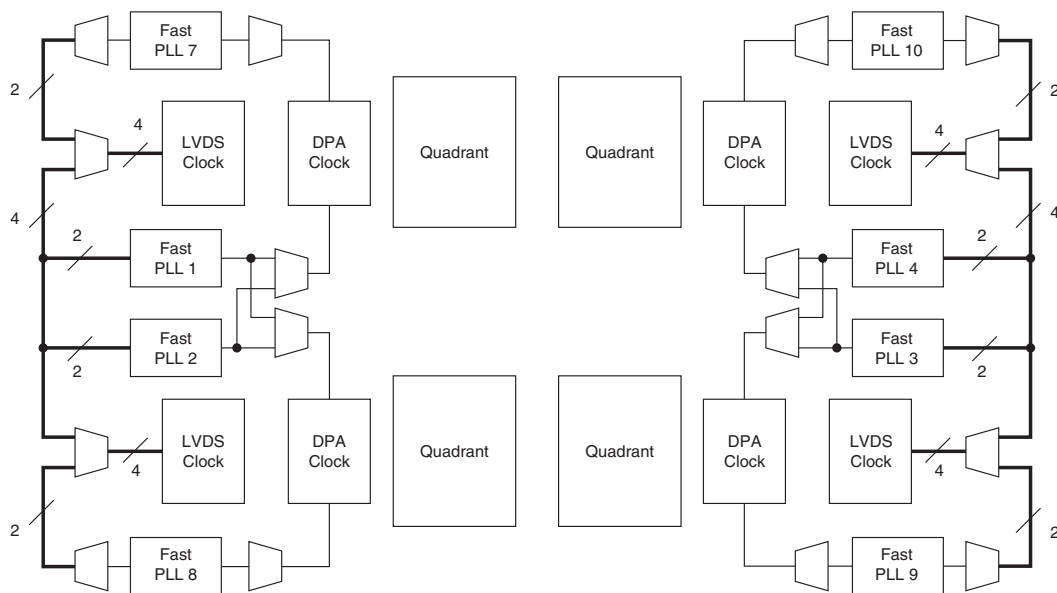
Stratix II devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Stratix II devices support on-chip series termination for single-ended I/O standards with typical R_S values of 25 and 50 Ω . Once matching impedance is selected, current drive strength is no longer selectable. [Table 2–17](#) shows the list of output standards that support on-chip series termination without calibration.

On-Chip Series Termination with Calibration

Stratix II devices support on-chip series termination with calibration in column I/O pins in top and bottom banks. There is one calibration circuit for the top I/O banks and one circuit for the bottom I/O banks. Each on-chip series termination calibration circuit compares the total impedance of each I/O buffer to the external 25- or 50- Ω resistors connected to the RUP and RDN pins, and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.



For more information on series on-chip termination supported by Stratix II devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

Figure 2-61. Fast PLL & Channel Layout in the EP2S60 to EP2S180 Devices *Note (1)*

Note to Figure 2-61:

(1) See Tables 2-22 through 2-26 for the number of channels each device supports.

Operating Modes

The Stratix II architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Stratix II devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

PORSEL is a dedicated input pin used to select POR delay times of 12 ms or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms; when the PORSEL pin is connected to V_{CC} , the POR time is 12 ms.

The nIO PULLUP pin is a dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose configuration I/O pins (nCS0, ASDO, DATA [7 . . 0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM [2 . . 0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLR) are on or off before and during configuration. A logic high (1.5, 1.8, 2.5, 3.3 V) turns off the weak internal pull-ups, while a logic low turns them on.

Stratix II devices also offer a new power supply, V_{CCPD} , which must be connected to 3.3 V in order to power the 3.3-V/2.5-V buffer available on the configuration input pins and JTAG pins. V_{CCPD} applies to all the JTAG input pins (TCK, TMS, TDI, and TRST) and the configuration input pins when VCCSEL is connected to ground. See [Table 3–4](#) for more information on the pins affected by VCCSEL.

The VCCSEL pin allows the V_{CCIO} setting (of the banks where the configuration inputs reside) to be independent of the voltage required by the configuration inputs. Therefore, when selecting the V_{CCIO} , the V_{IL} and V_{IH} levels driven to the configuration inputs do not have to be a concern.

you need to support configuration input voltages of 1.8 V/1.5 V, you should set the VCCSEL to a logic high and the V_{CCIO} of the bank that contains the configuration inputs to 1.8 V/1.5 V.



For more information on multi-volt support, including information on using TDO and nCEO in multi-volt systems, refer to the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Configuration Schemes

You can load the configuration data for a Stratix II device with one of five configuration schemes (see Table 3–5), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix II device. A configuration device can automatically configure a Stratix II device at system power-up.

You can configure multiple Stratix II devices in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Stratix II FPGAs offer the following:

- Configuration data decompression to reduce configuration file storage
- Design security using configuration data encryption to protect your designs
- Remote system upgrades for remotely updating your Stratix II designs

Table 3–5 summarizes which configuration features can be used in each configuration scheme.

Table 3–5. Stratix II Configuration Features (Part 1 of 2)

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
FPP	MAX II device or microprocessor and flash device	✓ (1)	✓ (1)	✓
	Enhanced configuration device		✓ (2)	✓
AS	Serial configuration device	✓	✓	✓ (3)
PS	MAX II device or microprocessor and flash device	✓	✓	✓
	Enhanced configuration device	✓	✓	✓
	Download cable (4)	✓	✓	

Operating Conditions

Stratix® II devices are offered in both commercial and industrial grades. Industrial devices are offered in -4 speed grades and commercial devices are offered in -3 (fastest), -4, -5 speed grades.

Tables 5–1 through 5–32 provide information about absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for Stratix II devices.

Absolute Maximum Ratings

Table 5–1 contains the absolute maximum ratings for the Stratix II device family.

Table 5–1. Stratix II Device Absolute Maximum Ratings <i>Notes (1), (2), (3)</i>					
Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Supply voltage	With respect to ground	–0.5	4.6	V
V_{CCPD}	Supply voltage	With respect to ground	–0.5	4.6	V
V_{CCA}	Analog power supply for PLLs	With respect to ground	–0.5	1.8	V
V_{CCD}	Digital power supply for PLLs	With respect to ground	–0.5	1.8	V
V_I	DC input voltage (4)		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_J	Junction temperature	BGA packages under bias	–55	125	°C

Notes to Tables 5–1

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Conditions beyond those listed in Table 5–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.
- (3) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.
- (4) During transitions, the inputs may overshoot to the voltage shown in Table 5–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 5–65. EP2S180 Column Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	2.003	2.100	3.652	3.993	4.648	ns
t_{COUT}	1.846	1.935	3.398	3.715	4.324	ns
t_{PLLCIN}	-0.3	-0.29	0.053	0.054	0.058	ns
$t_{PLLCOUT}$	-0.457	-0.455	-0.201	-0.224	-0.266	ns

Table 5–66. EP2S180 Row Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.759	1.844	3.273	3.577	4.162	ns
t_{COUT}	1.764	1.849	3.269	3.573	4.157	ns
t_{PLLCIN}	-0.542	-0.541	-0.317	-0.353	-0.414	ns
$t_{PLLCOUT}$	-0.537	-0.536	-0.321	-0.357	-0.419	ns

Table 5–67. EP2S180 Row Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.763	1.850	3.285	3.588	4.176	ns
t_{COUT}	1.768	1.855	3.281	3.584	4.171	ns
t_{PLLCIN}	-0.542	-0.542	-0.319	-0.355	-0.42	ns
$t_{PLLCOUT}$	-0.537	-0.537	-0.323	-0.359	-0.425	ns

Clock Network Skew Adders

The Quartus II software models skew within dedicated clock networks such as global and regional clocks. Therefore, intra-clock network skew adder is not specified. Table 5–68 specifies the clock skew between any two clock networks driving registers in the IOE.

Table 5–68. Clock Network Specifications

Name	Description	Min	Typ	Max	Unit
Clock skew adder EP2S15, EP2S30, EP2S60 (1)	Inter-clock network, same side			±50	ps
	Inter-clock network, entire chip			±100	ps
Clock skew adder EP2S90 (1)	Inter-clock network, same side			±55	ps
	Inter-clock network, entire chip			±110	ps
Clock skew adder EP2S130 (1)	Inter-clock network, same side			±63	ps
	Inter-clock network, entire chip			±125	ps
Clock skew adder EP2S180 (1)	Inter-clock network, same side			±75	ps
	Inter-clock network, entire chip			±150	ps

Note to Table 5–68:

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

Table 5–73. Stratix II I/O Input Delay for Column Pins (Part 3 of 3)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
1.2-V HSTL	t _{PI}	645	677	1194	1252	-	-	ps
	t _{PCOUT}	379	398	758	795	-	-	ps

Notes for Table 5–73:

- (1) These I/O standards are only supported on DQS pins.
- (2) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
- (3) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

Table 5–74. Stratix II I/O Input Delay for Row Pins (Part 1 of 2)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (1)	-3 Speed Grade (2)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
LVTTTL	t _{PI}	715	749	1287	1350	1477	1723	ps
	t _{PCOUT}	391	410	760	798	873	1018	ps
2.5 V	t _{PI}	726	761	1273	1335	1461	1704	ps
	t _{PCOUT}	402	422	746	783	857	999	ps
1.8 V	t _{PI}	788	827	1427	1497	1639	1911	ps
	t _{PCOUT}	464	488	900	945	1035	1206	ps
1.5 V	t _{PI}	792	830	1498	1571	1720	2006	ps
	t _{PCOUT}	468	491	971	1019	1116	1301	ps
LVCMOS	t _{PI}	715	749	1287	1350	1477	1723	ps
	t _{PCOUT}	391	410	760	798	873	1018	ps
SSTL-2 Class I	t _{PI}	547	573	879	921	1008	1176	ps
	t _{PCOUT}	223	234	352	369	404	471	ps
SSTL-2 Class II	t _{PI}	547	573	879	921	1008	1176	ps
	t _{PCOUT}	223	234	352	369	404	471	ps
SSTL-18 Class I	t _{PI}	577	605	960	1006	1101	1285	ps
	t _{PCOUT}	253	266	433	454	497	580	ps
SSTL-18 Class II	t _{PI}	577	605	960	1006	1101	1285	ps
	t _{PCOUT}	253	266	433	454	497	580	ps
1.5-V HSTL Class I	t _{PI}	602	631	1056	1107	1212	1413	ps
	t _{PCOUT}	278	292	529	555	608	708	ps

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 6 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
Differential SSTL-2 Class I	8 mA	t _{OP}	913	957	1715	1799	1971	2041	ps
		t _{DIP}	933	979	1781	1869	2047	2131	ps
	12 mA	t _{OP}	896	940	1672	1754	1921	1991	ps
		t _{DIP}	916	962	1738	1824	1997	2081	ps
Differential SSTL-2 Class II	16 mA	t _{OP}	876	918	1609	1688	1849	1918	ps
		t _{DIP}	896	940	1675	1758	1925	2008	ps
	20 mA	t _{OP}	877	919	1598	1676	1836	1905	ps
		t _{DIP}	897	941	1664	1746	1912	1995	ps
	24 mA	t _{OP}	872	915	1596	1674	1834	1903	ps
		t _{DIP}	892	937	1662	1744	1910	1993	ps
Differential SSTL-18 Class I	4 mA	t _{OP}	909	953	1690	1773	1942	2012	ps
		t _{DIP}	929	975	1756	1843	2018	2102	ps
	6 mA	t _{OP}	914	958	1656	1737	1903	1973	ps
		t _{DIP}	934	980	1722	1807	1979	2063	ps
	8 mA	t _{OP}	894	937	1640	1721	1885	1954	ps
		t _{DIP}	914	959	1706	1791	1961	2044	ps
	10 mA	t _{OP}	898	942	1638	1718	1882	1952	ps
		t _{DIP}	918	964	1704	1788	1958	2042	ps
	12 mA	t _{OP}	891	936	1626	1706	1869	1938	ps
		t _{DIP}	911	958	1692	1776	1945	2028	ps
Differential SSTL-18 Class II	8 mA	t _{OP}	883	925	1597	1675	1835	1904	ps
		t _{DIP}	903	947	1663	1745	1911	1994	ps
	16 mA	t _{OP}	894	937	1578	1655	1813	1882	ps
		t _{DIP}	914	959	1644	1725	1889	1972	ps
	18 mA	t _{OP}	890	933	1585	1663	1821	1890	ps
		t _{DIP}	910	955	1651	1733	1897	1980	ps
	20 mA	t _{OP}	890	933	1583	1661	1819	1888	ps
		t _{DIP}	910	955	1649	1731	1895	1978	ps

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Table 5–77 specifies the maximum input clock toggle rates. Table 5–78 specifies the maximum output clock toggle rates at 0pF load. Table 5–79 specifies the derating factors for the output clock toggle rate for a non 0pF load.

To calculate the output toggle rate for a non 0pF load, use this formula:

The toggle rate for a non 0pF load

$$= 1000 / (1000 / \text{toggle rate at 0pF load} + \text{derating factor} * \text{load value in pF} / 1000)$$

For example, the output toggle rate at 0pF load for SSTL-18 Class II 20mA I/O standard is 550 MHz on a -3 device clock output pin. The derating factor is 94ps/pF. For a 10pF load the toggle rate is calculated as:

$$1000 / (1000/550 + 94 \times 10 / 1000) = 363 \text{ (MHz)}$$

Tables 5–77 through 5–79 show the I/O toggle rates for Stratix II devices.

Table 5–77. Maximum Input Toggle Rate on Stratix II Devices (Part 1 of 2)

Input I/O Standard	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Dedicated Clock Inputs (MHz)		
	-3	-4	-5	-3	-4	-5	-3	-4	-5
LVTTL	500	500	450	500	500	450	500	500	400
2.5-V LVTTL/CMOS	500	500	450	500	500	450	500	500	400
1.8-V LVTTL/CMOS	500	500	450	500	500	450	500	500	400
1.5-V LVTTL/CMOS	500	500	450	500	500	450	500	500	400
LVC MOS	500	500	450	500	500	450	500	500	400
SSTL-2 Class I	500	500	500	500	500	500	500	500	500
SSTL-2 Class II	500	500	500	500	500	500	500	500	500
SSTL-18 Class I	500	500	500	500	500	500	500	500	500
SSTL-18 Class II	500	500	500	500	500	500	500	500	500
1.5-V HSTL Class I	500	500	500	500	500	500	500	500	500
1.5-V HSTL Class II	500	500	500	500	500	500	500	500	500
1.8-V HSTL Class I	500	500	500	500	500	500	500	500	500