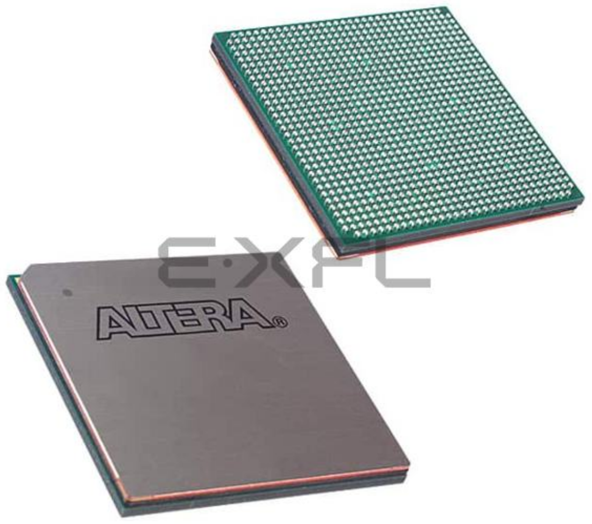
Intel - EP2S180F1020I4 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	8970
Number of Logic Elements/Cells	179400
Total RAM Bits	9383040
Number of I/O	742
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s180f1020i4

Email: info@E-XFL.COM

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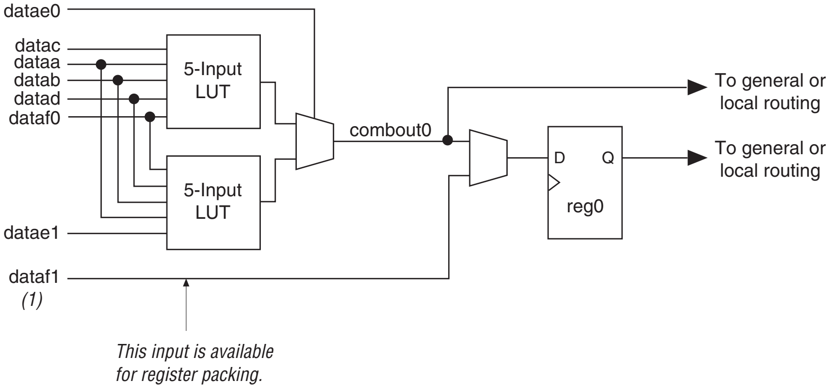
Chapter 6. Reference & Ordering Information

Chapter Revision Dates

The chapters in this book, *Stratix II Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1.	Introduction	
	Revised:	*May 2007*
	Part number:	*SII51001-4.2*
Chapter 2.	Stratix II Architecture	
	Revised:	*May 2007*
	Part number:	*SII51002-4.3*
Chapter 3.	Configuration & Testing	
	Revised:	*May 2007*
	Part number:	*SII51003-4.2*
Chapter 4.	Hot Socketing & Power-On Reset	
	Revised:	*May 2007*
	Part number:	*SII51004-3.2*
Chapter 5.	DC & Switching Characteristics	
	Revised:	*April 2011*
	Part number:	*SII51005-4.5*
Chapter 6.	Reference & Ordering Information	
	Revised:	*April 2011*
	Part number:	*SII51006-2.2*

Figure 2–10. Template for Supported Seven-Input Functions in Extended LUT Mode



Note to Figure 2–10:

(1) If the seven-input function is unregistered, the unused eighth input is available for register packing. The second register, `reg1`, is not available.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An ALM in arithmetic mode uses two sets of two four-input LUTs along with two dedicated full adders. The dedicated adders allow the LUTs to be available to perform pre-adder logic; therefore, each adder can add the output of two four-input functions. The four LUTs share the `dataa` and `datab` inputs. As shown in Figure 2–11, the carry-in signal feeds to `adder0`, and the carry-out from `adder0` feeds to carry-in of `adder1`. The carry-out from `adder1` drives to `adder0` of the next ALM in the LAB. ALMs in arithmetic mode can drive out registered and/or unregistered versions of the adder outputs.

M512 RAM Block

The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

☞ Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

M512 RAM blocks can have different clocks on its inputs and outputs. The wren, datain, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, rden, and output registers can be clocked by either of the two clocks driving the block. This allows the RAM block to operate in read/write or input/output clock modes. Only the output register can be bypassed. The six `labclk` signals or local interconnect can drive the `inclock`, `outclock`, `wren`, `rden`, and `outclr` signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, ALMs can also control the `wren` and `rden` signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 2–19 shows the M512 RAM block control signal generation logic.

The RAM blocks in Stratix II devices have local interconnects to allow ALMs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, C4, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. The M512 RAM block has up to 16 direct link input connections from the left adjacent LABs and another 16 from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through direct link interconnect. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 2–20 shows the M512 RAM block to logic array interface.

Figure 2–19. M512 RAM Block Control Signals

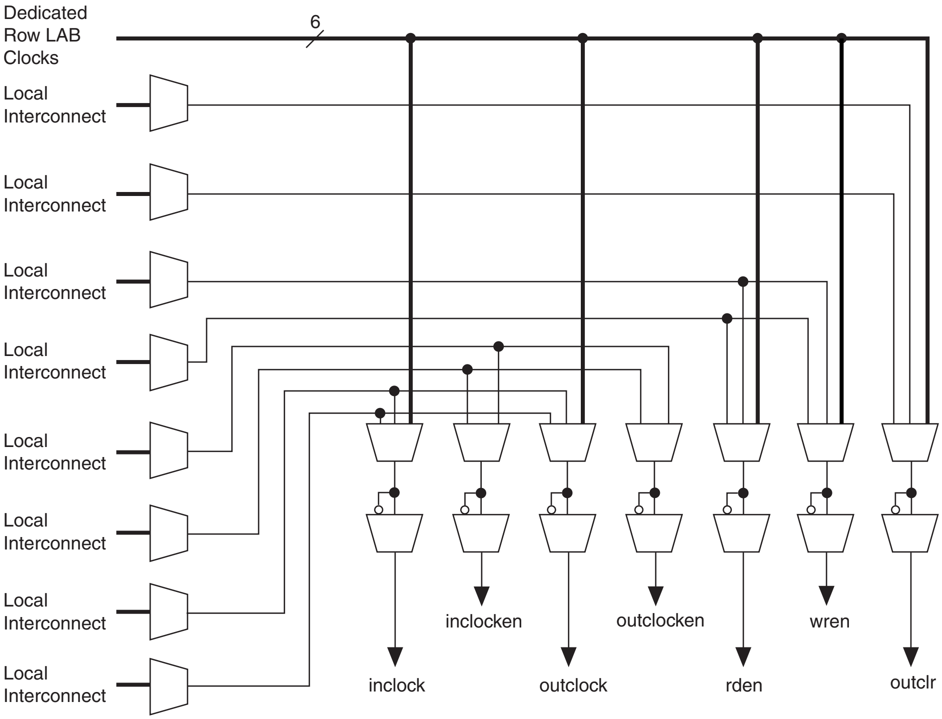


Figure 2–27 shows one of the columns with surrounding LAB rows.

Figure 2–27. DSP Blocks Arranged in Columns

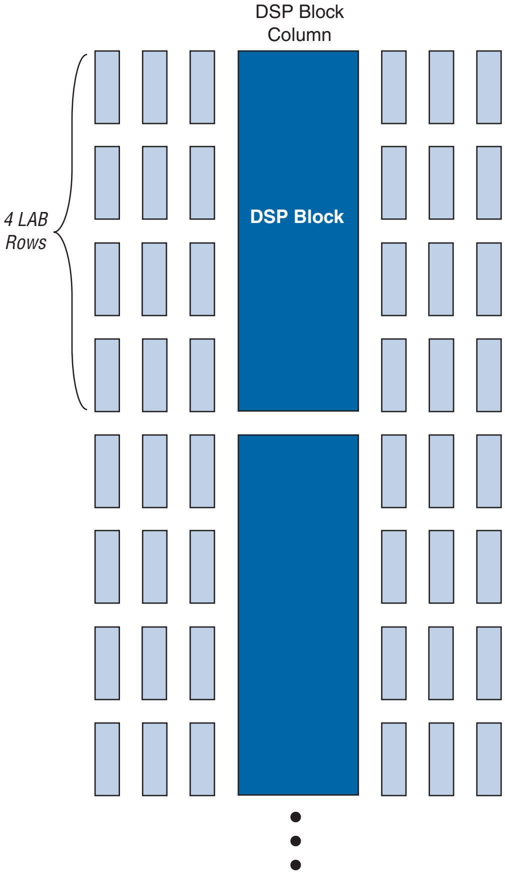
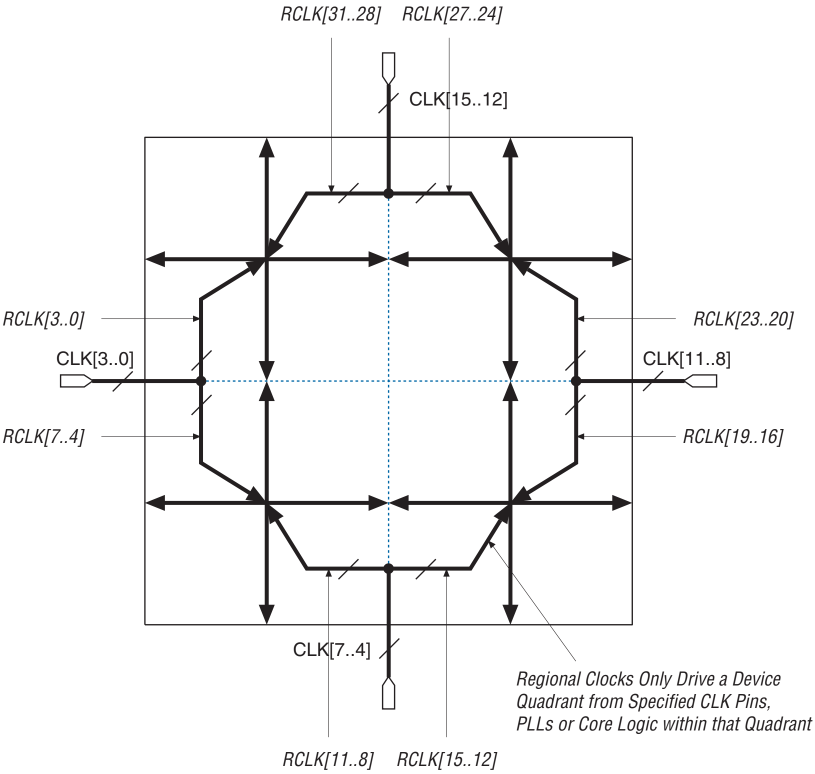


Figure 2–32. Regional Clocks



Regional Clocks Only Drive a Device Quadrant from Specified CLK Pins, PLLs or Core Logic within that Quadrant

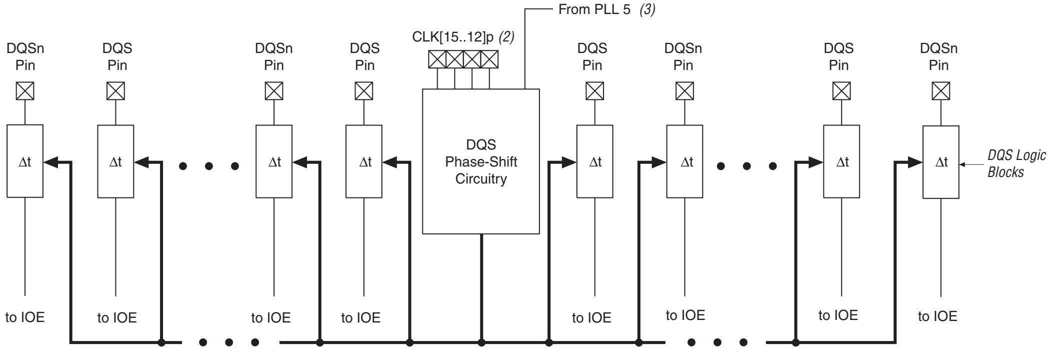
Dual-Regional Clock Network

A single source (`CLK` pin or PLL output) can generate a dual-regional clock by driving two regional clock network lines in adjacent quadrants (one from each quadrant). This allows logic that spans multiple quadrants to utilize the same low skew clock. The routing of this clock signal on an entire side has approximately the same speed but slightly higher clock skew when compared with a clock signal that drives a single quadrant. Internal logic-array routing can also drive a dual-regional clock. Clock pins and enhanced PLL outputs on the top and bottom can drive horizontal dual-regional clocks. Clock pins and fast PLL outputs on the left and right can drive vertical dual-regional clocks, as shown in Figure 2–33. Corner PLLs cannot drive dual-regional clocks.

Table 2–12. Global & Regional Clock Connections from Bottom Clock Pins & Enhanced PLL Outputs (Part 2 of 2)

Bottom Side Global & Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
GCLKDRV3					✓								
RCLKDRV0						✓				✓			
RCLKDRV1							✓				✓		
RCLKDRV2								✓				✓	
RCLKDRV3									✓				✓
RCLKDRV4						✓				✓			
RCLKDRV5							✓				✓		
RCLKDRV6								✓				✓	
RCLKDRV7									✓				✓
Enhanced PLL 6 outputs													
c0	✓	✓	✓			✓				✓			
c1	✓	✓	✓				✓				✓		
c2	✓			✓	✓			✓				✓	
c3	✓			✓	✓				✓				✓
c4	✓					✓		✓		✓		✓	
c5	✓						✓		✓		✓		✓
Enhanced PLL 12 outputs													
c0		✓	✓			✓				✓			
c1		✓	✓				✓				✓		
c2				✓	✓			✓				✓	
c3				✓	✓				✓				✓
c4						✓		✓		✓		✓	
c5							✓		✓		✓		✓

Figure 2–56. DQS Phase-Shift Circuitry *Notes (1), (2), (3), (4)*



Notes to Figure 2–56:

(1) There are up to 18 pairs of DQS and DQSn pins available on the top or the bottom of the Stratix II device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The Δt module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to the phase-shift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

These dedicated circuits combined with enhanced PLL clocking and phase-shift ability provide a complete hardware solution for interfacing to high-speed memory.

For more information on external memory interfaces, refer to the *External Memory Interfaces in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

Programmable Drive Strength

The output buffer for each Stratix II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that the user can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2–20. Supported TDO/TDI Voltage Combinations (Part 2 of 2)

Device	TDI Input Buffer Power	Stratix II TDO V_{CCIO} Voltage Level in I/O Bank 4				
		V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V	V_{CCIO} = 1.2 V
Non-Stratix II	VCC = 3.3 V	✓ *(1)*	✓ *(2)*	✓ *(3)*	Level shifter required	Level shifter required
	VCC = 2.5 V	✓ *(1)*, *(4)*	✓ *(2)*	✓ *(3)*	Level shifter required	Level shifter required
	VCC = 1.8 V	✓ *(1)*, *(4)*	✓ *(2)*, *(5)*	✓	Level shifter required	Level shifter required
	VCC = 1.5 V	✓ *(1)*, *(4)*	✓ *(2)*, *(5)*	✓ *(6)*	✓	✓

Notes to Table 2–20:

(1) The TDO output buffer meets V_{OH} (MIN) = 2.4 V.

(2) The TDO output buffer meets V_{OH} (MIN) = 2.0 V.

(3) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.

(4) Input buffer must be 3.3-V tolerant.

(5) Input buffer must be 2.5-V tolerant.

(6) Input buffer must be 1.8-V tolerant.

High-Speed Differential I/O with DPA Support

Stratix II devices contain dedicated circuitry for supporting differential standards at speeds up to 1 Gbps. The LVDS and HyperTransport differential I/O standards are supported in the Stratix II device. In addition, the LVPECL I/O standard is supported on input and output clock pins on the top and bottom I/O banks.

The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- Parallel RapidIO
- HyperTransport technology

There are four dedicated high-speed PLLs in the EP2S15 to EP2S30 devices and eight dedicated high-speed PLLs in the EP2S60 to EP2S180 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Tables 2–21 through 2–26 show the number of channels that each fast PLL can clock in each of the Stratix II devices. In Tables 2–21 through 2–26 the first row for each transmitter or receiver provides the number of channels driven directly by the PLL. The second row below it shows the maximum channels a PLL can drive if cross bank channels are used from the adjacent center PLL. For example, in the 484-pin FineLine BGA EP2S15 device, PLL 1 can drive a maximum of 10 transmitter channels in I/O bank 1 or a maximum of 19 transmitter channels in I/O banks 1 and 2. The Quartus II software may also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

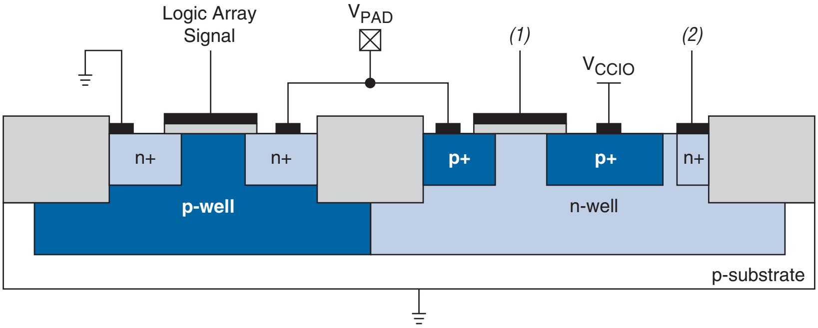
Table 2–21. EP2S15 Device Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs			
			PLL 1	PLL 2	PLL 3	PLL 4
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21
672-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21

Table 2–22. EP2S30 Device Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs			
			PLL 1	PLL 2	PLL 3	PLL 4
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21
672-pin FineLine BGA	Transmitter	58 *(2)*	16	13	13	16
		(3)	29	29	29	29
	Receiver	62 *(2)*	17	14	14	17
		(3)	31	31	31	31

Figure 4–2. Transistor Level Diagram of FPGA Device I/O Buffers



Notes to Figure 4–2:

(1) This is the logic array signal or the larger of either the V_{CCIO} or V_{PAD} signal.

(2) This is the larger of either the V_{CCIO} or V_{PAD} signal.

Power-On Reset Circuitry

Stratix II devices have a POR circuit to keep the whole device system in reset state until the power supply voltage levels have stabilized during power-up. The POR circuit monitors the V_{CCINT}, V_{CCIO}, and V_{CCPD} voltage levels and tri-states all the user I/O pins while V_{CC} is ramping up until normal user levels are reached. The POR circuitry also ensures that all eight I/O bank V_{CCIO} voltages, V_{CCPD} voltage, as well as the logic array V_{CCINT} voltage, reach an acceptable level before configuration is triggered. After the Stratix II device enters user mode, the POR circuit continues to monitor the V_{CCINT} voltage level so that a brown-out condition during user mode can be detected. If there is a V_{CCINT} voltage sag below the Stratix II operational level during user mode, the POR circuit resets the device.

When power is applied to a Stratix II device, a power-on-reset event occurs if V_{CC} reaches the recommended operating range within a certain period of time (specified as a maximum V_{CC} rise time). The maximum V_{CC} rise time for Stratix II device is 100 ms. Stratix II devices provide a dedicated input pin (`PORSEL`) to select POR delay times of 12 or 100 ms during power-up. When the `PORSEL` pin is connected to ground, the POR time is 100 ms. When the `PORSEL` pin is connected to V_{CC}, the POR time is 12 ms.

Table 5–10. 2.5-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)		2.375	2.500	2.625	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	$R_L = 100\ \Omega$	250		450	mV
V_{OCM}	Output common mode voltage	$R_L = 100\ \Omega$	1.125		1.375	V
R_L	Receiver differential input discrete resistor (external to Stratix II devices)		90	100	110	Ω

Table 5–11. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO} *(1)*	I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12)		3.135	3.300	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	$R_L = 100\ \Omega$	250		710	mV
V_{OCM}	Output common mode voltage	$R_L = 100\ \Omega$	840		1,570	mV
R_L	Receiver differential input discrete resistor (external to Stratix II devices)		90	100	110	Ω

Note to Table 5–11:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by `VCC_PLL_OUT`. For differential clock output/feedback operation, `VCC_PLL_OUT` should be connected to 3.3 V.

Table 5–23. 1.5-V HSTL Class I Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.3		$V_{REF} - 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	$V_{CCIO} - 0.4$			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 5–23:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–24. 1.5-V HSTL Class II Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.3		$V_{REF} - 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	$V_{CCIO} - 0.4$			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Note to Table 5–24:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–39. DSP Block Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade *(1)*		-3 Speed Grade *(2)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min *(3)*	Max	Min *(3)*	Max	Min *(4)*	Max	Min *(3)*	Max	
t_{SU}	Input, pipeline, and output register setup time before clock	50		52		57 57		67		ps
t_{H}	Input, pipeline, and output register hold time after clock	180		189		206 206		241		ps
t_{CO}	Input, pipeline, and output register clock-to-output delay	0	0	0	0	0 0	0	0	0	ps
$t_{INREG2PIPE9}$	Input register to DSP block pipeline register in 9 × 9-bit mode	1,312	2,030	1,312	2,030	1,250 1,312	2,334	1,312	2,720	ps
$t_{INREG2PIPE18}$	Input register to DSP block pipeline register in 18 × 18-bit mode	1,302	2,010	1,302	2,110	1,240 1,302	2,311	1,302	2,693	ps
$t_{INREG2PIPE36}$	Input register to DSP block pipeline register in 36 × 36-bit mode	1,302	2,010	1,302	2,110	1,240 1,302	2,311	1,302	2,693	ps
$t_{PIPE2OUTREG2ADD}$	DSP block pipeline register to output register delay in two-multipliers adder mode	924	1,450	924	1,522	880 924	1,667	924	1,943	ps
$t_{PIPE2OUTREG4ADD}$	DSP block pipeline register to output register delay in four-multipliers adder mode	1,134	1,850	1,134	1,942	1,080 1,134	2,127	1,134	2,479	ps
t_{PD9}	Combinational input to output delay for 9 × 9	2,100	2,880	2,100	3,024	2,000 2,100	3,312	2,100	3,859	ps
t_{PD18}	Combinational input to output delay for 18 × 18	2,110	2,990	2,110	3,139	2,010 2,110	3,438	2,110	4,006	ps
t_{PD36}	Combinational input to output delay for 36 × 36	2,939	4,450	2,939	4,672	2,800 2,939	5,117	2,939	5,962	ps
t_{CLR}	Minimum clear pulse width	2,212		2,322		2,543 2,543		2,964		ps

Table 5–76. Stratix II I/O Output Delay for Row Pins (Part 2 of 3)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
2.5 V	4 mA	t_{OP}	1128	1183	2091	2194	2403	2523	ps
		t_{DIP}	1086	1140	2036	2137	2340	2450	ps
	8 mA	t_{OP}	1030	1080	1872	1964	2152	2265	ps
		t_{DIP}	988	1037	1817	1907	2089	2192	ps
	12 mA *(1)*	t_{OP}	1012	1061	1775	1862	2040	2151	ps
		t_{DIP}	970	1018	1720	1805	1977	2078	ps
1.8 V	2 mA	t_{OP}	1196	1253	2954	3100	3396	3542	ps
		t_{DIP}	1154	1210	2899	3043	3333	3469	ps
	4 mA	t_{OP}	1184	1242	2294	2407	2637	2763	ps
		t_{DIP}	1142	1199	2239	2350	2574	2690	ps
	6 mA	t_{OP}	1079	1131	2039	2140	2344	2462	ps
		t_{DIP}	1037	1088	1984	2083	2281	2389	ps
	8 mA *(1)*	t_{OP}	1049	1100	1942	2038	2232	2348	ps
		t_{DIP}	1007	1057	1887	1981	2169	2275	ps
1.5 V	2 mA	t_{OP}	1158	1213	2530	2655	2908	3041	ps
		t_{DIP}	1116	1170	2475	2598	2845	2968	ps
	4 mA	t_{OP}	1055	1106	2020	2120	2322	2440	ps
		t_{DIP}	1013	1063	1965	2063	2259	2367	ps
SSTL-2 Class I	8 mA	t_{OP}	1002	1050	1759	1846	2022	2104	ps
		t_{DIP}	960	1007	1704	1789	1959	2031	ps
SSTL-2 Class II	16 mA *(1)*	t_{OP}	947	992	1581	1659	1817	1897	ps
		t_{DIP}	905	949	1526	1602	1754	1824	ps
SSTL-18 Class I	4 mA	t_{OP}	990	1038	1709	1793	1964	2046	ps
		t_{DIP}	948	995	1654	1736	1901	1973	ps
	6 mA	t_{OP}	994	1042	1648	1729	1894	1975	ps
		t_{DIP}	952	999	1593	1672	1831	1902	ps
	8 mA	t_{OP}	970	1018	1633	1713	1877	1958	ps
		t_{DIP}	928	975	1578	1656	1814	1885	ps
	10 mA *(1)*	t_{OP}	974	1021	1615	1694	1856	1937	ps
		t_{DIP}	932	978	1560	1637	1793	1864	ps

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Table 5–77 specifies the maximum input clock toggle rates. Table 5–78 specifies the maximum output clock toggle rates at 0pF load. Table 5–79 specifies the derating factors for the output clock toggle rate for a non 0pF load.

To calculate the output toggle rate for a non 0pF load, use this formula:

The toggle rate for a non 0pF load

= 1000 / (1000/ toggle rate at 0pF load + derating factor * load value in pF /1000)

For example, the output toggle rate at 0pF load for SSTL-18 Class II 20mA I/O standard is 550 MHz on a -3 device clock output pin. The derating factor is 94ps/pF. For a 10pF load the toggle rate is calculated as:

$$1000 / (1000/550 + 94 \times 10 / 1000) = 363 \text{ (MHz)}$$

Tables 5–77 through 5–79 show the I/O toggle rates for Stratix II devices.

Table 5–77. Maximum Input Toggle Rate on Stratix II Devices (Part 1 of 2)

Input I/O Standard	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Dedicated Clock Inputs (MHz)		
	-3	-4	-5	-3	-4	-5	-3	-4	-5
LVTTL	500	500	450	500	500	450	500	500	400
2.5-V LVTTL/CMOS	500	500	450	500	500	450	500	500	400
1.8-V LVTTL/CMOS	500	500	450	500	500	450	500	500	400
1.5-V LVTTL/CMOS	500	500	450	500	500	450	500	500	400
LVCMOS	500	500	450	500	500	450	500	500	400
SSTL-2 Class I	500	500	500	500	500	500	500	500	500
SSTL-2 Class II	500	500	500	500	500	500	500	500	500
SSTL-18 Class I	500	500	500	500	500	500	500	500	500
SSTL-18 Class II	500	500	500	500	500	500	500	500	500
1.5-V HSTL Class I	500	500	500	500	500	500	500	500	500
1.5-V HSTL Class II	500	500	500	500	500	500	500	500	500
1.8-V HSTL Class I	500	500	500	500	500	500	500	500	500

Table 5–84. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 2 of 2) Notes (1), (2)

DDIO Column Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	1.2-V HSTL	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	1.2 V	
1.8 V	150	265	85	85	85	ps
1.5-V LVCMOS	255	370	140	140	140	ps
SSTL-2 Class I	175	295	65	65	65	ps
SSTL-2 Class II	170	290	60	60	60	ps
SSTL-18 Class I	155	275	55	50	50	ps
SSTL-18 Class II	140	260	70	70	70	ps
1.8-V HSTL Class I	150	270	60	60	60	ps
1.8-V HSTL Class II	150	270	60	60	60	ps
1.5-V HSTL Class I	150	270	55	55	55	ps
1.5-V HSTL Class II	125	240	85	85	85	ps
1.2-V HSTL	240	360	155	155	155	ps
LVPECL	180	180	180	180	180	ps

Notes to Table 5–84:

(1) Table 5–84 assumes the input clock has zero DCD.

(2) The DCD specification is based on a no logic array noise condition.

Table 5–85. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -4 & -5 Devices (Part 1 of 2) Notes (1), (2)

DDIO Column Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)				Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	
3.3-V LVTTL	440	495	170	160	ps
3.3-V LVCMOS	390	450	120	110	ps
2.5 V	375	430	105	95	ps
1.8 V	325	385	90	100	ps
1.5-V LVCMOS	430	490	160	155	ps
SSTL-2 Class I	355	410	85	75	ps
SSTL-2 Class II	350	405	80	70	ps

Table 5–89. High-Speed I/O Specifications for -3 Speed Grade (Part 2 of 2) *Notes (1), (2)*

Symbol	Conditions			-3 Speed Grade			Unit
				Min	Typ	Max	
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		1,040	Mbps
	J = 2 (LVDS, HyperTransport technology)			*(4)*		760	Mbps
	J = 1 (LVDS only)			*(4)*		500	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		1,040	Mbps
TCCS	All differential standards			-		200	ps
SW	All differential standards			330		-	ps
Output jitter						190	ps
Output t_{RISE}	All differential I/O standards					160	ps
Output t_{FALL}	All differential I/O standards					180	ps
t_{DUTY}				45	50	55	%
DPA run length						6,400	UI
DPA jitter tolerance	Data channel peak-to-peak jitter			0.44			UI
DPA lock time	**Standard**	**Training Pattern**	**Transition Density**				Number of repetitions
	SPI-4	0000000000 1111111111	10%	256			
	Parallel Rapid I/O	00001111	25%	256			
		10010000	50%	256			
	Miscellaneous	10101010	100%	256			
		01010101		256			

Notes to Table 5–89:

(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: $150 \leq \text{input clock frequency} \times W \leq 1{,}040$.

(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.

Table 5–91 shows the high-speed I/O timing specifications for -5 speed grade Stratix II devices.

Table 5–91. High-Speed I/O Specifications for -5 Speed Grade *Notes (1), (2)*

<table>
<tr><th rowspan="2">Symbol</th><th rowspan="2" colspan="3">Conditions</th><th colspan="3">-5 Speed Grade</th><th rowspan="2">Unit</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td rowspan="3">f_{HSCLK} (clock frequency)
$f_{HSCLK} = f_{HSDR} / W$</td><td colspan="3">W = 2 to 32 (LVDS, HyperTransport technology) <i>(3)</i></td><td>16</td><td></td><td>420</td><td>MHz</td></tr>
<tr><td colspan="3">W = 1 (SERDES bypass, LVDS only)</td><td>16</td><td></td><td>500</td><td>MHz</td></tr>
<tr><td colspan="3">W = 1 (SERDES used, LVDS only)</td><td>150</td><td></td><td>640</td><td>MHz</td></tr>
<tr><td rowspan="3">f_{HSDR} (data rate)</td><td colspan="3">J = 4 to 10 (LVDS, HyperTransport technology)</td><td>150</td><td></td><td>840</td><td>Mbps</td></tr>
<tr><td colspan="3">J = 2 (LVDS, HyperTransport technology)</td><td><i>(4)</i></td><td></td><td>700</td><td>Mbps</td></tr>
<tr><td colspan="3">J = 1 (LVDS only)</td><td><i>(4)</i></td><td></td><td>500</td><td>Mbps</td></tr>
<tr><td>$f_{HSDRDPA}$ (DPA data rate)</td><td colspan="3">J = 4 to 10 (LVDS, HyperTransport technology)</td><td>150</td><td></td><td>840</td><td>Mbps</td></tr>
<tr><td>TCCS</td><td colspan="3">All differential I/O standards</td><td>-</td><td></td><td>200</td><td>ps</td></tr>
<tr><td>SW</td><td colspan="3">All differential I/O standards</td><td>440</td><td></td><td>-</td><td>ps</td></tr>
<tr><td>Output jitter</td><td colspan="3"></td><td></td><td></td><td>190</td><td>ps</td></tr>
<tr><td>Output t_{RISE}</td><td colspan="3">All differential I/O standards</td><td></td><td></td><td>290</td><td>ps</td></tr>
<tr><td>Output t_{FALL}</td><td colspan="3">All differential I/O standards</td><td></td><td></td><td>290</td><td>ps</td></tr>
<tr><td>t_{DUTY}</td><td colspan="3"></td><td>45</td><td>50</td><td>55</td><td>%</td></tr>
<tr><td>DPA run length</td><td colspan="3"></td><td></td><td></td><td>6,400</td><td>UI</td></tr>
<tr><td>DPA jitter tolerance</td><td colspan="3">Data channel peak-to-peak jitter</td><td>0.44</td><td></td><td></td><td>UI</td></tr>
<tr><td rowspan="6">DPA lock time</td><td>Standard</td><td>Training Pattern</td><td>Transition Density</td><td></td><td></td><td></td><td rowspan="6">Number of repetitions</td></tr>
<tr><td>SPI-4</td><td>0000000000
1111111111</td><td>10%</td><td>256</td><td></td><td></td></tr>
<tr><td rowspan="2">Parallel Rapid I/O</td><td>00001111</td><td>25%</td><td>256</td><td></td><td></td></tr>
<tr><td>10010000</td><td>50%</td><td>256</td><td></td><td></td></tr>
<tr><td rowspan="2">Miscellaneous</td><td>10101010</td><td>100%</td><td>256</td><td></td><td></td></tr>
<tr><td>01010101</td><td></td><td>256</td><td></td><td></td></tr>
</table>

Notes to Table 5–91:

(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: $150 \leq$ input clock frequency $\times W \leq 1{,}040$.

(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.