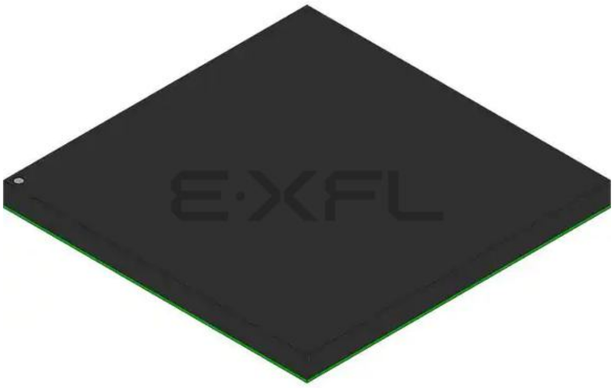
Altera - EP2S180F1508C3 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	-
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA (30x30)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2s180f1508c3

About this Handbook

This handbook provides comprehensive information about the Altera® Stratix® II family of devices.

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Email	www.altera.com/literature
Altera literature services	Website	literature@altera.com
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*

- Support for numerous single-ended and differential I/O standards
- High-speed differential I/O support with DPA circuitry for 1-Gbps performance
- Support for high-speed networking and communications bus standards including Parallel RapidIO, SPI-4 Phase 2 (POS-PHY Level 4), HyperTransport™ technology, and SFI-4
- Support for high-speed external memory, including DDR and DDR2 SDRAM, RLDRAM II, QDR II SRAM, and SDR SDRAM
- Support for multiple intellectual property megafunctions from Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
- Support for design security using configuration bitstream encryption
- Support for remote configuration updates

Table 1–1. Stratix II FPGA Family Features

Feature	EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
ALMs	6,240	13,552	24,176	36,384	53,016	71,760
Adaptive look-up tables (ALUTs) *(1)*	12,480	27,104	48,352	72,768	106,032	143,520
Equivalent LEs *(2)*	15,600	33,880	60,440	90,960	132,540	179,400
M512 RAM blocks	104	202	329	488	699	930
M4K RAM blocks	78	144	255	408	609	768
M-RAM blocks	0	1	2	4	6	9
Total RAM bits	419,328	1,369,728	2,544,192	4,520,488	6,747,840	9,383,040
DSP blocks	12	16	36	48	63	96
18-bit × 18-bit multipliers *(3)*	48	64	144	192	252	384
Enhanced PLLs	2	2	4	4	4	4
Fast PLLs	4	4	8	8	8	8
Maximum user I/O pins	366	500	718	902	1,126	1,170

Notes to Table 1–1:

(1) One ALM contains two ALUTs. The ALUT is the cell used in the Quartus® II software for logic synthesis.

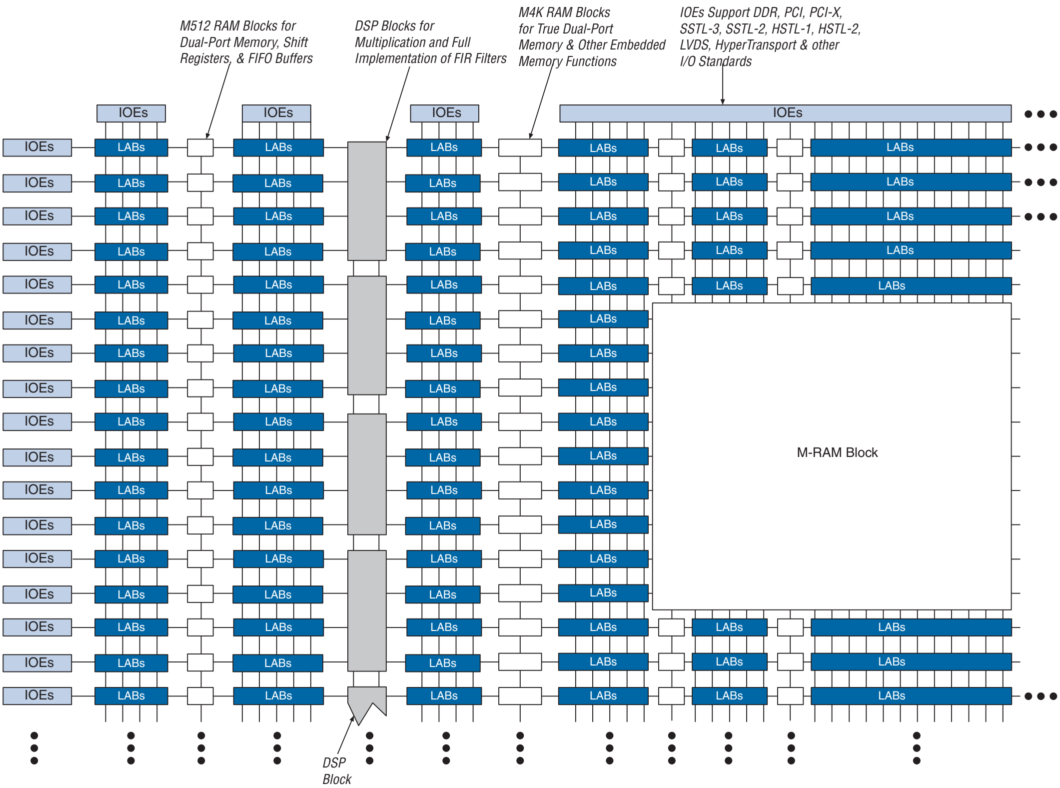
(2) This is the equivalent number of LEs in a Stratix device (four-input LUT-based architecture).

(3) These multipliers are implemented using the DSP blocks.

Each Stratix II device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with dedicated clocks, these registers provide exceptional performance and interface support with external memory devices such as DDR and DDR2 SDRAM, RLDRAM II, and QDR II SRAM devices. High-speed serial interface channels with dynamic phase alignment (DPA) support data transfer at up to 1 Gbps using LVDS or HyperTransport™ technology I/O standards.

Figure 2–1 shows an overview of the Stratix II device.

Figure 2–1. Stratix II Block Diagram



arithmetic chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A shared arithmetic chain can continue as far as a full column.

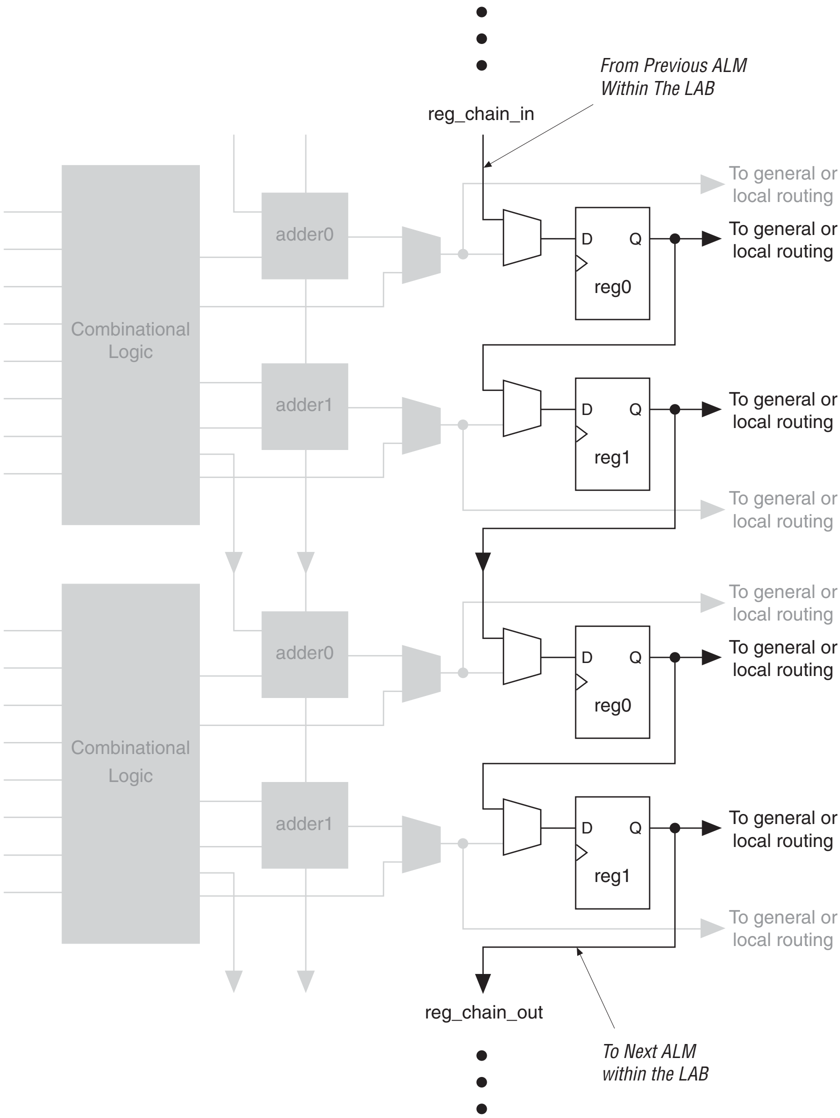
Similar to the carry chains, the shared arithmetic chains are also top- or bottom-half bypassable. This capability allows the shared arithmetic chain to cascade through half of the ALMs in a LAB while leaving the other half available for narrower fan-in functionality. Every other LAB column is top-half bypassable, while the other LAB columns are bottom-half bypassable.

See the "MultiTrack Interconnect" on page 2–22 section for more information on shared arithmetic chain interconnect.

Register Chain

In addition to the general routing outputs, the ALMs in an LAB have register chain outputs. The register chain routing allows registers in the same LAB to be cascaded together. The register chain interconnect allows an LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between ALMs while saving local interconnect resources (see Figure 2–15). The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance.

Figure 2–15. Register Chain within an LAB *Note (1)*



Note to Figure 2–15:

(1) The combinational or adder logic can be utilized to implement an unrelated, un-registered function.

See the "MultiTrack Interconnect" on page 2–22 section for more information on register chain interconnect.

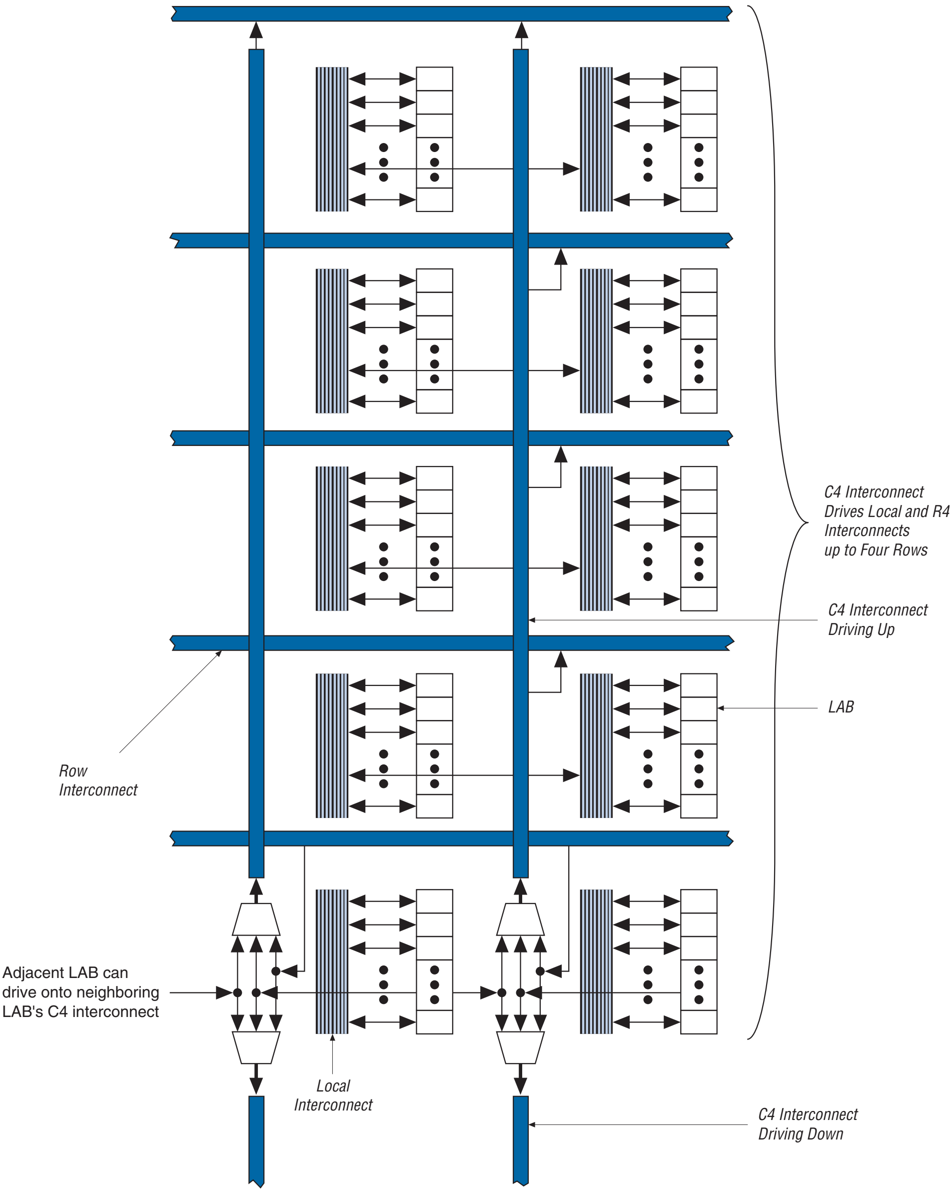
R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and Row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect. These column resources include:

- Shared arithmetic chain interconnects in an LAB
- Carry chain interconnects in an LAB and from LAB to LAB
- Register chain interconnects in an LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix II devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM to ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–17 shows the shared arithmetic chain, carry chain and register chain interconnects.

Figure 2–18. C4 Interconnect Connections *Note (1)*



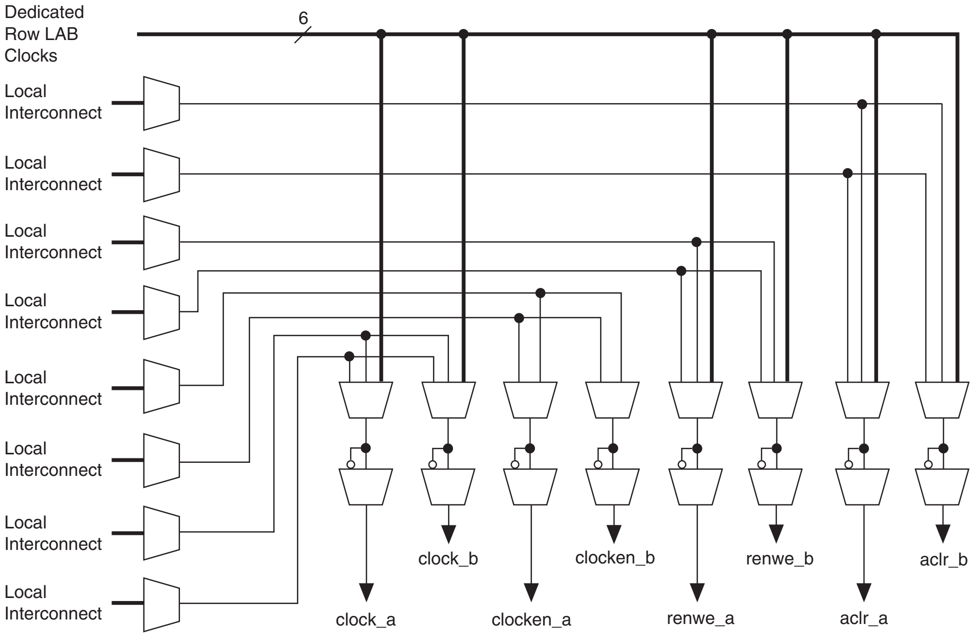
Note to Figure 2–18:

(1) Each C4 interconnect can drive either up or down four rows.

The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (renwe, address, byte enable, datain, and output registers). Only the output register can be bypassed. The six `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–21.

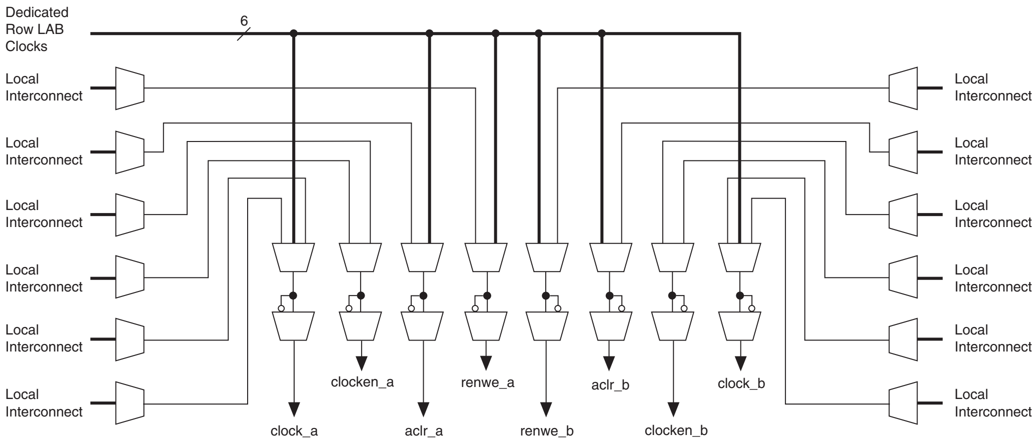
The R4, C4, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K RAM Block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–22 shows the M4K RAM block to logic array interface.

Figure 2–21. M4K RAM Block Control Signals



Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M-RAM block registers (renwe, address, byte enable, datain, and output registers). The output register can be bypassed. The six `labclk` signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals as shown in Figure 2–23.

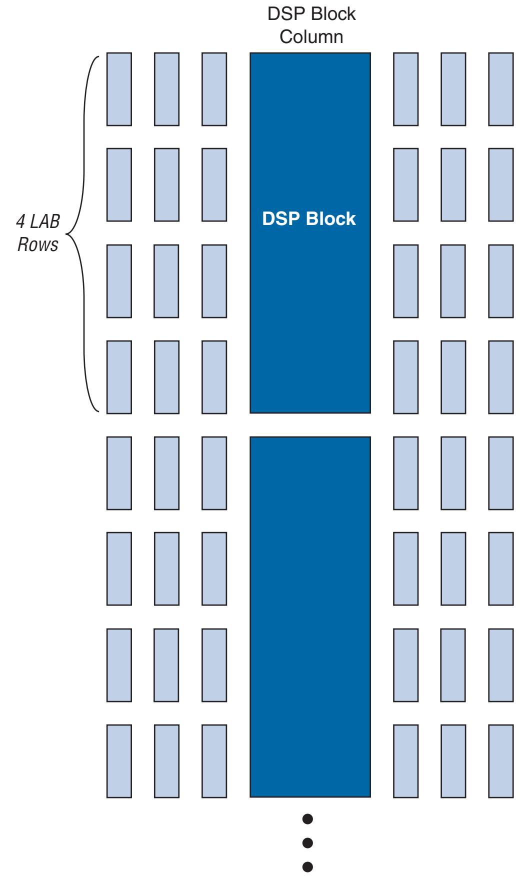
Figure 2–23. M-RAM Block Control Signals



The R4, R24, C4, and direct link interconnects from adjacent LABs on either the right or left side drive the M-RAM block local interconnect. Up to 16 direct link input connections to the M-RAM block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M-RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–24 shows an example floorplan for the EP2S130 device and the location of the M-RAM interfaces. Figures 2–25 and 2–26 show the interface between the M-RAM block and the logic array.

Figure 2–27 shows one of the columns with surrounding LAB rows.

Figure 2–27. DSP Blocks Arranged in Columns



The Stratix II clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all the logic fed by the clock net is in an off-state thereby reducing the overall power consumption of the device.

The global and regional clock networks can be powered down statically through a setting in the configuration (**.sof** or **.pof**) file. Clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software.

The dynamic clock enable/disable feature allows the internal logic to control power up/down synchronously on `GCLK` and `RCLK` nets and `PLL_OUT` pins. This function is independent of the PLL and is applied directly on the clock network or `PLL_OUT` pin, as shown in Figures 2–37 through 2–39.

The following restrictions for the input clock pins apply:

- `CLK0 pin -> inclk[0] of CLKCTRL`
- `CLK1 pin -> inclk[1] of CLKCTRL`
- `CLK2 pin -> inclk[0] of CLKCTRL`
- `CLK3 pin -> inclk[1] of CLKCTRL`

In general, even CLK numbers connect to the `inclk[0]` port of `CLKCTRL`, and odd CLK numbers connect to the `inclk[1]` port of `CLKCTRL`.

Failure to comply with these restrictions will result in a no-fit error.

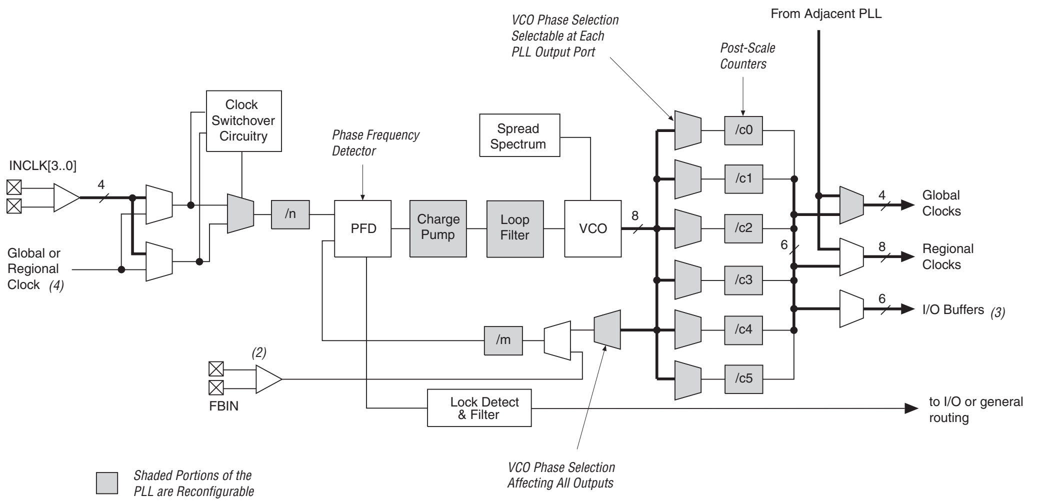
Enhanced & Fast PLLs

Stratix II devices provide robust clock management and synthesis using up to four enhanced PLLs and eight fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock-frequency synthesis. With features such as clock switchover, spread-spectrum clocking, reconfigurable bandwidth, phase control, and reconfigurable phase shifting, the Stratix II device's enhanced PLLs provide you with complete control of clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix II high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

Enhanced PLLs

Stratix II devices contain up to four enhanced PLLs with advanced clock management features. Figure 2–44 shows a diagram of the enhanced PLL.

Figure 2–44. Stratix II Enhanced PLL *Note (1)*



Notes to Figure 2–44:

(1) Each clock source can come from any of the four clock pins that are physically located on the same side of the device as the PLL.

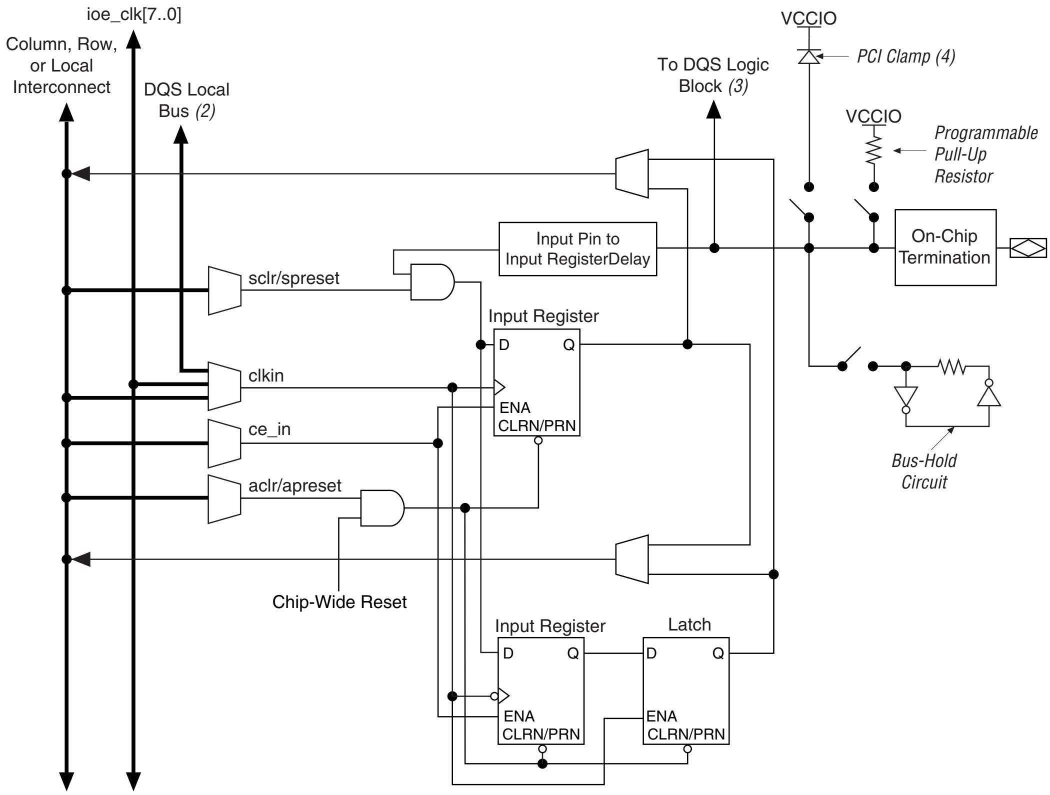
(2) If the feedback input is used, you lose one (or two, if FBIN is differential) external clock output pin.

(3) Each enhanced PLL has three differential external clock outputs or six single-ended external clock outputs.

(4) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used in the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 2–52 shows an IOE configured for DDR input. Figure 2–53 shows the DDR input timing diagram.

Figure 2–52. Stratix II IOE in DDR Input I/O Configuration *Notes (1), (2), (3)*



Notes to Figure 2–52:

(1) All input signals to the IOE can be inverted at the IOE.
(2) This signal connection is only allowed on dedicated DQ function pins.
(3) This signal is for dedicated DQS function pins only.
(4) The optional PCI clamp is only available on column I/O pins.

error status information. This dedicated remote system upgrade circuitry avoids system downtime and is the critical component for successful remote system upgrades.

RSC is supported in the following Stratix II configuration schemes: FPP, AS, PS, and PPA. RSC can also be implemented in conjunction with advanced Stratix II features such as real-time decompression of configuration data and design security using AES for secure and efficient field upgrades.

See the *Remote System Upgrades With Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information about remote configuration in Stratix II devices.

Configuring Stratix II FPGAs with JRunner

JRunner is a software driver that configures Altera FPGAs, including Stratix II FPGAs, through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File **(.rbf)** format. JRunner also requires a Chain Description File **(.cdf)** generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.

For more information on the JRunner software driver, see the *JRunner Software Driver: An Embedded Solution to the JTAG Configuration White Paper* and the source files on the Altera web site **(www.altera.com)**.

Programming Serial Configuration Devices with SRunner

A serial configuration device can be programmed in-system by an external microprocessor using SRunner. SRunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit in different embedded systems. SRunner is able to read a **.rpd** file (Raw Programming Data) and write to the serial configuration devices. The serial configuration device programming time using SRunner is comparable to the programming time when using the Quartus II software.

For more information about SRunner, see the *SRunner: An Embedded Solution for EPCS Programming* White Paper and the source code on the Altera web site at **www.altera.com**.

For more information on programming serial configuration devices, see the Serial Configuration Devices (EPCS1 & EPCS4) Data Sheet in the *Configuration Handbook.*

Table 5–30. Series On-Chip Termination Specification for Top & Bottom I/O Banks (Part 2 of 2) *Notes (1), 2*

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
50-Ω R_S 3.3/2.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	±30	%
50-Ω R_T 2.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
25-Ω R_S 1.8	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_S 1.8	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_T 1.8	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±10	±15	%
50–Ω R_S 1.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±36	±36	%
50-Ω R_T 1.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±10	±15	%
50–Ω R_S 1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±50	±50	%
50-Ω R_T 1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±10	±15	%

Notes for Table 5–30:

(1) The resistance tolerances for calibrated SOCT and POCT are for the moment of calibration. If the temperature or voltage changes over time, the tolerance may also change.

(2) On-chip parallel termination with calibration is only supported for input pins.

Table 5–36. Stratix II Performance Notes (Part 3 of 6) Note (1)

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Unit
DSP block	9 × 9-bit multiplier (5)	0	0	1	430.29	409.16	373.13	320.10	MHz
	18 × 18-bit multiplier (5)	0	0	1	410.17	390.01	356.12	305.06	MHz
	18 × 18-bit multiplier (7)	0	0	1	450.04	428.08	391.23	335.12	MHz
	36 × 36-bit multiplier (5)	0	0	1	250.00	238.15	217.48	186.60	MHz
	36 × 36-bit multiplier (6)	0	0	1	410.17	390.01	356.12	305.06	MHz
	18-bit, four-tap FIR filter	0	0	1	410.17	390.01	356.12	305.06	MHz
Larger designs	8-bit,16-tap parallel FIR filter	58	0	4	259.06	240.61	217.15	185.01	MHz
	8-bit, 1024-point, streaming, three multipliers and five adders FFT function	2976	22	9	398.72	364.03	355.23	306.37	MHz
	8-bit, 1024-point, streaming, four multipliers and two adders FFT function	2781	22	12	398.56	409.16	347.22	311.13	MHz
	8-bit, 1024-point, single output, one parallel FFT engine, burst, three multipliers and five adders FFT function	984	5	3	425.17	365.76	346.98	292.39	MHz
	8-bit, 1024-point, single output, one parallel FFT engine, burst, four multipliers and two adders FFT function	919	5	4	427.53	378.78	357.14	307.59	MHz

Table 5–76. Stratix II I/O Output Delay for Row Pins (Part 2 of 3)

I/O Standard	Drive Strength	Parameter	Minimum Timing Industrial	Minimum Timing Commercial	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
2.5 V	4 mA	t_{OP}	1128	1183	2091	2194	2403	2523	ps
		t_{DIP}	1086	1140	2036	2137	2340	2450	ps
	8 mA	t_{OP}	1030	1080	1872	1964	2152	2265	ps
		t_{DIP}	988	1037	1817	1907	2089	2192	ps
	12 mA *(1)*	t_{OP}	1012	1061	1775	1862	2040	2151	ps
		t_{DIP}	970	1018	1720	1805	1977	2078	ps
1.8 V	2 mA	t_{OP}	1196	1253	2954	3100	3396	3542	ps
		t_{DIP}	1154	1210	2899	3043	3333	3469	ps
	4 mA	t_{OP}	1184	1242	2294	2407	2637	2763	ps
		t_{DIP}	1142	1199	2239	2350	2574	2690	ps
	6 mA	t_{OP}	1079	1131	2039	2140	2344	2462	ps
		t_{DIP}	1037	1088	1984	2083	2281	2389	ps
	8 mA *(1)*	t_{OP}	1049	1100	1942	2038	2232	2348	ps
		t_{DIP}	1007	1057	1887	1981	2169	2275	ps
1.5 V	2 mA	t_{OP}	1158	1213	2530	2655	2908	3041	ps
		t_{DIP}	1116	1170	2475	2598	2845	2968	ps
	4 mA	t_{OP}	1055	1106	2020	2120	2322	2440	ps
		t_{DIP}	1013	1063	1965	2063	2259	2367	ps
SSTL-2 Class I	8 mA	t_{OP}	1002	1050	1759	1846	2022	2104	ps
		t_{DIP}	960	1007	1704	1789	1959	2031	ps
SSTL-2 Class II	16 mA *(1)*	t_{OP}	947	992	1581	1659	1817	1897	ps
		t_{DIP}	905	949	1526	1602	1754	1824	ps
SSTL-18 Class I	4 mA	t_{OP}	990	1038	1709	1793	1964	2046	ps
		t_{DIP}	948	995	1654	1736	1901	1973	ps
	6 mA	t_{OP}	994	1042	1648	1729	1894	1975	ps
		t_{DIP}	952	999	1593	1672	1831	1902	ps
	8 mA	t_{OP}	970	1018	1633	1713	1877	1958	ps
		t_{DIP}	928	975	1578	1656	1814	1885	ps
	10 mA *(1)*	t_{OP}	974	1021	1615	1694	1856	1937	ps
		t_{DIP}	932	978	1560	1637	1793	1864	ps

Table 5–82. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path for -3 Devices Notes (1), (2)

Row DDIO Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS/ HyperTransport Technology	
	3.3 & 2.5 V	1.8 & 1.5 V	2.5 V	1.8 & 1.5 V	3.3 V	
3.3-V LVTTL	260	380	145	145	110	ps
3.3-V LVCMOS	210	330	100	100	65	ps
2.5 V	195	315	85	85	75	ps
1.8 V	150	265	85	85	120	ps
1.5-V LVCMOS	255	370	140	140	105	ps
SSTL-2 Class I	175	295	65	65	70	ps
SSTL-2 Class II	170	290	60	60	75	ps
SSTL-18 Class I	155	275	55	50	90	ps
1.8-V HSTL Class I	150	270	60	60	95	ps
1.5-V HSTL Class I	150	270	55	55	90	ps
LVDS/ HyperTransport technology	180	180	180	180	180	ps

Notes to Table 5–82:

(1) The information in Table 5–82 assumes the input clock has zero DCD.

(2) The DCD specification is based on a no logic array noise condition.

Here is an example for calculating the DCD in percentage for a DDIO output on a row I/O on a -3 device:

If the input I/O standard is SSTL-2 and the DDIO output I/O standard is SSTL-2 Class II, the maximum DCD is 60 ps (see Table 5–82). If the clock frequency is 267 MHz, the clock period T is:

$$T = 1/ f = 1 / 267 \text{ MHz} = 3.745 \text{ ns} = 3745 \text{ ps}$$

Calculate the DCD as a percentage:

$(T/2 – DCD) / T = (3745ps/2 – 60ps) / 3745ps = 48.4\%$ (for low boundary)

$(T/2 + DCD) / T = (3745 ps/2 + 60 ps) / 3745ps = 51.6\%$ (for high boundary)

Table 5–86. Maximum DCD for DDIO Output on Row I/O Pins with PLL in the Clock Path (Part 2 of 2) Note (1)

Row DDIO Output I/O Standard	Maximum DCD (PLL Output Clock Feeding DDIO Clock Port)		Unit
	-3 Device	-4 & -5 Device	
LVDS/ HyperTransport technology	180	180	ps

Note to Table 5–86:
(1) The DCD specification is based on a no logic array noise condition.

Table 5–87. Maximum DCD for DDIO Output on Column I/O with PLL in the Clock Path Note (1)

Column DDIO Output I/O Standard	Maximum DCD (PLL Output Clock Feeding DDIO Clock Port)		Unit
	-3 Device	-4 & -5 Device	
3.3-V LVTTL	145	160	ps
3.3-V LVCMOS	100	110	ps
2.5V	85	95	ps
1.8V	85	100	ps
1.5-V LVCMOS	140	155	ps
SSTL-2 Class I	65	75	ps
SSTL-2 Class II	60	70	ps
SSTL-18 Class I	50	65	ps
SSTL-18 Class II	70	80	ps
1.8-V HSTL Class I	60	70	ps
1.8-V HSTL Class II	60	70	ps
1.5-V HSTL Class I	55	70	ps
1.5-V HSTL Class II	85	100	ps
1.2-V HSTL	155	-	ps
LVPECL	180	180	ps

Notes to Table 5–87:
(1) The DCD specification is based on a no logic array noise condition.
(2) 1.2-V HSTL is only supported in -3 devices.

Table 5–97. DQS Phase Jitter Specifications for DLL-Delayed Clock (tDQS PHASE_JITTER) Note (1)		
Number of DQS Delay Buffer Stages *(2)*	**DQS Phase Jitter**	**Unit**
1	30	ps
2	60	ps
3	90	ps
4	120	ps

Notes to Table 5–97:

(1) Peak-to-peak phase jitter on the phase shifted DDS clock (digital jitter is caused by DLL tracking).

(2) Delay stages used for requested DQS phase shift are reported in your project's Compilation Report in the Quartus II software.

Table 5–98. DQS Phase-Shift Error Specifications for DLL-Delayed Clock (tDQS_PSERR) (1)				
Number of DQS Delay Buffer Stages *(2)*	**–3 Speed Grade**	**–4 Speed Grade**	**–5 Speed Grade**	**Unit**
1	25	30	35	ps
2	50	60	70	ps
3	75	90	105	ps
4	100	120	140	ps

Notes to Table 5–98:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three delay buffer stages in a C3 speed grade is 75 ps or ± 37.5 ps.

(2) Delay stages used for requested DQS phase shift are reported in your project's Compilation Report in the Quartus II software.

Table 5–99. DQS Bus Clock Skew Adder Specifications (tDQS_CLOCK_SKEW_ADDER)		
Mode	**DQS Clock Skew Adder**	**Unit**
×4 DQ per DQS	40	ps
×9 DQ per DQS	70	ps
×18 DQ per DQS	75	ps
×36 DQ per DQS	95	ps

Note to Table 5–99:

(1) This skew specification is the absolute maximum and minimum skew. For example, skew on a ×4 DQ group is 40 ps or ±20 ps.