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Understanding Embedded - FPGAs (Field Programmable Gate Array)

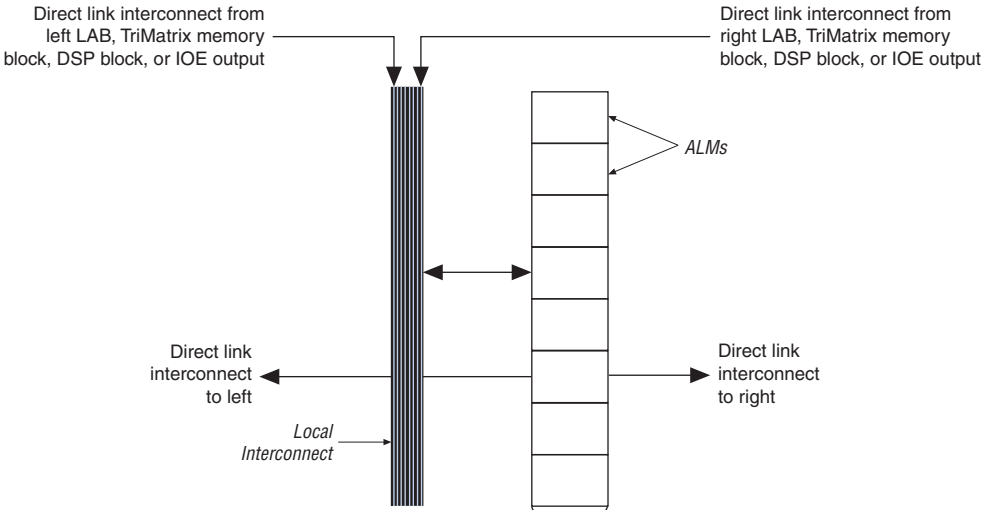
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8970
Number of Logic Elements/Cells	179400
Total RAM Bits	9383040
Number of I/O	1170
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s180f1508c3n

Figure 2–3. Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, and synchronous load control signals. This gives a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2–4. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. By default, the Quartus II software uses a `NOT` gate push-back technique to achieve preset. If you disable the `NOT` gate push-up option or assign a given register to power up high using the Quartus II software, the preset is achieved using the asynchronous load

One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, asynchronous load data, and synchronous and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous load data. The asynchronous load data input comes from the `datae` or `dataf` input of the ALM, which are the same inputs that can be used for register packing. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of the ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers independently (see Figure 2–6). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.

See the *Performance & Logic Efficiency Analysis of Stratix II Devices White Paper* for more information on the efficiencies of the Stratix II ALM and comparisons with previous architectures.

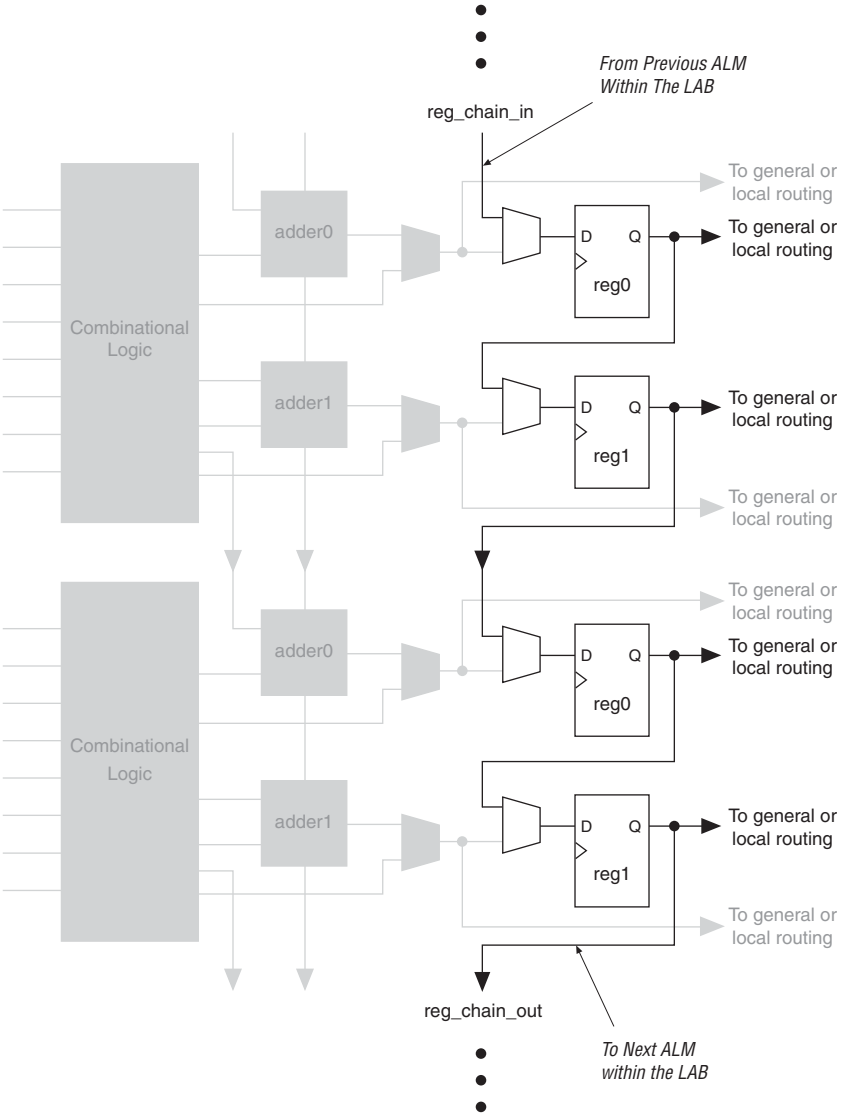
ALM Operating Modes

The Stratix II ALM can operate in one of the following modes:

- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

Each mode uses ALM resources differently. In each mode, eleven available inputs to the ALM--the eight data inputs from the LAB local interconnect; `carry-in` from the previous ALM or LAB; the shared arithmetic chain connection from the previous ALM or LAB; and the register chain connection--are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear,

Figure 2–15. Register Chain within an LAB *Note (1)*



Note to Figure 2–15:
(1) The combinational or adder logic can be utilized to implement an unrelated, un-registered function.

See the "MultiTrack Interconnect" on page 2–22 section for more information on register chain interconnect.

The Stratix II clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all the logic fed by the clock net is in an off-state thereby reducing the overall power consumption of the device.

The global and regional clock networks can be powered down statically through a setting in the configuration (**.sof** or **.pof**) file. Clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software.

The dynamic clock enable/disable feature allows the internal logic to control power up/down synchronously on GCLK and RCLK nets and PLL_OUT pins. This function is independent of the PLL and is applied directly on the clock network or PLL_OUT pin, as shown in Figures 2–37 through 2–39.

The following restrictions for the input clock pins apply:

- CLK0 pin -> inclk[0] of CLKCTRL
- CLK1 pin -> inclk[1] of CLKCTRL
- CLK2 pin -> inclk[0] of CLKCTRL
- CLK3 pin -> inclk[1] of CLKCTRL

In general, even CLK numbers connect to the inclk[0] port of CLKCTRL, and odd CLK numbers connect to the inclk[1] port of CLKCTRL.

Failure to comply with these restrictions will result in a no-fit error.

Enhanced & Fast PLLs

Stratix II devices provide robust clock management and synthesis using up to four enhanced PLLs and eight fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock-frequency synthesis. With features such as clock switchover, spread-spectrum clocking, reconfigurable bandwidth, phase control, and reconfigurable phase shifting, the Stratix II device's enhanced PLLs provide you with complete control of clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix II high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

Table 2–11. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs (Part 2 of 2)

Top Side Global & Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
c4	✓					✓		✓		✓		✓	
c5	✓						✓		✓		✓		✓
Enhanced PLL 11 outputs													
c0		✓	✓			✓				✓			
c1		✓	✓				✓				✓		
c2				✓	✓			✓				✓	
c3				✓	✓				✓				✓
c4						✓		✓		✓		✓	
c5							✓		✓		✓		✓

Table 2–12. Global & Regional Clock Connections from Bottom Clock Pins & Enhanced PLL Outputs (Part 1 of 2)

Bottom Side Global & Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
Clock pins													
CLK4p	✓	✓	✓			✓				✓			
CLK5p	✓	✓	✓				✓				✓		
CLK6p	✓			✓	✓			✓				✓	
CLK7p	✓			✓	✓				✓				✓
CLK4n		✓				✓				✓			
CLK5n			✓				✓				✓		
CLK6n				✓				✓				✓	
CLK7n					✓				✓				✓
Drivers from internal logic													
GCLKDRV0		✓											
GCLKDRV1			✓										
GCLKDRV2				✓									

Table 2–12. Global & Regional Clock Connections from Bottom Clock Pins & Enhanced PLL Outputs (Part 2 of 2)

Bottom Side Global & Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
GCLKDRV3					✓								
RCLKDRV0						✓				✓			
RCLKDRV1							✓				✓		
RCLKDRV2								✓				✓	
RCLKDRV3									✓				✓
RCLKDRV4						✓				✓			
RCLKDRV5							✓				✓		
RCLKDRV6								✓				✓	
RCLKDRV7									✓				✓
Enhanced PLL 6 outputs													
c0	✓	✓	✓			✓				✓			
c1	✓	✓	✓				✓				✓		
c2	✓			✓	✓			✓				✓	
c3	✓			✓	✓				✓				✓
c4	✓					✓		✓		✓		✓	
c5	✓						✓		✓		✓		✓
Enhanced PLL 12 outputs													
c0		✓	✓			✓				✓			
c1		✓	✓				✓				✓		
c2				✓	✓			✓				✓	
c3				✓	✓				✓				✓
c4						✓		✓		✓		✓	
c5							✓		✓		✓		✓

Table 2–27. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
January 2005, v2.0	• Updated the "MultiVolt I/O Interface" and "TriMatrix Memory" sections. • Updated Tables 2–3, 2–17, and 2–19.	—
October 2004, v1.2	• Updated Tables 2–9, 2–16, 2–26, and 2–27.	—
July 2004, v1.1	• Updated note to Tables 2–9 and 2–16. • Updated Tables 2–16, 2–17, 2–18, 2–19, and 2–20. • Updated Figures 2–41, 2–42, and 2–57. • Removed 3 from list of SERDES factor *J*. • Updated "High-Speed Differential I/O with DPA Support" section. • In "Dedicated Circuitry with DPA Support" section, removed XSBI and changed RapidIO to Parallel RapidIO.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

Operating Modes

The Stratix II architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Stratix II devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

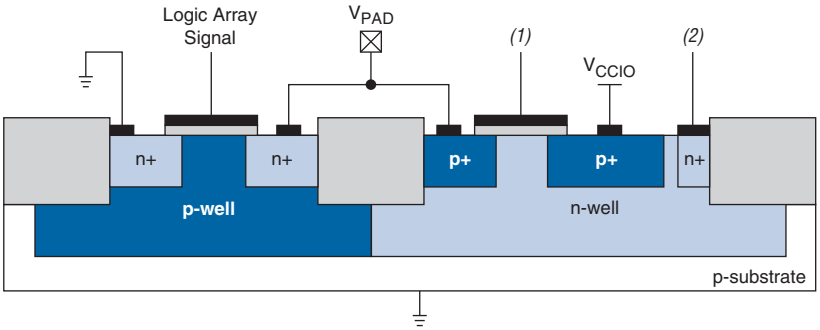
PORSEL is a dedicated input pin used to select POR delay times of 12 ms or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms; when the PORSEL pin is connected to V_{CC}, the POR time is 12 ms.

The nIO PULLUP pin is a dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose configuration I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[2..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLR) are on or off before and during configuration. A logic high (1.5, 1.8, 2.5, 3.3 V) turns off the weak internal pull-ups, while a logic low turns them on.

Stratix II devices also offer a new power supply, V_{CCPD}, which must be connected to 3.3 V in order to power the 3.3-V/2.5-V buffer available on the configuration input pins and JTAG pins. V_{CCPD} applies to all the JTAG input pins (TCK, TMS, TDI, and TRST) and the configuration input pins when VCCSEL is connected to ground. See Table 3–4 for more information on the pins affected by VCCSEL.

The VCCSEL pin allows the V_{CCIO} setting (of the banks where the configuration inputs reside) to be independent of the voltage required by the configuration inputs. Therefore, when selecting the V_{CCIO}, the V_{IL} and V_{IH} levels driven to the configuration inputs do not have to be a concern.

Figure 4–2. Transistor Level Diagram of FPGA Device I/O Buffers



Notes to Figure 4–2:
(1) This is the logic array signal or the larger of either the V_{CCIO} or V_{PAD} signal.
(2) This is the larger of either the V_{CCIO} or V_{PAD} signal.

Power-On Reset Circuitry

Stratix II devices have a POR circuit to keep the whole device system in reset state until the power supply voltage levels have stabilized during power-up. The POR circuit monitors the V_{CCINT}, V_{CCIO}, and V_{CCPD} voltage levels and tri-states all the user I/O pins while V_{CC} is ramping up until normal user levels are reached. The POR circuitry also ensures that all eight I/O bank V_{CCIO} voltages, V_{CCPD} voltage, as well as the logic array V_{CCINT} voltage, reach an acceptable level before configuration is triggered. After the Stratix II device enters user mode, the POR circuit continues to monitor the V_{CCINT} voltage level so that a brown-out condition during user mode can be detected. If there is a V_{CCINT} voltage sag below the Stratix II operational level during user mode, the POR circuit resets the device.

When power is applied to a Stratix II device, a power-on-reset event occurs if V_{CC} reaches the recommended operating range within a certain period of time (specified as a maximum V_{CC} rise time). The maximum V_{CC} rise time for Stratix II device is 100 ms. Stratix II devices provide a dedicated input pin (PORSEL) to select POR delay times of 12 or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms. When the PORSEL pin is connected to V_{CC}, the POR time is 12 ms.

Table 5–4. Stratix II Device DC Operating Conditions (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions		Minimum	Typical	Maximum	Unit
I_{CCI00}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25° C	EP2S15		4.0	*(3)*	mA
			EP2S30		4.0	*(3)*	mA
			EP2S60		4.0	*(3)*	mA
			EP2S90		4.0	*(3)*	mA
			EP2S130		4.0	*(3)*	mA
			EP2S180		4.0	*(3)*	mA
R_{CONF} *(4)*	Value of I/O pin pull-up resistor before and during configuration	Vi = 0; V_{CCIO} = 3.3 V		10	25	50	kΩ
		Vi = 0; V_{CCIO} = 2.5 V		15	35	70	kΩ
		Vi = 0; V_{CCIO} = 1.8 V		30	50	100	kΩ
		Vi = 0; V_{CCIO} = 1.5 V		40	75	150	kΩ
		Vi = 0; V_{CCIO} = 1.2 V		50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration				1	2	kΩ

Notes to Table 5–4:

(1) Typical values are for T_A = 25°C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(3) Maximum values depend on the actual T_J and design utilization. See the Excel-based PowerPlay Early Power Estimator (available at **www.altera.com**) or the Quartus II PowerPlay Power Analyzer feature for maximum values. See the section "Power Consumption" on page 5–20 for more information.

(4) Pin pull-up resistance values are lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Tables 5–5 through 5–32 show the Stratix II device family I/O standard specifications.

Table 5–5. LVTTL Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		3.135	3.465	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(2)*	2.4		V

Table 5–19. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.500	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.188	1.250	1.313	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.18		3.00	V
V_{IL} (DC)	Low-level DC input voltage		–0.30		V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.35			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} - 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(1)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(1)*			V_{TT} – 0.57	V

Note to Table 5–19:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–20. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.500	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.188	1.250	1.313	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.18		V_{CCIO} + 0.30	V
V_{IL} (DC)	Low-level DC input voltage		–0.30		V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.35			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} - 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(1)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(1)*			V_{TT} – 0.76	V

Note to Table 5–20:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–30. Series On-Chip Termination Specification for Top & Bottom I/O Banks (Part 2 of 2)
Notes (1), 2

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
50-Ω R_S 3.3/2.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	±30	%
50-Ω R_T 2.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
25-Ω R_S 1.8	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_S 1.8	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_T 1.8	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±10	±15	%
50–Ω R_S 1.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±36	±36	%
50-Ω R_T 1.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±10	±15	%
50–Ω R_S 1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±50	±50	%
50-Ω R_T 1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±10	±15	%

Notes for Table 5–30:
(1) The resistance tolerances for calibrated SOCT and POCT are for the moment of calibration. If the temperature or voltage changes over time, the tolerance may also change.
(2) On-chip parallel termination with calibration is only supported for input pins.

Table 5–36. Stratix II Performance Notes (Part 2 of 6) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
TriMatrix Memory M-RAM block	Single port RAM 4K × 144 bit	0	1	0	349.65	333.33	303.95	261.09	MHz
	Simple dual-port RAM 4K × 144 bit	0	1	0	420.16	400.00	364.96	313.47	MHz
	True dual-port RAM 4K × 144 bit	0	1	0	349.65	333.33	303.95	261.09	MHz
	Single port RAM 8K × 72 bit	0	1	0	354.60	337.83	307.69	263.85	MHz
	Simple dual-port RAM 8K × 72 bit	0	1	0	420.16	400.00	364.96	313.47	MHz
	True dual-port RAM 8K × 72 bit	0	1	0	349.65	333.33	303.95	261.09	MHz
	Single port RAM 16K × 36 bit	0	1	0	364.96	347.22	317.46	271.73	MHz
	Simple dual-port RAM 16K × 36 bit	0	1	0	420.16	400.00	364.96	313.47	MHz
	True dual-port RAM 16K × 36 bit	0	1	0	359.71	342.46	313.47	268.09	MHz
	Single port RAM 32K × 18 bit	0	1	0	364.96	347.22	317.46	271.73	MHz
	Simple dual-port RAM 32K × 18 bit	0	1	0	420.16	400.0	364.96	313.47	MHz
	True dual-port RAM 32K × 18 bit	0	1	0	359.71	342.46	313.47	268.09	MHz
	Single port RAM 64K × 9 bit	0	1	0	364.96	347.22	317.46	271.73	MHz
	Simple dual-port RAM 64K × 9 bit	0	1	0	420.16	400.0	364.96	313.47	MHz
	True dual-port RAM 64K × 9 bit	0	1	0	359.71	342.46	313.47	268.09	MHz

I/O Delays

See Tables 5–72 through 5–76 for I/O delays.

Table 5–72. I/O Delay Parameters

Symbol	Parameter
t_{DIP}	Delay from I/O datain to output pad
t_{OP}	Delay from I/O output register to output pad
t_{PCOUT}	Delay from input pad to I/O dataout to core
t_{PI}	Delay from input pad to I/O input register

Table 5–73. Stratix II I/O Input Delay for Column Pins (Part 1 of 3)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
LVTTL	t_{PI}	674	707	1223	1282	1405	1637	ps
	t_{PCOUT}	408	428	787	825	904	1054	ps
2.5 V	t_{PI}	684	717	1210	1269	1390	1619	ps
	t_{PCOUT}	418	438	774	812	889	1036	ps
1.8 V	t_{PI}	747	783	1366	1433	1570	1829	ps
	t_{PCOUT}	481	504	930	976	1069	1246	ps
1.5 V	t_{PI}	749	786	1436	1506	1650	1922	ps
	t_{PCOUT}	483	507	1000	1049	1149	1339	ps
LVCMOS	t_{PI}	674	707	1223	1282	1405	1637	ps
	t_{PCOUT}	408	428	787	825	904	1054	ps
SSTL-2 Class I	t_{PI}	507	530	818	857	939	1094	ps
	t_{PCOUT}	241	251	382	400	438	511	ps
SSTL-2 Class II	t_{PI}	507	530	818	857	939	1094	ps
	t_{PCOUT}	241	251	382	400	438	511	ps
SSTL-18 Class I	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
SSTL-18 Class II	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.5-V HSTL Class I	t_{PI}	560	587	993	1041	1141	1329	ps
	t_{PCOUT}	294	308	557	584	640	746	ps

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 2 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
LVCMOS	4 mA	t_{OP}	1041	1091	2036	2136	2340	2448	ps
		t_{DIP}	1061	1113	2102	2206	2416	2538	ps
	8 mA	t_{OP}	952	999	1786	1874	2053	2153	ps
		t_{DIP}	972	1021	1852	1944	2129	2243	ps
	12 mA	t_{OP}	926	971	1720	1805	1977	2075	ps
		t_{DIP}	946	993	1786	1875	2053	2165	ps
	16 mA	t_{OP}	933	978	1693	1776	1946	2043	ps
		t_{DIP}	953	1000	1759	1846	2022	2133	ps
	20 mA	t_{OP}	921	965	1677	1759	1927	2025	ps
		t_{DIP}	941	987	1743	1829	2003	2115	ps
	24 mA (1)	t_{OP}	909	954	1659	1741	1906	2003	ps
		t_{DIP}	929	976	1725	1811	1982	2093	ps
2.5 V	4 mA	t_{OP}	1004	1053	2063	2165	2371	2480	ps
		t_{DIP}	1024	1075	2129	2235	2447	2570	ps
	8 mA	t_{OP}	955	1001	1841	1932	2116	2218	ps
		t_{DIP}	975	1023	1907	2002	2192	2308	ps
	12 mA	t_{OP}	934	980	1742	1828	2002	2101	ps
		t_{DIP}	954	1002	1808	1898	2078	2191	ps
	16 mA (1)	t_{OP}	918	962	1679	1762	1929	2027	ps
		t_{DIP}	938	984	1745	1832	2005	2117	ps

Therefore, the DCD percentage for the 267 MHz SSTL-2 Class II non-DDIO row output clock on a –3 device ranges from 47.5% to 52.5%.

Table 5–81. Maximum DCD for Non-DDIO Output on Column I/O Pins *Note (1)*

Column I/O Output Standard I/O Standard	Maximum DCD for Non-DDIO Output		Unit
	-3 Devices	-4 & -5 Devices	
3.3-V LVTTL	190	220	ps
3.3-V LVCMOS	140	175	ps
2.5 V	125	155	ps
1.8 V	80	110	ps
1.5-V LVCMOS	185	215	ps
SSTL-2 Class I	105	135	ps
SSTL-2 Class II	100	130	ps
SSTL-18 Class I	90	115	ps
SSTL-18 Class II	70	100	ps
1.8-V HSTL Class I	80	110	ps
1.8-V HSTL Class II	80	110	ps
1.5-V HSTL Class I	85	115	ps
1.5-V HSTL Class II	50	80	ps
1.2-V HSTL *(2)*	170	-	ps
LVPECL	55	80	ps

Notes to Table 5–81:
(1) The DCD specification is based on a no logic array noise condition.
(2) 1.2-V HSTL is only supported in -3 devices.

Table 5–84. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 2 of 2) *Notes (1), (2)*

DDIO Column Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	1.2-V HSTL	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	1.2 V	
1.8 V	150	265	85	85	85	ps
1.5-V LVCMOS	255	370	140	140	140	ps
SSTL-2 Class I	175	295	65	65	65	ps
SSTL-2 Class II	170	290	60	60	60	ps
SSTL-18 Class I	155	275	55	50	50	ps
SSTL-18 Class II	140	260	70	70	70	ps
1.8-V HSTL Class I	150	270	60	60	60	ps
1.8-V HSTL Class II	150	270	60	60	60	ps
1.5-V HSTL Class I	150	270	55	55	55	ps
1.5-V HSTL Class II	125	240	85	85	85	ps
1.2-V HSTL	240	360	155	155	155	ps
LVPECL	180	180	180	180	180	ps

Notes to Table 5–84:
(1) Table 5–84 assumes the input clock has zero DCD.
(2) The DCD specification is based on a no logic array noise condition.

Table 5–85. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -4 & -5 Devices (Part 1 of 2) *Notes (1), (2)*

DDIO Column Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)				Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	
3.3-V LVTTL	440	495	170	160	ps
3.3-V LVCMOS	390	450	120	110	ps
2.5 V	375	430	105	95	ps
1.8 V	325	385	90	100	ps
1.5-V LVCMOS	430	490	160	155	ps
SSTL-2 Class I	355	410	85	75	ps
SSTL-2 Class II	350	405	80	70	ps

Table 5–85. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -4 & -5 Devices (Part 2 of 2) *Notes (1), (2)*

DDIO Column Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)				Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	
SSTL-18 Class I	335	390	65	65	ps
SSTL-18 Class II	320	375	70	80	ps
1.8-V HSTL Class I	330	385	60	70	ps
1.8-V HSTL Class II	330	385	60	70	ps
1.5-V HSTL Class I	330	390	60	70	ps
1.5-V HSTL Class II	330	360	90	100	ps
1.2-V HSTL	420	470	155	165	ps
LVPECL	180	180	180	180	ps

Notes to Table 5–85:
(1) Table 5–85 assumes the input clock has zero DCD.
(2) The DCD specification is based on a no logic array noise condition.

Table 5–86. Maximum DCD for DDIO Output on Row I/O Pins with PLL in the Clock Path (Part 1 of 2) *Note (1)*

Row DDIO Output I/O Standard	Maximum DCD (PLL Output Clock Feeding DDIO Clock Port)		Unit
	-3 Device	-4 & -5 Device	
3.3-V LVTTL	110	105	ps
3.3-V LVCMOS	65	75	ps
2.5V	75	90	ps
1.8V	85	100	ps
1.5-V LVCMOS	105	100	ps
SSTL-2 Class I	65	75	ps
SSTL-2 Class II	60	70	ps
SSTL-18 Class I	50	65	ps
1.8-V HSTL Class I	50	70	ps
1.5-V HSTL Class I	55	70	ps

High-Speed I/O Specifications

Table 5–88 provides high-speed timing specifications definitions.

Table 5–88. High-Speed Timing Specifications & Definitions

High-Speed Timing Specifications	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
J	Deserialization factor (width of parallel data bus).
W	PLL multiplication factor.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter	Peak-to-peak input jitter on high-speed PLLs.
Output jitter	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Table 5–89 shows the high-speed I/O timing specifications for -3 speed grade Stratix II devices.

Table 5–89. High-Speed I/O Specifications for -3 Speed Grade (Part 1 of 2) *Notes (1), (2)*

Symbol	Conditions	-3 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (clock frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*	16		520	MHz
	W = 1 (SERDES bypass, LVDS only)	16		500	MHz
	W = 1 (SERDES used, LVDS only)	150		717	MHz

Table 5–93. Fast PLL Specifications

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (for -3 and -4 speed grade devices)	16.08		717	MHz
	Input clock frequency (for -5 speed grade devices)	16.08		640	MHz
f_{INPFD}	Input frequency to the PFD	16.08		500	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$t_{INJITTER}$	Input clock jitter tolerance in terms of period jitter. Bandwidth ≤ 2 MHz		0.5		ns (p-p)
	Input clock jitter tolerance in terms of period jitter. Bandwidth > 2 MHz		1.0		ns (p-p)
f_{VCO}	Upper VCO frequency range for –3 and –4 speed grades	300		1,040	MHz
	Upper VCO frequency range for –5 speed grades	300		840	MHz
	Lower VCO frequency range for –3 and –4 speed grades	150		520	MHz
	Lower VCO frequency range for –5 speed grades	150		420	MHz
f_{OUT}	PLL output frequency to GCLK or RCLK	4.6875		550	MHz
	PLL output frequency to LVDS or DPA clock	150		1,040	MHz
f_{OUT_IO}	PLL clock output frequency to regular I/O pin	4.6875		*(1)*	MHz
$f_{SCANCLK}$	Scanclk frequency			100	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for fast PLLs		$75/f_{SCANCLK}$		ns
f_{CLBW}	PLL closed-loop bandwidth	1.16	5.00	28.00	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of the device configuration		0.03	1.00	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift			±15	ps
t_{ARESET}	Minimum pulse width on areset signal.	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scandone goes high.	500			ns

Note to Table 5–93:
(1) Limited by I/O f_{MAX}. See Table 5–77 on page 5–67 for the maximum.