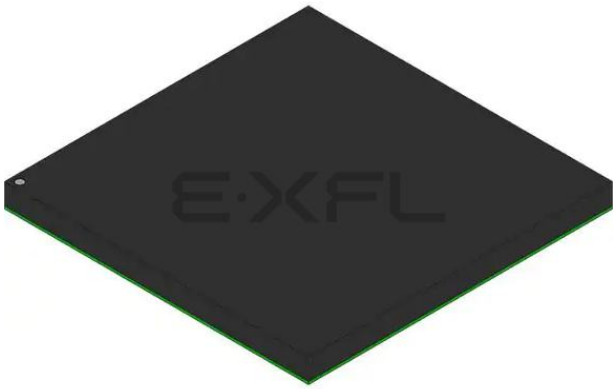


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	8970
Number of Logic Elements/Cells	179400
Total RAM Bits	9383040
Number of I/O	1170
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2s180f1508c4n

Chapter 3. Configuration & Testing

Chapter 4. Hot Socketing & Power-On Reset

Chapter 5. DC & Switching Characteristics

Stratix II devices are available in space-saving FineLine BGA® packages (see Tables 1–2 and 1–3).

Table 1–2. Stratix II Package Options & I/O Pin Counts *Notes (1), (2)*

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	342		366			
EP2S30	342		500			
EP2S60 *(3)*	334		492		718	
EP2S90 *(3)*		308		534	758	902
EP2S130 *(3)*				534	742	1,126
EP2S180 *(3)*					742	1,170

Notes to Table 1–2:

(1) All I/O pin counts include eight dedicated clock input pins (`clk1p`, `clk1n`, `clk3p`, `clk3n`, `clk9p`, `clk9n`, `clk11p`, and `clk11n`) that can be used for data inputs.

(2) The Quartus II software I/O pin counts include one additional pin, `PLL_ENA`, which is not available as general-purpose I/O pins. The `PLL_ENA` pin can only be used to enable the PLLs within the device.

(3) The I/O pin counts for the EP2S60, EP2S90, EP2S130, and EP2S180 devices in the 1020-pin and 1508-pin packages include eight dedicated fast PLL clock inputs (`FPLL7CLKp/n`, `FPLL8CLKp/n`, `FPLL9CLKp/n`, and `FPLL10CLKp/n`) that can be used for data inputs.

Table 1–3. Stratix II FineLine BGA Package Sizes

Dimension	484 Pin	484-Pin Hybrid	672 Pin	780 Pin	1,020 Pin	1,508 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00
Area (mm2)	529	729	729	841	1,089	1,600
Length × width (mm × mm)	23 × 23	27 × 27	27 × 27	29 × 29	33 × 33	40 × 40

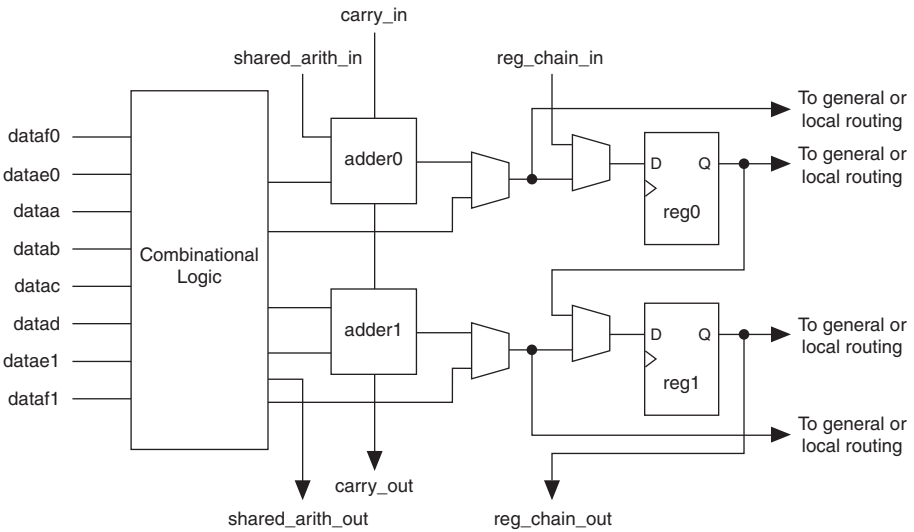
All Stratix II devices support vertical migration within the same package (for example, you can migrate between the EP2S15, EP2S30, and EP2S60 devices in the 672-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

To ensure that a board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus II software (Assignments menu > Device > Migration Devices).

completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–5 shows a high-level block diagram of the Stratix II ALM while Figure 2–6 shows a detailed view of all the connections in the ALM.

Figure 2–5. High-Level Block Diagram of the Stratix II ALM



Clear & Preset Logic Control

LAB-wide signals control the logic for the register's clear and load/preset signals. The ALM directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. Stratix II devices support simultaneous asynchronous load/preset, and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one load/preset signal.

In addition to the clear and load/preset ports, Stratix II devices provide a device-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This device-wide reset overrides all other control signals.

MultiTrack Interconnect

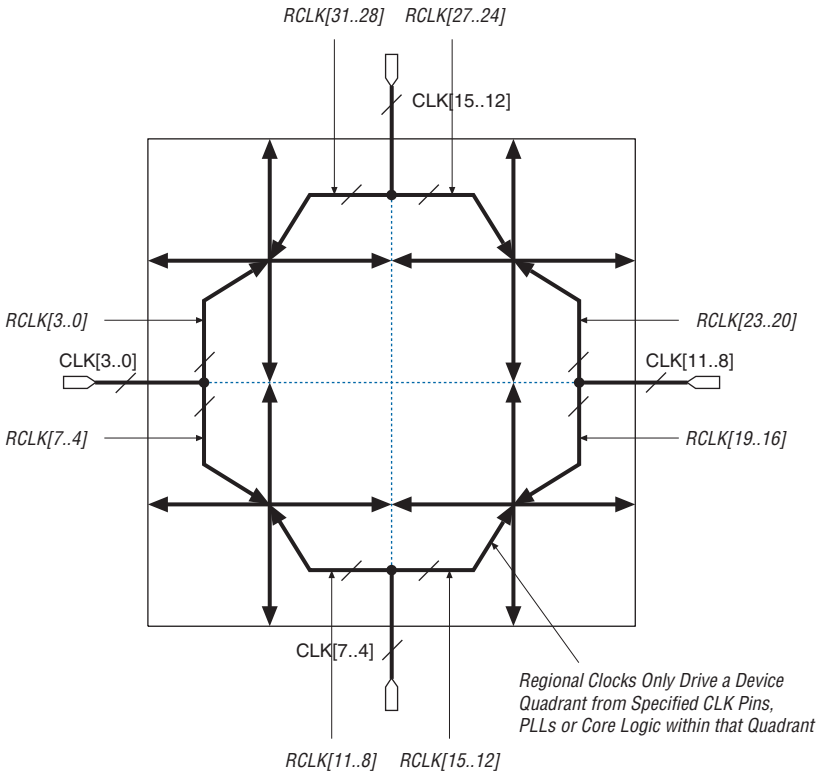
In the Stratix II architecture, connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory in the same row. These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 row interconnects for high-speed access across the length of the device

Figure 2–32. Regional Clocks



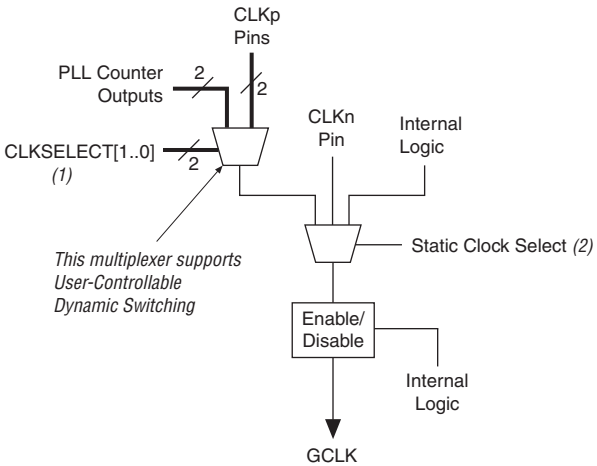
Dual-Regional Clock Network

A single source (CLK pin or PLL output) can generate a dual-regional clock by driving two regional clock network lines in adjacent quadrants (one from each quadrant). This allows logic that spans multiple quadrants to utilize the same low skew clock. The routing of this clock signal on an entire side has approximately the same speed but slightly higher clock skew when compared with a clock signal that drives a single quadrant. Internal logic-array routing can also drive a dual-regional clock. Clock pins and enhanced PLL outputs on the top and bottom can drive horizontal dual-regional clocks. Clock pins and fast PLL outputs on the left and right can drive vertical dual-regional clocks, as shown in Figure 2–33. Corner PLLs cannot drive dual-regional clocks.

When using the global or regional clock control blocks in Stratix II devices to select between multiple clocks or to enable and disable clock networks, be aware of possible narrow pulses or glitches when switching from one clock signal to another. A glitch or runt pulse has a width that is less than the width of the highest frequency input clock signal. To prevent logic errors within the FPGA, Altera recommends that you build circuits that filter out glitches and runt pulses.

Figures 2–37 through 2–39 show the clock control block for the global clock, regional clock, and PLL external clock output, respectively.

Figure 2–37. Global Clock Control Blocks



Notes to Figure 2–37:

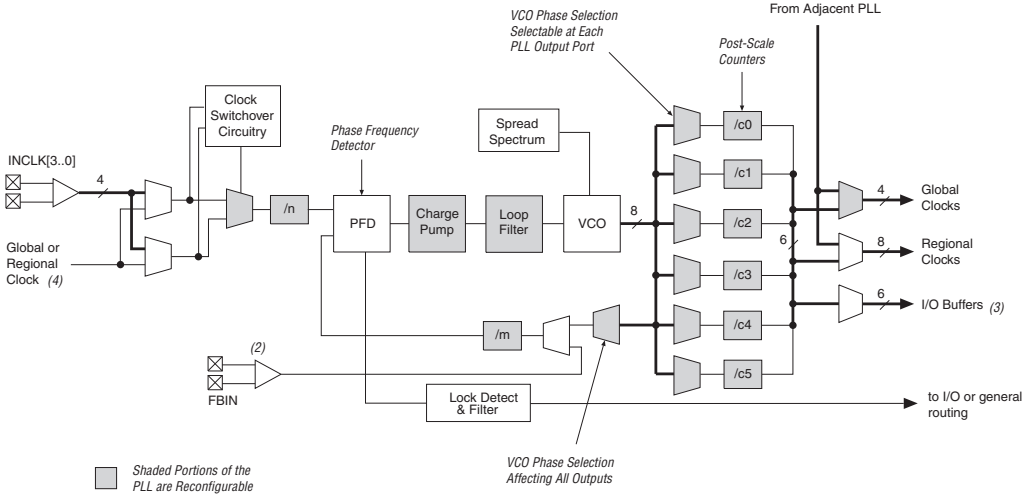
(1) These clock select signals can be dynamically controlled through internal logic when the device is operating in user mode.

(2) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

Enhanced PLLs

Stratix II devices contain up to four enhanced PLLs with advanced clock management features. Figure 2–44 shows a diagram of the enhanced PLL.

Figure 2–44. Stratix II Enhanced PLL *Note (1)*



Notes to Figure 2–44:

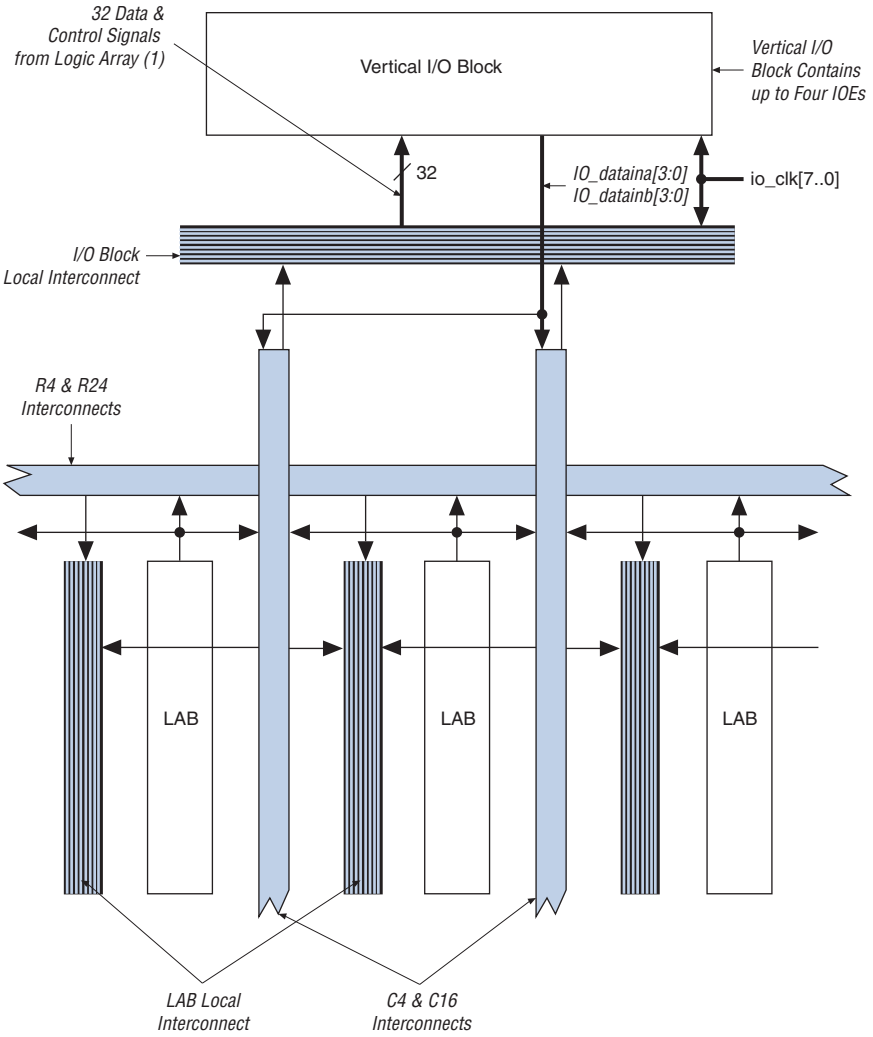
(1) Each clock source can come from any of the four clock pins that are physically located on the same side of the device as the PLL.

(2) If the feedback input is used, you lose one (or two, if FBIN is differential) external clock output pin.

(3) Each enhanced PLL has three differential external clock outputs or six single-ended external clock outputs.

(4) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

Figure 2–48. Column I/O Block Connection to the Interconnect *Note (1)*



Note to Figure 2–48:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

Table 2–14. DQS & DQ Bus Mode Support (Part 2 of 2) *Note (1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2S90	484-pin Hybrid FineLine BGA	8	4	0	0
	780-pin FineLine BGA	18	8	4	0
	1,020-pin FineLine BGA	36	18	8	4
	1,508-pin FineLine BGA	36	18	8	4
EP2S130	780-pin FineLine BGA	18	8	4	0
	1,020-pin FineLine BGA	36	18	8	4
	1,508-pin FineLine BGA	36	18	8	4
EP2S180	1,020-pin FineLine BGA	36	18	8	4
	1,508-pin FineLine BGA	36	18	8	4

Notes to Table 2–14:
(1) Check the pin table for each DQS/DQ group in the different modes.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

The Stratix II device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed the phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits.

Figure 2–56 illustrates the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Table 3–7. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
April 2006, v4.1	Updated "Device Security Using Configuration Bitstream Encryption" section.	—
December 2005, v4.0	Updated "Software Interface" section.	—
May 2005, v3.0	• Updated "IEEE Std. 1149.1 JTAG Boundary-Scan Support" section. • Updated "Operating Modes" section.	—
January 2005, v2.1	Updated JTAG chain device limits.	—
January 2005, v2.0	Updated Table 3–3.	—
July 2004, v1.1	• Added "Automated Single Event Upset (SEU) Detection" section. • Updated "Device Security Using Configuration Bitstream Encryption" section. • Updated Figure 3–2.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

5. DC & Switching Characteristics

SII51005-4.5

Operating Conditions

Stratix® II devices are offered in both commercial and industrial grades. Industrial devices are offered in -4 speed grades and commercial devices are offered in -3 (fastest), -4, -5 speed grades.

Tables 5–1 through 5–32 provide information about absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for Stratix II devices.

Absolute Maximum Ratings

Table 5–1 contains the absolute maximum ratings for the Stratix II device family.

Table 5–1. Stratix II Device Absolute Maximum Ratings *Notes (1), (2), (3)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Supply voltage	With respect to ground	–0.5	4.6	V
V_{CCPD}	Supply voltage	With respect to ground	–0.5	4.6	V
V_{CCA}	Analog power supply for PLLs	With respect to ground	–0.5	1.8	V
V_{CCD}	Digital power supply for PLLs	With respect to ground	–0.5	1.8	V
V_I	DC input voltage *(4)*		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_J	Junction temperature	BGA packages under bias	–55	125	°C

Notes to Tables 5–1

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Conditions beyond those listed in Table 5–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.
(3) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.
(4) During transitions, the inputs may overshoot to the voltage shown in Table 5–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Figure 5–1. Receiver Input Waveforms for Differential I/O Standards

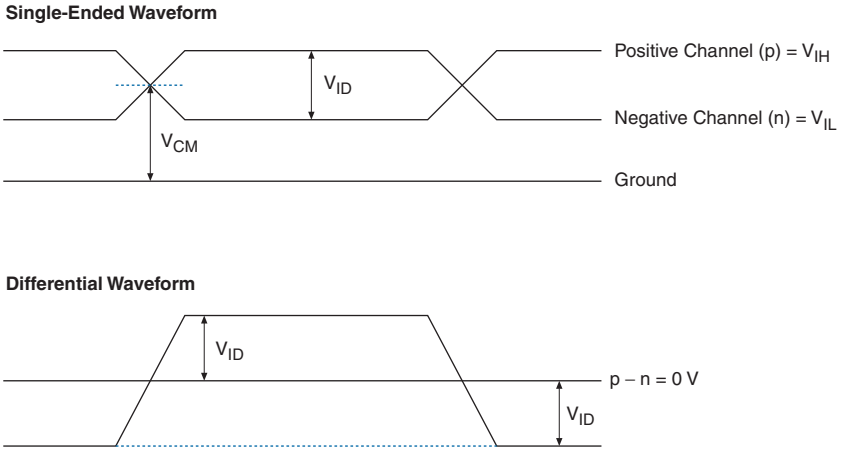


Figure 5–2. Transmitter Output Waveforms for Differential I/O Standards

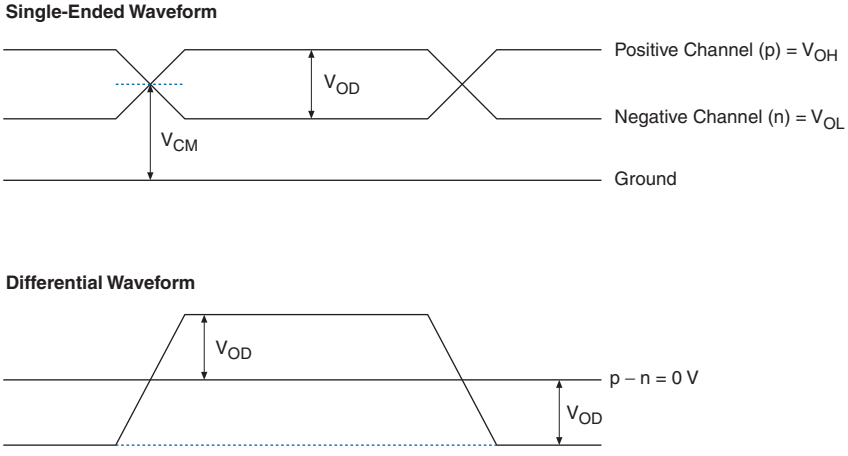


Table 5–25. 1.5-V HSTL Class I & II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.425	1.500	1.575	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.90	V
V_{DIF} (AC)	AC differential input voltage		0.4			V
V_{OX} (AC)	AC differential cross point voltage		0.68		0.90	V

Table 5–26. 1.8-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Input reference voltage		0.85	0.90	0.95	V
V_{TT}	Termination voltage		0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 5–26:

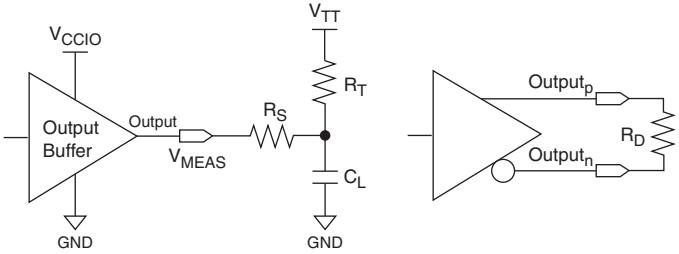
(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

4. Record the time to V_{MEAS}.

5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-output) of the PCB trace.

The Quartus II software reports the timing with the conditions shown in Table 5–34 using the above equation. Figure 5–4 shows the model of the circuit that is represented by the output timing of the Quartus II software.

Figure 5–4. Output Delay Timing Reporting Setup Modeled by Quartus II



Notes to Figure 5–4:

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.

(2) V_{CCPD} is 3.085 V unless otherwise specified.

(3) V_{CCINT} is 1.12 V unless otherwise specified.

Figures 5–5 and 5–6 show the measurement setup for output disable and output enable timing.

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 2 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
1.8-V LVTTL/LVCMOS	2 mA	951	1421	1421	951	1421	1421	904	1421	1421
	4 mA	405	516	516	405	516	516	393	516	516
	6 mA	261	325	325	261	325	325	253	325	325
	8 mA	223	274	274	223	274	274	224	274	274
	10 mA	194	236	236	-	-	-	199	236	236
	12 mA	174	209	209	-	-	-	180	209	209
1.5-V LVTTL/LVCMOS	2 mA	652	963	963	652	963	963	618	963	963
	4 mA	333	347	347	333	347	347	270	347	347
	6 mA	182	247	247	-	-	-	198	247	247
	8 mA	135	194	194	-	-	-	155	194	194
SSTL-2 Class I	8 mA	364	680	680	364	680	680	350	680	680
	12 mA	163	207	207	163	207	207	188	207	207
SSTL-2 Class II	16 mA	118	147	147	118	147	147	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116
SSTL-18 Class I	4 mA	458	570	570	458	570	570	505	570	570
	6 mA	305	380	380	305	380	380	336	380	380
	8 mA	225	282	282	225	282	282	248	282	282
	10 mA	167	220	220	167	220	220	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175
SSTL-18 Class II	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
SSTL-2 Class I	8 mA	364	680	680	364	680	680	350	680	680
	12 mA	163	207	207	163	207	207	188	207	207
SSTL-2 Class II	16 mA	118	147	147	118	147	147	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 4 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
Differential SSTL-18 Class I *(3)*	4 mA	458	570	570	-	-	-	505	570	570
	6 mA	305	380	380	-	-	-	336	380	380
	8 mA	225	282	282	-	-	-	248	282	282
	10 mA	167	220	220	-	-	-	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175
Differential SSTL-18 Class II *(3)*	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
1.8-V Differential HSTL Class I *(3)*	4 mA	245	282	282	-	-	-	229	282	282
	6 mA	164	188	188	-	-	-	153	188	188
	8 mA	123	140	140	-	-	-	114	140	140
	10 mA	110	124	124	-	-	-	108	124	124
	12 mA	97	110	110	-	-	-	104	110	110
1.8-V Differential HSTL Class II *(3)*	16 mA	101	104	104	-	-	-	99	104	104
	18 mA	98	102	102	-	-	-	93	102	102
	20 mA	93	99	99	-	-	-	88	99	99
1.5-V Differential HSTL Class I *(3)*	4 mA	168	196	196	-	-	-	188	196	196
	6 mA	112	131	131	-	-	-	125	131	131
	8 mA	84	99	99	-	-	-	95	99	99
	10 mA	87	98	98	-	-	-	90	98	98
	12 mA	86	98	98	-	-	-	87	98	98
1.5-V Differential HSTL Class II *(3)*	16 mA	95	101	101	-	-	-	96	101	101
	18 mA	95	100	100	-	-	-	101	100	100
	20 mA	94	101	101	-	-	-	104	101	101
3.3-V PCI		134	177	177	-	-	-	143	177	177
3.3-V PCI-X		134	177	177	-	-	-	143	177	177
LVDS		-	-	-	155 *(1)*	155 *(1)*	155 *(1)*	134	134	134
HyperTransport technology		-	-	-	155 *(1)*	155 *(1)*	155 *(1)*	-	-	-
LVPECL *(4)*		-	-	-	-	-	-	134	134	134

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 5 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVTTL	OCT 50 Ω	133	152	152	133	152	152	147	152	152
2.5-V LVTTL	OCT 50 Ω	207	274	274	207	274	274	235	274	274
1.8-V LVTTL	OCT 50 Ω	151	165	165	151	165	165	153	165	165
3.3-V LVCMOS	OCT 50 Ω	300	316	316	300	316	316	263	316	316
1.5-V LVCMOS	OCT 50 Ω	157	171	171	157	171	171	174	171	171
SSTL-2 Class I	OCT 50 Ω	121	134	134	121	134	134	77	134	134
SSTL-2 Class II	OCT 25 Ω	56	101	101	56	101	101	58	101	101
SSTL-18 Class I	OCT 50 Ω	100	123	123	100	123	123	106	123	123
SSTL-18 Class II	OCT 25 Ω	61	110	110	-	-	-	59	110	110
1.2-V HSTL *(2)*	OCT 50 Ω	95	-	-	-	-	-	-	-	95

Notes to Table 5–79:

(1) For LVDS and HyperTransport technology output on row I/O pins, the toggle rate derating factors apply to loads larger than 5 pF. In the derating calculation, subtract 5 pF from the intended load value in pF for the correct result. For a load less than or equal to 5 pF, refer to Table 5–78 for output toggle rates.
(2) 1.2-V HSTL is only supported on column I/O pins in I/O banks 4,7, and 8.
(3) Differential HSTL and SSTL is only supported on column clock and DQS outputs.
(4) LVPECL is only supported on column clock outputs.

Duty Cycle Distortion

Duty cycle distortion (DCD) describes how much the falling edge of a clock is off from its ideal position. The ideal position is when both the clock high time (CLKH) and the clock low time (CLKL) equal half of the clock period (T), as shown in Figure 5–7. DCD is the deviation of the non-ideal falling edge from the ideal falling edge, such as D1 for the falling edge A and D2 for the falling edge B (Figure 5–7). The maximum DCD for a clock is the larger value of D1 and D2.

Table 5–91 shows the high-speed I/O timing specifications for -5 speed grade Stratix II devices.

Table 5–91. High-Speed I/O Specifications for -5 Speed Grade *Notes (1), (2)*

Symbol	Conditions			-5 Speed Grade			Unit
				Min	Typ	Max	
f_{HSCLK} (clock frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*			16		420	MHz
	W = 1 (SERDES bypass, LVDS only)			16		500	MHz
	W = 1 (SERDES used, LVDS only)			150		640	MHz
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		840	Mbps
	J = 2 (LVDS, HyperTransport technology)			*(4)*		700	Mbps
	J = 1 (LVDS only)			*(4)*		500	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		840	Mbps
TCCS	All differential I/O standards			-		200	ps
SW	All differential I/O standards			440		-	ps
Output jitter						190	ps
Output t_{RISE}	All differential I/O standards					290	ps
Output t_{FALL}	All differential I/O standards					290	ps
t_{DUTY}				45	50	55	%
DPA run length						6,400	UI
DPA jitter tolerance	Data channel peak-to-peak jitter			0.44			UI
DPA lock time	**Standard**	**Training Pattern**	**Transition Density**				Number of repetitions
	SPI-4	0000000000 1111111111	10%	256			
	Parallel Rapid I/O	00001111	25%	256			
		10010000	50%	256			
	Miscellaneous	10101010	100%	256			
		01010101		256			

Notes to Table 5–91:

(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤ input clock frequency × W ≤ 1,040.

(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.

Table 5–100. DQS Phase Offset Delay Per Stage Notes (1), (2), (3)			
Speed Grade	**Min**	**Max**	**Unit**
-3	9	14	ps
-4	9	14	ps
-5	9	15	ps

Notes to Table 5–100:
(1) The delay settings are linear.
(2) The valid settings for phase offset are -64 to +63 for frequency mode 0 and -32 to +31 for frequency modes 1, 2, and 3.
(3) The typical value equals the average of the minimum and maximum values.

Table 5–101. DDIO Outputs Half-Period Jitter Notes (1), (2)			
Name	**Description**	**Max**	**Unit**
$t_{OUTHALFJITTER}$	Half-period jitter (PLL driving DDIO outputs)	200	ps

Notes to Table 5–101:
(1) The worst-case half period is equal to the ideal half period subtracted by the DCD and half-period jitter values.
(2) The half-period jitter was characterized using a PLL driving DDIO outputs.

JTAG Timing Specifications

Figure 5–10 shows the timing requirements for the JTAG signals.

Figure 5–10. Stratix II JTAG Waveforms

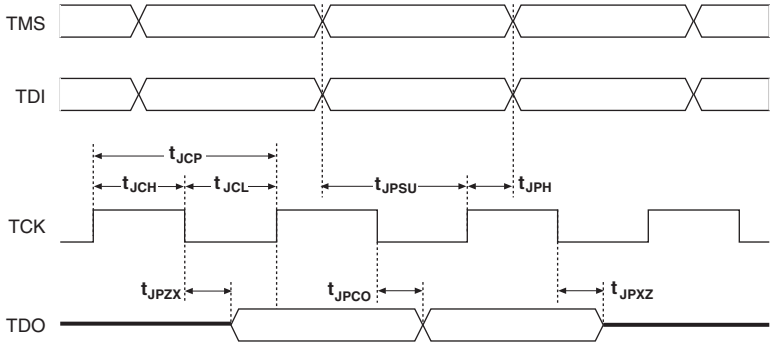


Table 5–103. Document Revision History (Part 2 of 3)

Date and Document Version	Changes Made	Summary of Changes
August, 2006, v4.2	Updated Table 5–73, Table 5–75, Table 5–77, Table 5–78, Table 5–79, Table 5–81, Table 5–85, and Table 5–87.	—
April 2006, v4.1	• Updated Table 5–3. • Updated Table 5–11. • Updated Figures 5–8 and 5–9. • Added parallel on-chip termination information to "On-Chip Termination Specifications" section. • Updated Tables 5–28, 5–30,5–31, and 5–34. • Updated Table 5–78, Tables 5–81 through 5–90, and Tables 5–92, 5–93, and 5–98. • Updated "PLL Timing Specifications" section. • Updated "External Memory Interface Specifications" section. • Added Tables 5–95 and 5–101. • Updated "JTAG Timing Specifications" section, including Figure 5–10 and Table 5–102.	• Changed 0.2 MHz to 2 MHz in Table 5–93. • Added new spec for half period jitter (Table 5–101). • Added support for PLL clock switchover for industrial temperature range. • Changed f_{INPFD} (min) spec from 4 MHz to 2 MHz in Table 5–92. • Fixed typo in $t_{OUTJITTER}$ specification in Table 5–92. • Updated V_{DIF} AC & DC max specifications in Table 5–28. • Updated minimum values for t_{JCH}, t_{JCL}, and t_{JPSU} in Table 5–102. • Update maximum values for t_{JPCO}, t_{JPZX}, and t_{JPXZ} in Table 5–102.
December 2005, v4.0	• Updated "External Memory Interface Specifications" section. • Updated timing numbers throughout chapter.	—
July 2005, v3.1	• Updated HyperTransport technology information in Table 5–13. • Updated "Timing Model" section. • Updated "PLL Timing Specifications" section. • Updated "External Memory Interface Specifications" section.	—
May 2005, v3.0	• Updated tables throughout chapter. • Updated "Power Consumption" section. • Added various tables. • Replaced "Maximum Input & Output Clock Rate" section with "Maximum Input & Output Clock Toggle Rate" section. • Added "Duty Cycle Distortion" section. • Added "External Memory Interface Specifications" section.	—
March 2005, v2.2	Updated tables in "Internal Timing Parameters" section.	—
January 2005, v2.1	Updated input rise and fall time.	—