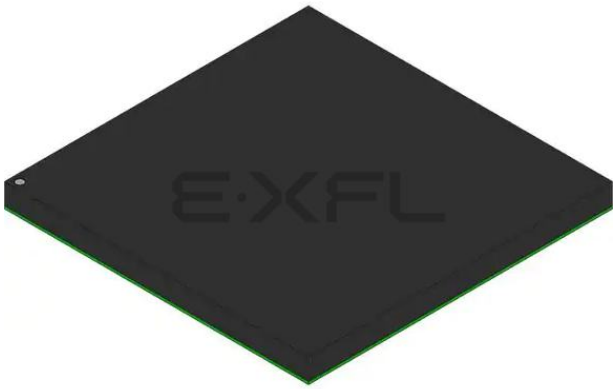

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Details	
Product Status	Active
Number of LABs/CLBs	8970
Number of Logic Elements/Cells	179400
Total RAM Bits	9383040
Number of I/O	1170
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2s180f1508c5

Chapter 3. Configuration & Testing

Chapter 4. Hot Socketing & Power-On Reset

Chapter 5. DC & Switching Characteristics

Chapter Revision Dates

The chapters in this book, *Stratix II Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Introduction
Revised: *May 2007*
Part number: *SII51001-4.2*

Chapter 2. Stratix II Architecture
Revised: *May 2007*
Part number: *SII51002-4.3*

Chapter 3. Configuration & Testing
Revised: *May 2007*
Part number: *SII51003-4.2*

Chapter 4. Hot Socketing & Power-On Reset
Revised: *May 2007*
Part number: *SII51004-3.2*

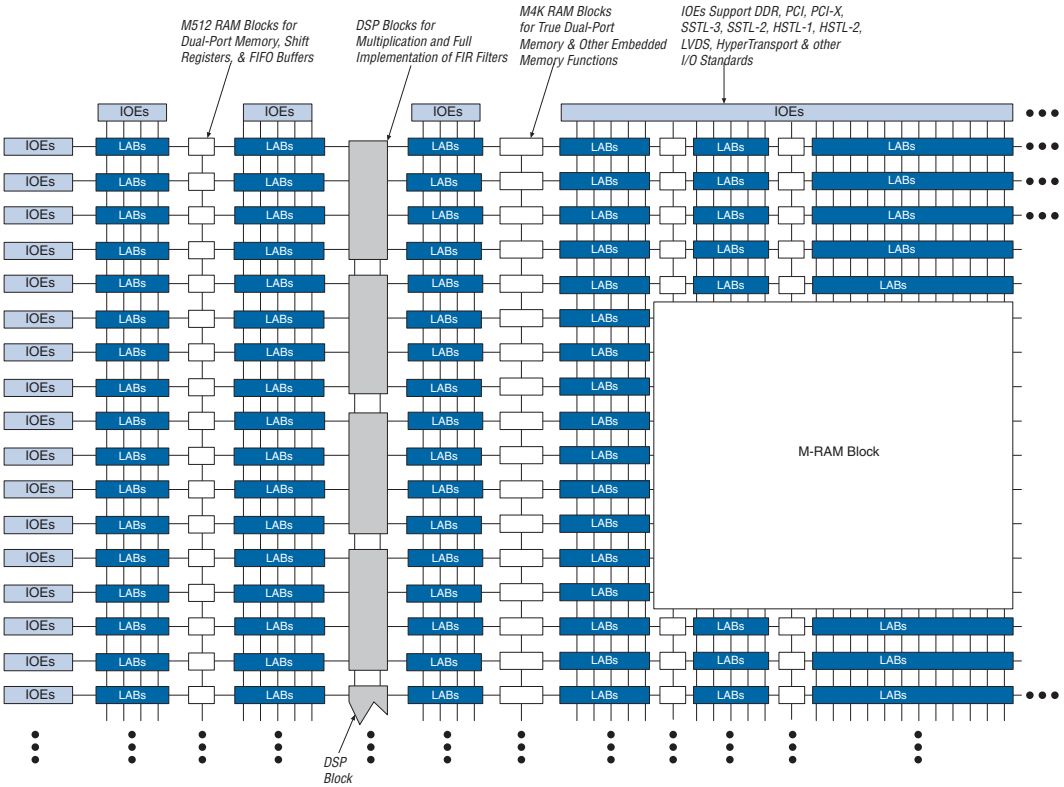
Chapter 5. DC & Switching Characteristics
Revised: *April 2011*
Part number: *SII51005-4.5*

Chapter 6. Reference & Ordering Information
Revised: *April 2011*
Part number: *SII51006-2.2*

Each Stratix II device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with dedicated clocks, these registers provide exceptional performance and interface support with external memory devices such as DDR and DDR2 SDRAM, RLDRAM II, and QDR II SRAM devices. High-speed serial interface channels with dynamic phase alignment (DPA) support data transfer at up to 1 Gbps using LVDS or HyperTransport™ technology I/O standards.

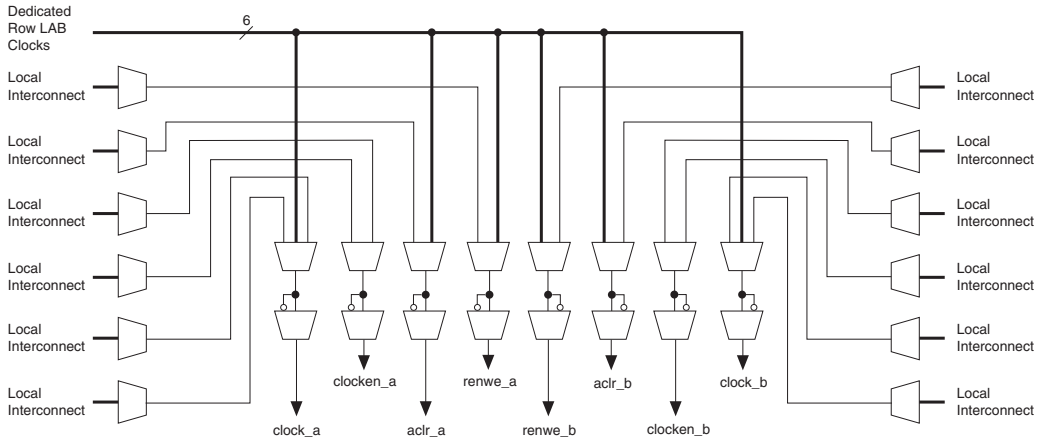
Figure 2–1 shows an overview of the Stratix II device.

Figure 2–1. Stratix II Block Diagram



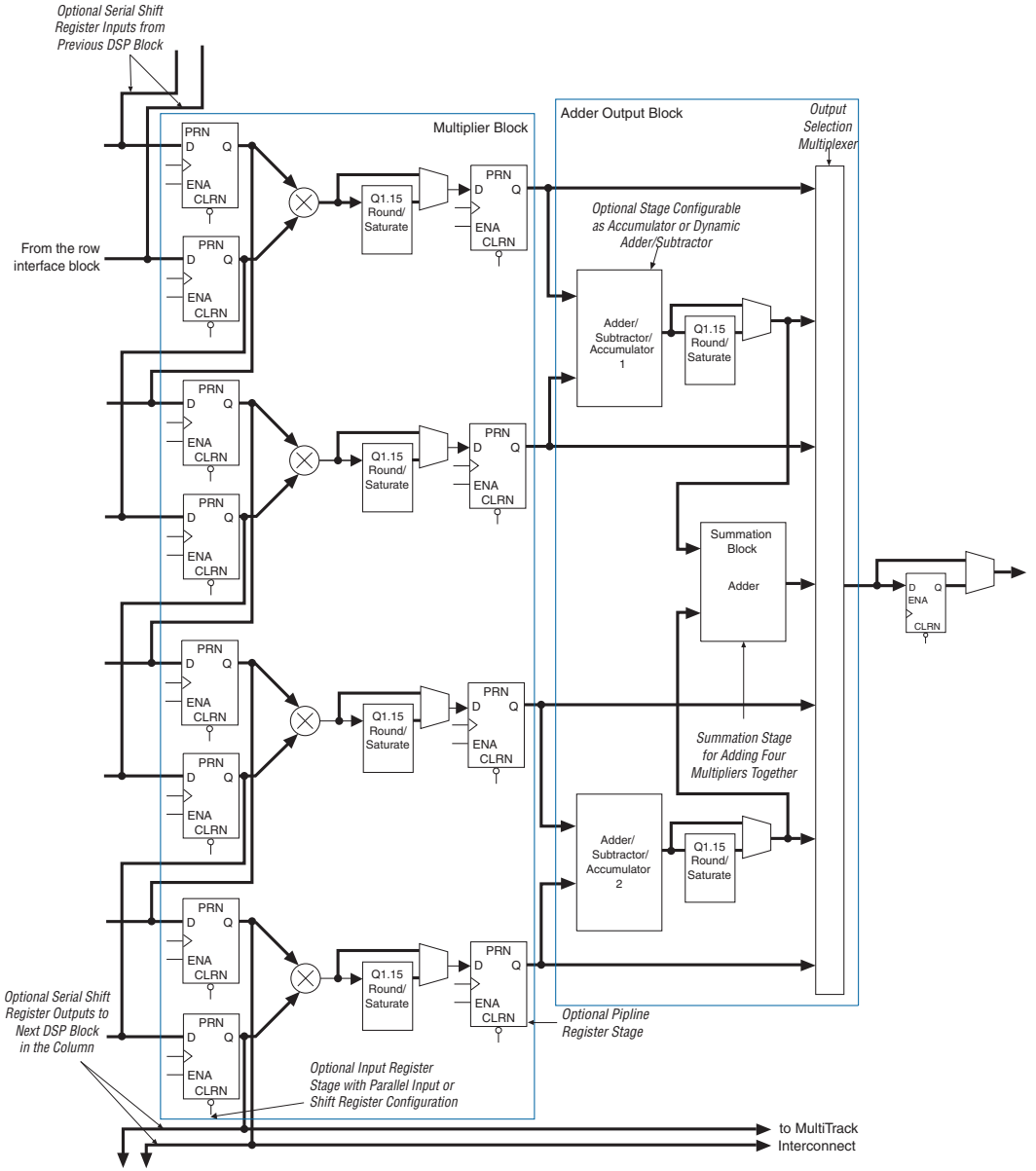
Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M-RAM block registers (renwe, address, byte enable, datain, and output registers). The output register can be bypassed. The six `labclk` signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals as shown in Figure 2–23.

Figure 2–23. M-RAM Block Control Signals



The R4, R24, C4, and direct link interconnects from adjacent LABs on either the right or left side drive the M-RAM block local interconnect. Up to 16 direct link input connections to the M-RAM block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M-RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–24 shows an example floorplan for the EP2S130 device and the location of the M-RAM interfaces. Figures 2–25 and 2–26 show the interface between the M-RAM block and the logic array.

Figure 2–28. DSP Block Diagram for 18 × 18-Bit Configuration



The DSP block is divided into four block units that interface with four LAB rows on the left and right. Each block unit can be considered one complete 18 × 18-bit multiplier with 36 inputs and 36 outputs. A local interconnect region is associated with each DSP block. Like an LAB, this interconnect region can be fed with 16 direct link interconnects from the LAB to the left or right of the DSP block in the same row. R4 and C4 routing resources can access the DSP block's local interconnect region. The outputs also work similarly to LAB outputs as well. Eighteen outputs from the DSP block can drive to the left LAB through direct link interconnects and eighteen can drive to the right LAB though direct link interconnects. All 36 outputs can drive to R4 and C4 routing interconnects. Outputs can drive right- or left-column routing. Figures 2–29 and 2–30 show the DSP block interfaces to LAB rows.

Figure 2–29. DSP Block Interconnect Interface

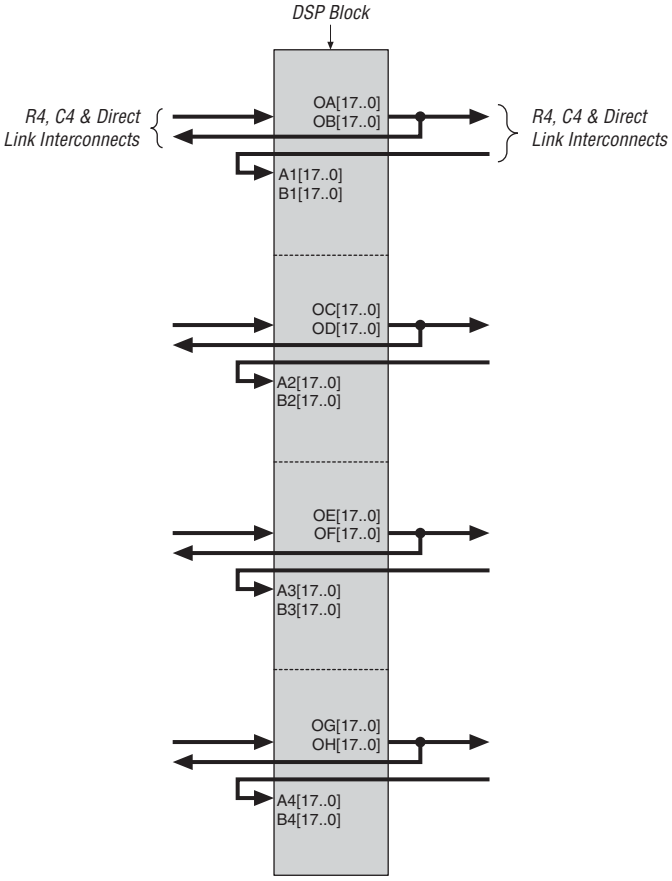
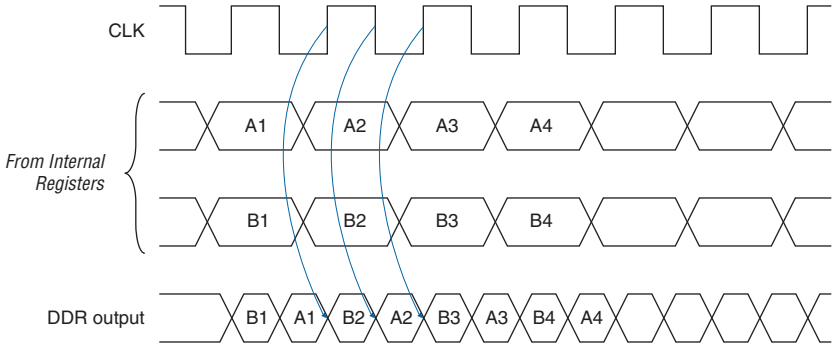


Figure 2–55. Output TIming Diagram in DDR Mode



The Stratix II IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Stratix II devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces. Stratix II devices support DDR and DDR2 SDRAM, QDR II SRAM, RLDRAM II, and SDR SDRAM memory interfaces. In every Stratix II device, the I/O banks at the top (banks 3 and 4) and bottom (banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36. Table 2–14 shows the number of DQ and DQS buses that are supported per device.

Table 2–14. DQS & DQ Bus Mode Support (Part 1 of 2) *Note (1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2S15	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
EP2S30	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
EP2S60	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
	1,020-pin FineLine BGA	36	18	8	4

Table 2–18 summarizes Stratix II MultiVolt I/O support.

Table 2–18. Stratix II MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal (V)					Output Signal (V)					
	1.2	1.5	1.8	2.5	3.3	1.2	1.5	1.8	2.5	3.3	5.0
1.2	(4)	✓ (2)	✓ (2)	✓ (2)	✓ (2)	✓ (4)					
1.5	(4)	✓	✓	✓ (2)	✓ (2)	✓ (3)	✓				
1.8	(4)	✓	✓	✓ (2)	✓ (2)	✓ (3)	✓ (3)	✓			
2.5	(4)			✓	✓	✓ (3)	✓ (3)	✓ (3)	✓		
3.3	(4)			✓	✓	✓ (3)	✓ (3)	✓ (3)	✓ (3)	✓	✓

Notes to Table 2–18:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and select the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.

(2) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable Stratix II V_{IL} maximum and V_{IH} minimum voltage specifications.

(3) Although V_{CCIO} specifies the voltage necessary for the Stratix II device to drive out, a receiving device powered at a different level can still interface with the Stratix II device if it has inputs that tolerate the V_{CCIO} value.

(4) Stratix II devices do not support 1.2-V LVTTL and 1.2-V LVCMOS. Stratix II devices support 1.2-V HSTL.

The TDO and nCEO pins are powered by V_{CCIO} of the bank that they reside in. TDO is in I/O bank 4 and nCEO is in I/O bank 7.

Ideally, the V_{CC} supplies for the I/O buffers of any two connected pins are at the same voltage level. This may not always be possible depending on the V_{CCIO} level of TDO and nCEO pins on master devices and the configuration voltage level chosen by VCCSEL on slave devices. Master and slave devices can be in any position in the chain. Master indicates that it is driving out TDO or nCEO to a slave device.

For multi-device passive configuration schemes, the nCEO pin of the master device drives the nCE pin of the slave device. The VCCSEL pin on the slave device selects which input buffer is used for nCE. When VCCSEL is logic high, it selects the 1.8-V/1.5-V buffer powered by V_{CCIO}. When VCCSEL is logic low it selects the 3.3-V/2.5-V input buffer powered by V_{CCPD}. The ideal case is to have the V_{CCIO} of the nCEO bank in a master device match the VCCSEL settings for the nCE input buffer of the slave device it is connected to, but that may not be possible depending on the application. Table 2–19 contains board design recommendations to ensure that nCEO can successfully drive nCE for all power supply combinations.

Table 3–1. Stratix II JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring a Stratix II device via the JTAG port with a USB Blaster, MasterBlaster™, ByteBlasterMV™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Notes to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information on using the CONFIG_IO instruction, see the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper.*

Table 5–34. Output Timing Measurement Methodology for Output Pins *Notes (1), (2), (3)*

I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
LVTTL *(4)*				3.135		0	1.5675
LVCMOS *(4)*				3.135		0	1.5675
2.5 V *(4)*				2.375		0	1.1875
1.8 V *(4)*				1.710		0	0.855
1.5 V *(4)*				1.425		0	0.7125
PCI *(5)*				2.970		10	1.485
PCI-X *(5)*				2.970		10	1.485
SSTL-2 Class I	25		50	2.325	1.123	0	1.1625
SSTL-2 Class II	25		25	2.325	1.123	0	1.1625
SSTL-18 Class I	25		50	1.660	0.790	0	0.83
SSTL-18 Class II	25		25	1.660	0.790	0	0.83
1.8-V HSTL Class I	50		50	1.660	0.790	0	0.83
1.8-V HSTL Class II	25		25	1.660	0.790	0	0.83
1.5-V HSTL Class I	50		50	1.375	0.648	0	0.6875
1.5-V HSTL Class II			25	1.375	0.648	0	0.6875
1.2-V HSTL with OCT	50			1.140		0	0.570
Differential SSTL-2 Class I	50		50	2.325	1.123	0	1.1625
Differential SSTL-2 Class II	25		25	2.325	1.123	0	1.1625
Differential SSTL-18 Class I	50		50	1.660	0.790	0	0.83
Differential SSTL-18 Class II	25		25	1.660	0.790	0	0.83
1.5-V Differential HSTL Class I	50		50	1.375	0.648	0	0.6875
1.5-V Differential HSTL Class II			25	1.375	0.648	0	0.6875
1.8-V Differential HSTL Class I	50		50	1.660	0.790	0	0.83
1.8-V Differential HSTL Class II	25		25	1.660	0.790	0	0.83
LVDS		100		2.325		0	1.1625
HyperTransport		100		2.325		0	1.1625
LVPECL		100		3.135		0	1.5675

Notes to Table 5–34:

(1) Input measurement point at internal node is $0.5 \times V_{CCINT}$.

(2) Output measuring point for V_{MEAS} at buffer output is $0.5 \times V_{CCIO}$.

(3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.

(4) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple

(5) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V

Table 5–36. Stratix II Performance Notes (Part 3 of 6) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
DSP block	9 × 9-bit multiplier *(5)*	0	0	1	430.29	409.16	373.13	320.10	MHz
	18 × 18-bit multiplier *(5)*	0	0	1	410.17	390.01	356.12	305.06	MHz
	18 × 18-bit multiplier *(7)*	0	0	1	450.04	428.08	391.23	335.12	MHz
	36 × 36-bit multiplier *(5)*	0	0	1	250.00	238.15	217.48	186.60	MHz
	36 × 36-bit multiplier *(6)*	0	0	1	410.17	390.01	356.12	305.06	MHz
	18-bit, four-tap FIR filter	0	0	1	410.17	390.01	356.12	305.06	MHz
Larger designs	8-bit,16-tap parallel FIR filter	58	0	4	259.06	240.61	217.15	185.01	MHz
	8-bit, 1024-point, streaming, three multipliers and five adders FFT function	2976	22	9	398.72	364.03	355.23	306.37	MHz
	8-bit, 1024-point, streaming, four multipliers and two adders FFT function	2781	22	12	398.56	409.16	347.22	311.13	MHz
	8-bit, 1024-point, single output, one parallel FFT engine, burst, three multipliers and five adders FFT function	984	5	3	425.17	365.76	346.98	292.39	MHz
	8-bit, 1024-point, single output, one parallel FFT engine, burst, four multipliers and two adders FFT function	919	5	4	427.53	378.78	357.14	307.59	MHz

Table 5–36. Stratix II Performance Notes (Part 5 of 6) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
Larger designs	8-bit, 1024-point, quadrant output, four parallel FFT engines, burst, three multipliers and five adders FFT function	6850	28	36	334.11	345.66	308.54	276.31	MHz
	8-bit, 1024-point, quadrant output, four parallel FFT engines, burst, four multipliers two adders FFT function	6067	28	48	367.91	349.04	327.33	268.24	MHz
	8-bit, 1024-point, quadrant output, one parallel FFT engine, buffered burst, three multipliers and adders FFT function	2730	18	9	387.44	388.34	364.56	306.84	MHz
	8-bit, 1024-point, quadrant output, one parallel FFT engine, buffered burst, four multipliers and two adders FFT function	2534	18	12	419.28	369.66	364.96	307.88	MHz
	8-bit, 1024-point, quadrant output, two parallel FFT engines, buffered burst, three multipliers five adders FFT function	4358	30	18	396.51	378.07	340.13	291.29	MHz
	8-bit, 1024-point, quadrant output, two parallel FFT engines, buffered burst four multipliers and two adders FFT function	3966	30	24	389.71	398.08	356.53	280.74	MHz

Table 5–41. M4K Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min (4)	Max	Min (4)	Max	Min (5)	Max	Min (4)	Max	
$t_{M4KDATAASU}$	A port data setup time before clock	22		23		25 25		29		ps
$t_{M4KDATAAH}$	A port data hold time after clock	203		213		233 233		272		ps
$t_{M4KADDRASU}$	A port address setup time before clock	22		23		25 25		29		ps
$t_{M4KADDRAH}$	A port address hold time after clock	203		213		233 233		272		ps
$t_{M4KDATABSU}$	B port data setup time before clock	22		23		25 25		29		ps
$t_{M4KDATABH}$	B port data hold time after clock	203		213		233 233		272		ps
$t_{M4KRADDRBSU}$	B port address setup time before clock	22		23		25 25		29		ps
$t_{M4KRADDRBH}$	B port address hold time after clock	203		213		233 233		272		ps
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers	334	524	334	549	319 334	601	334	701	ps
$t_{M4KDATACO2}$ (6)	Clock-to-output delay without output registers	1,616	2,453	1,616	2,574	1,540 1,616	2,820	1,616	3,286	ps
$t_{M4KCLKH}$	Minimum clock high time	1,250		1,312		1,437 1,437		1,675		ps
$t_{M4KCLKL}$	Minimum clock low time	1,250		1,312		1,437 1,437		1,675		ps
t_{M4KCLR}	Minimum clear pulse width	144		151		165 165		192		ps

Notes to Table 5–41:

(1) F_{MAX} of M4K Block obtained using the Quartus II software does not necessarily equal to 1/TM4KRC.
(2) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(3) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.
(4) For the -3 and -5 speed grades, the minimum timing is for the commercial temperature grade. Only -4 speed grade devices offer the industrial temperature grade.
(5) For the -4 speed grade, the first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.
(6) Numbers apply to unpacked memory modes, true dual-port memory modes, and simple dual-port memory modes that use locally routed or non-identical sources for the A and B port registers.

Table 5–50. EP2S30 Row Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.304	1.184	1.966	2.251	2.616	ns
t_{COUT}	1.309	1.189	1.962	2.247	2.611	ns
t_{PLLCIN}	-0.135	–0.158	–0.208	–0.254	–0.302	ns
$t_{PLLCOUT}$	-0.13	–0.153	–0.212	–0.258	–0.307	ns

Table 5–51. EP2S30 Row Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.289	1.352	2.238	2.567	2.990	ns
t_{COUT}	1.294	1.357	2.234	2.563	2.985	ns
t_{PLLCIN}	-0.14	-0.154	-0.169	-0.205	-0.254	ns
$t_{PLLCOUT}$	-0.135	-0.149	-0.173	-0.209	-0.259	ns

EP2S60 Clock Timing Parameters

Tables 5–52 through 5–55 show the maximum clock timing parameters for EP2S60 devices.

Table 5–52. EP2S60 Column Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.681	1.762	2.945	3.381	3.931	ns
t_{COUT}	1.524	1.597	2.703	3.103	3.607	ns
t_{PLLCIN}	0.066	0.064	0.279	0.311	0.348	ns
$t_{PLLCOUT}$	-0.091	-0.101	0.037	0.033	0.024	ns

Table 5–73. Stratix II I/O Input Delay for Column Pins (Part 2 of 3)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
1.5-V HSTL Class II	t_{PI}	560	587	993	1041	1141	1329	ps
	t_{PCOUT}	294	308	557	584	640	746	ps
1.8-V HSTL Class I	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.8-V HSTL Class II	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
PCI	t_{PI}	679	712	1214	1273	1395	1625	ps
	t_{PCOUT}	413	433	778	816	894	1042	ps
PCI-X	t_{PI}	679	712	1214	1273	1395	1625	ps
	t_{PCOUT}	413	433	778	816	894	1042	ps
Differential SSTL-2 Class I (1)	t_{PI}	507	530	818	857	939	1094	ps
	t_{PCOUT}	241	251	382	400	438	511	ps
Differential SSTL-2 Class II (1)	t_{PI}	507	530	818	857	939	1094	ps
	t_{PCOUT}	241	251	382	400	438	511	ps
Differential SSTL-18 Class I (1)	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
Differential SSTL-18 Class II (1)	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.8-V Differential HSTL Class I (1)	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.8-V Differential HSTL Class II (1)	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.5-V Differential HSTL Class I (1)	t_{PI}	560	587	993	1041	1141	1329	ps
	t_{PCOUT}	294	308	557	584	640	746	ps
1.5-V Differential HSTL Class II (1)	t_{PI}	560	587	993	1041	1141	1329	ps
	t_{PCOUT}	294	308	557	584	640	746	ps

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 5 of 5) *Note (1)*

I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
1.2-V Differential HSTL	OCT 50 Ω	280	-	-	-	-	-	280	-	-

Notes to Table 5–78:

(1) The toggle rate applies to 0-pF output load for all I/O standards except for LVDS and HyperTransport technology on row I/O pins. For LVDS and HyperTransport technology on row I/O pins, the toggle rates apply to load from 0 to 5pF.
(2) 1.2-V HSTL is only supported on column I/O pins in I/O banks 4, 7, and 8.
(3) Differential HSTL and SSTL is only supported on column clock and DQS outputs.
(4) HyperTransport technology is only supported on row I/O and row dedicated clock input pins.
(5) LVPECL is only supported on column clock pins.
(6) Refer to Tables 5–81 through 5–91 if using SERDES block. Use the toggle rate values from the clock output column for PLL output.

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 1 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVTTL	4 mA	478	510	510	478	510	510	466	510	510
	8 mA	260	333	333	260	333	333	291	333	333
	12 mA	213	247	247	213	247	247	211	247	247
	16 mA	136	197	197	-	-	-	166	197	197
	20 mA	138	187	187	-	-	-	154	187	187
	24 mA	134	177	177	-	-	-	143	177	177
3.3-V LVCMOS	4 mA	377	391	391	377	391	391	377	391	391
	8 mA	206	212	212	206	212	212	178	212	212
	12 mA	141	145	145	-	-	-	115	145	145
	16 mA	108	111	111	-	-	-	86	111	111
	20 mA	83	88	88	-	-	-	79	88	88
	24 mA	65	72	72	-	-	-	74	72	72
2.5-V LVTTL/LVCMOS	4 mA	387	427	427	387	427	427	391	427	427
	8 mA	163	224	224	163	224	224	170	224	224
	12 mA	142	203	203	142	203	203	152	203	203
	16 mA	120	182	182	-	-	-	134	182	182

Table 5–84. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 2 of 2) *Notes (1), (2)*

DDIO Column Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	1.2-V HSTL	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	1.2 V	
1.8 V	150	265	85	85	85	ps
1.5-V LVCMOS	255	370	140	140	140	ps
SSTL-2 Class I	175	295	65	65	65	ps
SSTL-2 Class II	170	290	60	60	60	ps
SSTL-18 Class I	155	275	55	50	50	ps
SSTL-18 Class II	140	260	70	70	70	ps
1.8-V HSTL Class I	150	270	60	60	60	ps
1.8-V HSTL Class II	150	270	60	60	60	ps
1.5-V HSTL Class I	150	270	55	55	55	ps
1.5-V HSTL Class II	125	240	85	85	85	ps
1.2-V HSTL	240	360	155	155	155	ps
LVPECL	180	180	180	180	180	ps

Notes to Table 5–84:
(1) Table 5–84 assumes the input clock has zero DCD.
(2) The DCD specification is based on a no logic array noise condition.

Table 5–85. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -4 & -5 Devices (Part 1 of 2) *Notes (1), (2)*

DDIO Column Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)				Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	
3.3-V LVTTL	440	495	170	160	ps
3.3-V LVCMOS	390	450	120	110	ps
2.5 V	375	430	105	95	ps
1.8 V	325	385	90	100	ps
1.5-V LVCMOS	430	490	160	155	ps
SSTL-2 Class I	355	410	85	75	ps
SSTL-2 Class II	350	405	80	70	ps

Table 5–103. Document Revision History (Part 2 of 3)

Date and Document Version	Changes Made	Summary of Changes
August, 2006, v4.2	Updated Table 5–73, Table 5–75, Table 5–77, Table 5–78, Table 5–79, Table 5–81, Table 5–85, and Table 5–87.	—
April 2006, v4.1	• Updated Table 5–3. • Updated Table 5–11. • Updated Figures 5–8 and 5–9. • Added parallel on-chip termination information to "On-Chip Termination Specifications" section. • Updated Tables 5–28, 5–30,5–31, and 5–34. • Updated Table 5–78, Tables 5–81 through 5–90, and Tables 5–92, 5–93, and 5–98. • Updated "PLL Timing Specifications" section. • Updated "External Memory Interface Specifications" section. • Added Tables 5–95 and 5–101. • Updated "JTAG Timing Specifications" section, including Figure 5–10 and Table 5–102.	• Changed 0.2 MHz to 2 MHz in Table 5–93. • Added new spec for half period jitter (Table 5–101). • Added support for PLL clock switchover for industrial temperature range. • Changed f_{INPFD} (min) spec from 4 MHz to 2 MHz in Table 5–92. • Fixed typo in $t_{OUTJITTER}$ specification in Table 5–92. • Updated V_{DIF} AC & DC max specifications in Table 5–28. • Updated minimum values for t_{JCH}, t_{JCL}, and t_{JPSU} in Table 5–102. • Update maximum values for t_{JPCO}, t_{JPZX}, and t_{JPXZ} in Table 5–102.
December 2005, v4.0	• Updated "External Memory Interface Specifications" section. • Updated timing numbers throughout chapter.	—
July 2005, v3.1	• Updated HyperTransport technology information in Table 5–13. • Updated "Timing Model" section. • Updated "PLL Timing Specifications" section. • Updated "External Memory Interface Specifications" section.	—
May 2005, v3.0	• Updated tables throughout chapter. • Updated "Power Consumption" section. • Added various tables. • Replaced "Maximum Input & Output Clock Rate" section with "Maximum Input & Output Clock Toggle Rate" section. • Added "Duty Cycle Distortion" section. • Added "External Memory Interface Specifications" section.	—
March 2005, v2.2	Updated tables in "Internal Timing Parameters" section.	—
January 2005, v2.1	Updated input rise and fall time.	—

Table 5–103. Document Revision History (Part 3 of 3)

Date and Document Version	Changes Made	Summary of Changes
January 2005, v2.0	• Updated the "Power Consumption" section. • Added the "High-Speed I/O Specifications" and "On-Chip Termination Specifications" sections. • Removed the ESD Protection Specifications section. • Updated Tables 5–3 through 5–13, 5–16 through 5–18, 5–21, 5–35, 5–39, and 5–40. • Updated tables in "Timing Model" section. • Added Tables 5–30 and 5–31.	—
October 2004, v1.2	• Updated Table 5–3. • Updated introduction text in the "PLL Timing Specifications" section.	—
July 2004, v1.1	• Re-organized chapter. • Added typical values and C_{OUTFB} to Table 5–32. • Added undershoot specification to Note (4) for Tables 5–1 through 5–9. • Added Note (1) to Tables 5–5 and 5–6. • Added V_{ID} and V_{ICM} to Table 5–10. • Added "I/O Timing Measurement Methodology" section. • Added Table 5–72. • Updated Tables 5–1 through 5–2 and Tables 5–24 through 5–29.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—