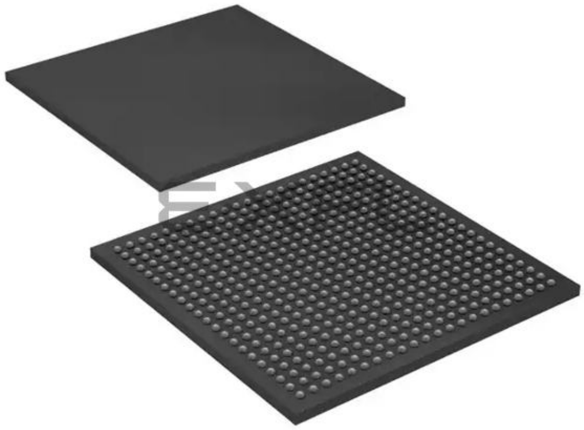

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1694
Number of Logic Elements/Cells	33880
Total RAM Bits	1369728
Number of I/O	342
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s30f484c3

About this Handbook

This handbook provides comprehensive information about the Altera® Stratix® II family of devices.

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Email	www.altera.com/literature
Altera literature services	Website	literature@altera.com
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to table:

(1) You can also contact your local Altera sales office or sales representative.

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This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*

Visual Cue	Meaning
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>*.**pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
WARNING	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Table 2–3. TriMatrix Memory Features (Part 2 of 2)			
Memory Feature	**M512 RAM Block (32 × 18 Bits)**	**M4K RAM Block (128 × 36 Bits)**	**M-RAM Block (4K × 144 Bits)**
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support		✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Output registers	Output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

Notes to Table 2–3:

(1) The M-RAM block does not support memory initializations. However, the M-RAM block can emulate a ROM function using a dual-port RAM bock. The Stratix II device must write to the dual-port memory once and then disable the write-enable ports afterwards.

Memory Block Size

TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

When applied to input registers, the asynchronous clear signal for the TriMatrix embedded memory immediately clears the input registers. However, the output of the memory block does not show the effects until the next clock edge. When applied to output registers, the asynchronous clear signal clears the output registers and the effects are seen immediately.

Table 2–4. M-RAM Row Interface Unit Signals

Unit Interface Block	Input Signals	Output Signals
L0	datain_a[14..0] byteena_a[1..0]	dataout_a[11..0]
L1	datain_a[29..15] byteena_a[3..2]	dataout_a[23..12]
L2	datain_a[35..30] addressa[4..0] addr_ena_a clock_a clocken_a renwe_a aclr_a	dataout_a[35..24]
L3	addressa[15..5] datain_a[41..36]	dataout_a[47..36]
L4	datain_a[56..42] byteena_a[5..4]	dataout_a[59..48]
L5	datain_a[71..57] byteena_a[7..6]	dataout_a[71..60]
R0	datain_b[14..0] byteena_b[1..0]	dataout_b[11..0]
R1	datain_b[29..15] byteena_b[3..2]	dataout_b[23..12]
R2	datain_b[35..30] addressb[4..0] addr_ena_b clock_b clocken_b renwe_b aclr_b	dataout_b[35..24]
R3	addressb[15..5] datain_b[41..36]	dataout_b[47..36]
R4	datain_b[56..42] byteena_b[5..4]	dataout_b[59..48]
R5	datain_b[71..57] byteena_b[7..6]	dataout_b[71..60]

See the *TriMatrix Embedded Memory Blocks in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information on TriMatrix memory.

Figure 2–27 shows one of the columns with surrounding LAB rows.

Figure 2–27. DSP Blocks Arranged in Columns

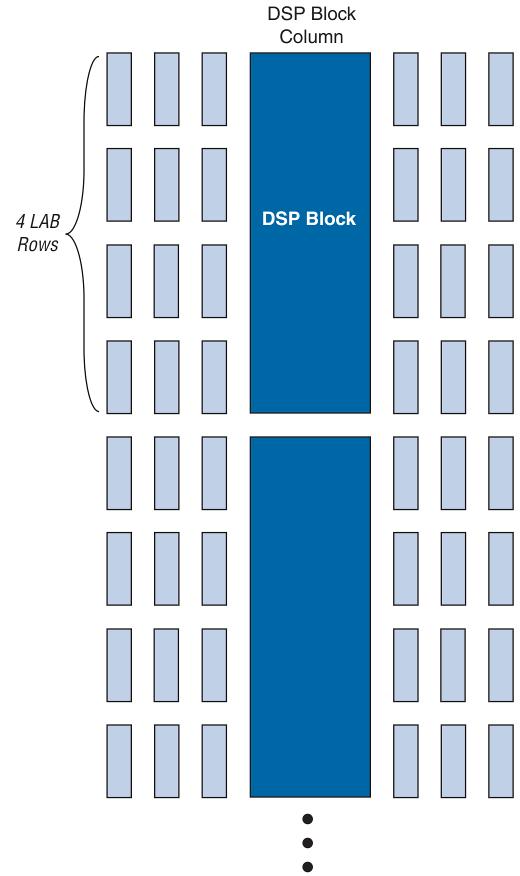
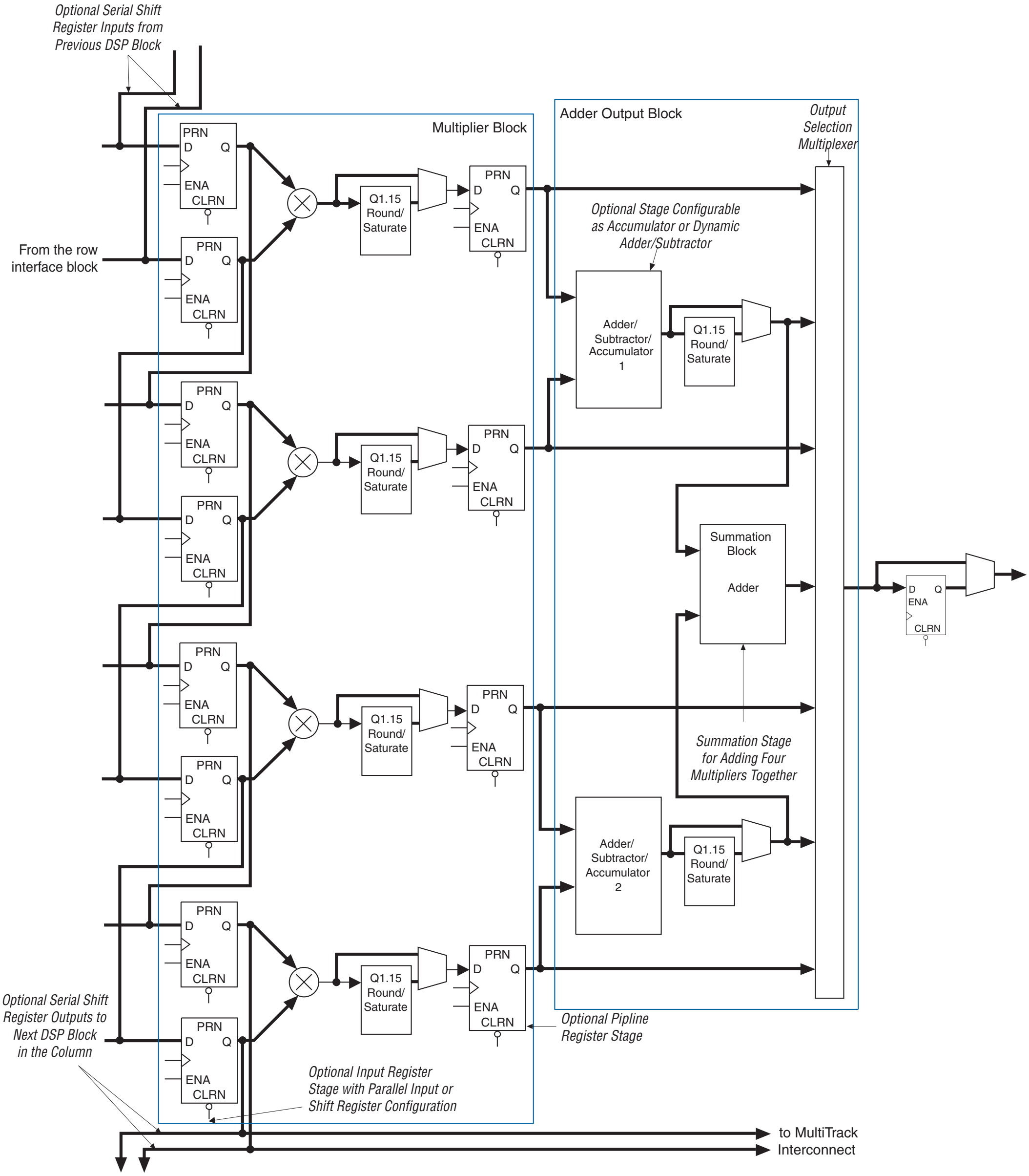


Figure 2–28. DSP Block Diagram for 18 × 18-Bit Configuration



The LAB row source for control signals, data inputs, and outputs is shown in Table 2–7.

Table 2–7. DSP Block Signal Sources & Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1[17..0] B1[17..0]	OA[17..0] OB[17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2[17..0] B2[17..0]	OC[17..0] OD[17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3[17..0] B3[17..0]	OE[17..0] OF[17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4[17..0] B4[17..0]	OG[17..0] OH[17..0]

See the *DSP Blocks in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*, for more information on DSP blocks.

The Stratix II clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all the logic fed by the clock net is in an off-state thereby reducing the overall power consumption of the device.

The global and regional clock networks can be powered down statically through a setting in the configuration (**.sof** or **.pof**) file. Clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software.

The dynamic clock enable/disable feature allows the internal logic to control power up/down synchronously on `GCLK` and `RCLK` nets and `PLL_OUT` pins. This function is independent of the PLL and is applied directly on the clock network or `PLL_OUT` pin, as shown in Figures 2–37 through 2–39.

☞ The following restrictions for the input clock pins apply:

- `CLK0 pin -> inclk[0] of CLKCTRL`
- `CLK1 pin -> inclk[1] of CLKCTRL`
- `CLK2 pin -> inclk[0] of CLKCTRL`
- `CLK3 pin -> inclk[1] of CLKCTRL`

In general, even CLK numbers connect to the `inclk[0]` port of `CLKCTRL`, and odd CLK numbers connect to the `inclk[1]` port of `CLKCTRL`.

Failure to comply with these restrictions will result in a no-fit error.

Enhanced & Fast PLLs

Stratix II devices provide robust clock management and synthesis using up to four enhanced PLLs and eight fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock-frequency synthesis. With features such as clock switchover, spread-spectrum clocking, reconfigurable bandwidth, phase control, and reconfigurable phase shifting, the Stratix II device's enhanced PLLs provide you with complete control of clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix II high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

Table 2–16. Stratix II Supported I/O Standards (Part 2 of 2)				
I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
SSTL-2 Class I and II	Voltage-referenced	1.25	2.5	1.25

Notes to Table 2–16:

(1) This I/O standard is only available on input and output column clock pins.

(2) This I/O standard is only available on input clock pins and DQS pins in I/O banks 3, 4, 7, and 8, and output clock pins in I/O banks 9,10, 11, and 12.

(3) V_{CCIO} is 3.3 V when using this I/O standard in input and output column clock pins (in I/O banks 9, 10, 11, and 12). The clock input pins supporting LVDS on banks 3, 4, 7, and 8 use V_{CCINT} for LVDS input operations and have no dependency on the V_{CCIO} level of the bank.

(4) 1.2-V HSTL is only supported in I/O banks 4,7, and 8.

For more information on I/O standards supported by Stratix II I/O banks, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

Stratix II devices contain eight I/O banks and four enhanced PLL external clock output banks, as shown in Figure 2–57. The four I/O banks on the right and left of the device contain circuitry to support high-speed differential I/O for LVDS and HyperTransport inputs and outputs. These banks support all Stratix II I/O standards except PCI or PCI-X I/O pins, and SSTL-18 Class II and HSTL outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, enhanced PLL external clock output banks allow clock output capabilities such as differential support for SSTL and HSTL.

Table 2–17 shows the Stratix II on-chip termination support per I/O bank.

Table 2–17. On-Chip Termination Support by I/O Banks (Part 1 of 2)

On-Chip Termination Support	I/O Standard Support	Top & Bottom Banks	Left & Right Banks
Series termination without calibration	3.3-V LVTTL	✓	✓
	3.3-V LVCMOS	✓	✓
	2.5-V LVTTL	✓	✓
	2.5-V LVCMOS	✓	✓
	1.8-V LVTTL	✓	✓
	1.8-V LVCMOS	✓	✓
	1.5-V LVTTL	✓	✓
	1.5-V LVCMOS	✓	✓
	SSTL-2 Class I and II	✓	✓
	SSTL-18 Class I	✓	✓
	SSTL-18 Class II	✓	
	1.8-V HSTL Class I	✓	✓
	1.8-V HSTL Class II	✓	
	1.5-V HSTL Class I	✓	✓
	1.2-V HSTL	✓	

Differential On-Chip Termination

Stratix II devices support internal differential termination with a nominal resistance value of 100 Ω for LVDS or HyperTransport technology input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. Differential on-chip termination is supported across the full range of supported differential data rates as shown in the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*.

For more information on differential on-chip termination, refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

For more information on tolerance specifications for differential on-chip termination, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook.*

On-Chip Series Termination Without Calibration

Stratix II devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Stratix II devices support on-chip series termination for single-ended I/O standards with typical R_S values of 25 and 50 Ω. Once matching impedance is selected, current drive strength is no longer selectable. Table 2–17 shows the list of output standards that support on-chip series termination without calibration.

On-Chip Series Termination with Calibration

Stratix II devices support on-chip series termination with calibration in column I/O pins in top and bottom banks. There is one calibration circuit for the top I/O banks and one circuit for the bottom I/O banks. Each on-chip series termination calibration circuit compares the total impedance of each I/O buffer to the external 25- or 50-Ω resistors connected to the `RUP` and `RDN` pins, and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.

For more information on series on-chip termination supported by Stratix II devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

Table 2–18 summarizes Stratix II MultiVolt I/O support.

Table 2–18. Stratix II MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal (V)					Output Signal (V)					
	1.2	1.5	1.8	2.5	3.3	1.2	1.5	1.8	2.5	3.3	5.0
1.2	*(4)*	✓ *(2)*	✓ *(2)*	✓ *(2)*	✓ *(2)*	✓ *(4)*					
1.5	*(4)*	✓	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓				
1.8	*(4)*	✓	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓ *(3)*	✓			
2.5	*(4)*			✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓		
3.3	*(4)*			✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	✓

Notes to Table 2–18:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and select the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.

(2) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable Stratix II V_{IL} maximum and V_{IH} minimum voltage specifications.

(3) Although V_{CCIO} specifies the voltage necessary for the Stratix II device to drive out, a receiving device powered at a different level can still interface with the Stratix II device if it has inputs that tolerate the V_{CCIO} value.

(4) Stratix II devices do not support 1.2-V LVTTL and 1.2-V LVCMOS. Stratix II devices support 1.2-V HSTL.

The `TDO` and `nCEO` pins are powered by V_{CCIO} of the bank that they reside in. `TDO` is in I/O bank 4 and `nCEO` is in I/O bank 7.

Ideally, the V_{CC} supplies for the I/O buffers of any two connected pins are at the same voltage level. This may not always be possible depending on the V_{CCIO} level of `TDO` and `nCEO` pins on master devices and the configuration voltage level chosen by `VCCSEL` on slave devices. Master and slave devices can be in any position in the chain. Master indicates that it is driving out `TDO` or `nCEO` to a slave device.

For multi-device passive configuration schemes, the `nCEO` pin of the master device drives the `nCE` pin of the slave device. The `VCCSEL` pin on the slave device selects which input buffer is used for `nCE`. When `VCCSEL` is logic high, it selects the 1.8-V/1.5-V buffer powered by V_{CCIO}. When `VCCSEL` is logic low it selects the 3.3-V/2.5-V input buffer powered by V_{CCPD}. The ideal case is to have the V_{CCIO} of the `nCEO` bank in a master device match the `VCCSEL` settings for the `nCE` input buffer of the slave device it is connected to, but that may not be possible depending on the application. Table 2–19 contains board design recommendations to ensure that `nCEO` can successfully drive `nCE` for all power supply combinations.

Table 5–3. Stratix II Device Recommended Operating Conditions (Part 2 of 2) Note (1)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
T_J	Operating junction temperature	For commercial use	0	85	°C
		For industrial use	–40	100	°C
		For military use *(7)*	–55	125	°C

Notes to Table 5–3:

(1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.
(2) During transitions, the inputs may overshoot to the voltage shown in Table 5–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically from ground to V_{CC}.
(4) V_{CCPD} must ramp-up from 0 V to 3.3 V within 100 μs to 100 ms. If V_{CCPD} is not ramped up within this specified time, your Stratix II device does not configure successfully. If your system does not allow for a V_{CCPD} ramp-up time of 100 ms or less, you must hold `nCONFIG` low until all power supplies are reliable.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT}, V_{CCPD}, and V_{CCIO} are powered.
(6) V_{CCIO} maximum and minimum conditions for PCI and PCI-X are shown in parentheses.
(7) For more information, refer to the *Stratix II Military Temperature Range Support* technical brief.

DC Electrical Characteristics

Table 5–4 shows the Stratix II device family DC electrical characteristics.

Table 5–4. Stratix II Device DC Operating Conditions (Part 1 of 2) Note (1)

Symbol	Parameter	Conditions		Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(2)*		–10		10	μA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(2)*		–10		10	μA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25° C	EP2S15		0.25	*(3)*	A
			EP2S30		0.30	*(3)*	A
			EP2S60		0.50	*(3)*	A
			EP2S90		0.62	*(3)*	A
			EP2S130		0.82	*(3)*	A
			EP2S180		1.12	*(3)*	A
I_{CCPD0}	V_{CCPD} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25° C, V_{CCPD} = 3.3V	EP2S15		2.2	*(3)*	mA
			EP2S30		2.7	*(3)*	mA
			EP2S60		3.6	*(3)*	mA
			EP2S90		4.3	*(3)*	mA
			EP2S130		5.4	*(3)*	mA
			EP2S180		6.8	*(3)*	mA

Table 5–12. LVPECL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO} *(1)*	I/O supply voltage		3.135	3.300	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		300	600	1,000	mV
V_{ICM}	Input common mode voltage		1.0		2.5	V
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	525		970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1,650		2,250	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Note to Table 5–12:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by `VCC_PLL_OUT`. For differential clock output/feedback operation, `VCC_PLL_OUT` should be connected to 3.3 V.

Table 5–13. HyperTransport Technology Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)		2.375	2.500	2.625	V
V_{ID}	Input differential voltage swing (single-ended)	R_L = 100 Ω	300	600	900	mV
V_{ICM}	Input common mode voltage	R_L = 100 Ω	385	600	845	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	400	600	820	mV
ΔV_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			75	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	440	600	780	mV
ΔV_{OCM}	Change in V_{OCM} between high and low	R_L = 100 Ω			50	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Table 5–14. 3.3-V PCI Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V

Table 5–17. SSTL-18 Class II Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Reference voltage		0.855	0.900	0.945	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.125			V
V_{IL} (DC)	Low-level DC input voltage				V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.25			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{CCIO} – 0.28			V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*			0.28	V

Note to Table 5–17:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–18. SSTL-18 Class I & II Differential Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{SWING} (DC)	DC differential input voltage		0.25			V
V_X (AC)	AC differential input cross point voltage		(V_{CCIO}/2) – 0.175		(V_{CCIO}/2) + 0.175	V
V_{SWING} (AC)	AC differential input voltage		0.5			V
V_{ISO}	Input clock signal offset voltage			0.5 × V_{CCIO}		V
ΔV_{ISO}	Input clock signal offset voltage variation			±200		mV
V_{OX} (AC)	AC differential cross point voltage		(V_{CCIO}/2) – 0.125		(V_{CCIO}/2) + 0.125	V

Table 5–21. SSTL-2 Class I & II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.500	2.625	V
V_{SWING} (DC)	DC differential input voltage		0.36			V
V_X (AC)	AC differential input cross point voltage		$(V_{CCIO}/2) - 0.2$		$(V_{CCIO}/2) + 0.2$	V
V_{SWING} (AC)	AC differential input voltage		0.7			V
V_{ISO}	Input clock signal offset voltage			$0.5 \times V_{CCIO}$		V
ΔV_{ISO}	Input clock signal offset voltage variation			±200		mV
V_{OX} (AC)	AC differential output cross point voltage		$(V_{CCIO}/2) - 0.2$		$(V_{CCIO}/2) + 0.2$	V

Table 5–22. 1.2-V HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.14	1.20	1.26	V
V_{REF}	Reference voltage		$0.48 \times V_{CCIO}$	$0.50 \times V_{CCIO}$	$0.52 \times V_{CCIO}$	V
V_{IH} (DC)	High-level DC input voltage		$V_{REF} + 0.08$		$V_{CCIO} + 0.15$	V
V_{IL} (DC)	Low-level DC input voltage		–0.15		$V_{REF} - 0.08$	V
V_{IH} (AC)	High-level AC input voltage		$V_{REF} + 0.15$		$V_{CCIO} + 0.24$	V
V_{IL} (AC)	Low-level AC input voltage		–0.24		$V_{REF} - 0.15$	V
V_{OH}	High-level output voltage	$I_{OH} = 8$ mA	$V_{REF} + 0.15$		$V_{CCIO} + 0.15$	V
V_{OL}	Low-level output voltage	$I_{OH} = -8$ mA	–0.15		$V_{REF} - 0.15$	V

Table 5–65. EP2S180 Column Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	2.003	2.100	3.652	3.993	4.648	ns
t_{COUT}	1.846	1.935	3.398	3.715	4.324	ns
t_{PLLCIN}	-0.3	-0.29	0.053	0.054	0.058	ns
$t_{PLLCOUT}$	-0.457	-0.455	-0.201	-0.224	-0.266	ns

Table 5–66. EP2S180 Row Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.759	1.844	3.273	3.577	4.162	ns
t_{COUT}	1.764	1.849	3.269	3.573	4.157	ns
t_{PLLCIN}	-0.542	-0.541	-0.317	-0.353	-0.414	ns
$t_{PLLCOUT}$	-0.537	-0.536	-0.321	-0.357	-0.419	ns

Table 5–67. EP2S180 Row Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.763	1.850	3.285	3.588	4.176	ns
t_{COUT}	1.768	1.855	3.281	3.584	4.171	ns
t_{PLLCIN}	-0.542	-0.542	-0.319	-0.355	-0.42	ns
$t_{PLLCOUT}$	-0.537	-0.537	-0.323	-0.359	-0.425	ns

Table 5–71. Default Loading of Different I/O Standards for Stratix II (Part 2 of 2)

I/O Standard	Capacitive Load	Unit
SSTL-2 Class II	0	pF
SSTL-18 Class I	0	pF
SSTL-18 Class II	0	pF
1.5-V HSTL Class I	0	pF
1.5-V HSTL Class II	0	pF
1.8-V HSTL Class I	0	pF
1.8-V HSTL Class II	0	pF
1.2-V HSTL with OCT	0	pF
Differential SSTL-2 Class I	0	pF
Differential SSTL-2 Class II	0	pF
Differential SSTL-18 Class I	0	pF
Differential SSTL-18 Class II	0	pF
1.5-V Differential HSTL Class I	0	pF
1.5-V Differential HSTL Class II	0	pF
1.8-V Differential HSTL Class I	0	pF
1.8-V Differential HSTL Class II	0	pF
LVDS	0	pF
HyperTransport	0	pF
LVPECL	0	pF

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 3 of 5) Note (1)

I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
Differential SSTL-18 Class I *(3)*	4 mA	200	150	150	200	150	150	200	150	150
	6 mA	350	250	200	350	250	200	350	250	200
	8 mA	450	300	300	450	300	300	450	300	300
	10 mA	500	400	400	500	400	400	500	400	400
	12 mA	700	550	400	350	350	297	650	550	400
Differential SSTL-18 Class II *(3)*	8 mA	200	200	150	-	-	-	200	200	150
	16 mA	400	350	350	-	-	-	400	350	350
	18 mA	450	400	400	-	-	-	450	400	400
	20 mA	550	500	450	-	-	-	550	500	450
1.8-V Differential HSTL Class I *(3)*	4 mA	300	300	300	-	-	-	300	300	300
	6 mA	500	450	450	-	-	-	500	450	450
	8 mA	650	600	600	-	-	-	650	600	600
	10 mA	700	650	600	-	-	-	700	650	600
	12 mA	700	700	650	-	-	-	700	700	650
1.8-V Differential HSTL Class II *(3)*	16 mA	500	500	450	-	-	-	500	500	450
	18 mA	550	500	500	-	-	-	550	500	500
	20 mA	650	550	550	-	-	-	550	550	550
1.5-V Differential HSTL Class I *(3)*	4 mA	350	300	300	-	-	-	350	300	300
	6 mA	500	500	450	-	-	-	500	500	450
	8 mA	700	650	600	-	-	-	700	650	600
	10 mA	700	700	650	-	-	-	700	700	650
	12 mA	700	700	700	-	-	-	700	700	700
1.5-V Differential HSTL Class II *(3)*	16 mA	600	600	550	-	-	-	600	600	550
	18 mA	650	600	600	-	-	-	650	600	600
	20 mA	700	650	600	-	-	-	700	650	600
3.3-V PCI		1,000	790	670	-	-	-	1,000	790	670
3.3-V PCI-X		1,000	790	670	-	-	-	1,000	790	670
LVDS *(6)*		-	-	-	500	500	500	450	400	300
HyperTransport technology *(4)*, *(6)*					500	500	500	-	-	-
LVPECL *(5)*		-	-	-	-	-	-	450	400	300
3.3-V LVTTL	OCT 50 Ω	400	400	350	400	400	350	400	400	350
2.5-V LVTTL	OCT 50 Ω	350	350	300	350	350	300	350	350	300

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 5 of 5) Note (1)										
I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
1.2-V Differential HSTL	OCT 50 Ω	280	-	-	-	-	-	280	-	-

Notes to Table 5–78:

(1) The toggle rate applies to 0-pF output load for all I/O standards except for LVDS and HyperTransport technology on row I/O pins. For LVDS and HyperTransport technology on row I/O pins, the toggle rates apply to load from 0 to 5pF.
(2) 1.2-V HSTL is only supported on column I/O pins in I/O banks 4, 7, and 8.
(3) Differential HSTL and SSTL is only supported on column clock and DQS outputs.
(4) HyperTransport technology is only supported on row I/O and row dedicated clock input pins.
(5) LVPECL is only supported on column clock pins.
(6) Refer to Tables 5–81 through 5–91 if using SERDES block. Use the toggle rate values from the clock output column for PLL output.

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 1 of 5)										
I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVTTL	4 mA	478	510	510	478	510	510	466	510	510
	8 mA	260	333	333	260	333	333	291	333	333
	12 mA	213	247	247	213	247	247	211	247	247
	16 mA	136	197	197	-	-	-	166	197	197
	20 mA	138	187	187	-	-	-	154	187	187
	24 mA	134	177	177	-	-	-	143	177	177
3.3-V LVCMOS	4 mA	377	391	391	377	391	391	377	391	391
	8 mA	206	212	212	206	212	212	178	212	212
	12 mA	141	145	145	-	-	-	115	145	145
	16 mA	108	111	111	-	-	-	86	111	111
	20 mA	83	88	88	-	-	-	79	88	88
	24 mA	65	72	72	-	-	-	74	72	72
2.5-V LVTTL/LVCMOS	4 mA	387	427	427	387	427	427	391	427	427
	8 mA	163	224	224	163	224	224	170	224	224
	12 mA	142	203	203	142	203	203	152	203	203
	16 mA	120	182	182	-	-	-	134	182	182