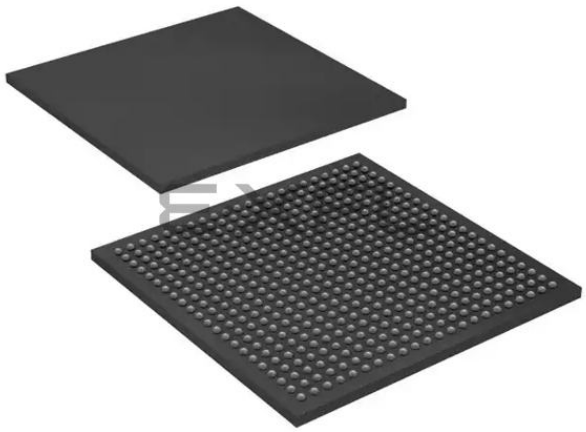
# Intel - EP2S30F484C4 Datasheet



Welcome to E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1694 |
| Number of Logic Elements/Cells | 33880 |
| Total RAM Bits | 1369728 |
| Number of I/O | 342 |
| Number of Gates | - |
| Voltage - Supply | 1.15V ~ 1.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep2s30f484c4 |

# Contents

**Chapter Revision Dates** ..... vii

**About this Handbook** ..... i
How to Contact Altera ..... i
Typographic Conventions ..... i

## Section I. Stratix II Device Family Data Sheet
Revision History ..... Section I–1

### Chapter 1. Introduction
Introduction ..... 1–1
Features ..... 1–1
Document Revision History ..... 1–6

### Chapter 2. Stratix II Architecture
Functional Description ..... 2–1
Logic Array Blocks ..... 2–3
LAB Interconnects ..... 2–4
LAB Control Signals ..... 2–5
Adaptive Logic Modules ..... 2–6
ALM Operating Modes ..... 2–9
Register Chain ..... 2–20
Clear & Preset Logic Control ..... 2–22
MultiTrack Interconnect ..... 2–22
TriMatrix Memory ..... 2–28
Memory Block Size ..... 2–29
Digital Signal Processing Block ..... 2–40
Modes of Operation ..... 2–44
DSP Block Interface ..... 2–44
PLLs & Clock Networks ..... 2–48
Global & Hierarchical Clocking ..... 2–48
Enhanced & Fast PLLs ..... 2–57
Enhanced PLLs ..... 2–68
Fast PLLs ..... 2–69
I/O Structure ..... 2–69
Double Data Rate I/O Pins ..... 2–77
External RAM Interfacing ..... 2–81
Programmable Drive Strength ..... 2–83

Timing Model ..... 5–20
Preliminary & Final Timing ..... 5–20
I/O Timing Measurement Methodology ..... 5–21
Performance ..... 5–27
Internal Timing Parameters ..... 5–34
Stratix II Clock Timing Parameters ..... 5–41
Clock Network Skew Adders ..... 5–50
IOE Programmable Delay ..... 5–51
Default Capacitive Loading of Different I/O Standards ..... 5–52
I/O Delays ..... 5–54
Maximum Input & Output Clock Toggle Rate ..... 5–66
Duty Cycle Distortion ..... 5–77
DCD Measurement Techniques ..... 5–78
High-Speed I/O Specifications ..... 5–87
PLL Timing Specifications ..... 5–91
External Memory Interface Specifications ..... 5–94
JTAG Timing Specifications ..... 5–96
Document Revision History ..... 5–97

## Chapter 6. Reference & Ordering Information

Software ..... 6–1
Device Pin-Outs ..... 6–1
Ordering Information ..... 6–1
Document Revision History ..... 6–2

# Chapter Revision Dates

The chapters in this book, *Stratix II Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Introduction
Revised: *May 2007*
Part number: *SII51001-4.2*

Chapter 2. Stratix II Architecture
Revised: *May 2007*
Part number: *SII51002-4.3*

Chapter 3. Configuration & Testing
Revised: *May 2007*
Part number: *SII51003-4.2*

Chapter 4. Hot Socketing & Power-On Reset
Revised: *May 2007*
Part number: *SII51004-3.2*

Chapter 5. DC & Switching Characteristics
Revised: *April 2011*
Part number: *SII51005-4.5*

Chapter 6. Reference & Ordering Information
Revised: *April 2011*
Part number: *SII51006-2.2*

- Support for numerous single-ended and differential I/O standards
- High-speed differential I/O support with DPA circuitry for 1-Gbps performance
- Support for high-speed networking and communications bus standards including Parallel RapidIO, SPI-4 Phase 2 (POS-PHY Level 4), HyperTransport™ technology, and SFI-4
- Support for high-speed external memory, including DDR and DDR2 SDRAM, RLDRAM II, QDR II SRAM, and SDR SDRAM
- Support for multiple intellectual property megafunctions from Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
- Support for design security using configuration bitstream encryption
- Support for remote configuration updates

*Table 1–1. Stratix II FPGA Family Features*

| Feature | EP2S15 | EP2S30 | EP2S60 | EP2S90 | EP2S130 | EP2S180 |
|---|---|---|---|---|---|---|
| ALMs | 6,240 | 13,552 | 24,176 | 36,384 | 53,016 | 71,760 |
| Adaptive look-up tables (ALUTs) *(1)* | 12,480 | 27,104 | 48,352 | 72,768 | 106,032 | 143,520 |
| Equivalent LEs *(2)* | 15,600 | 33,880 | 60,440 | 90,960 | 132,540 | 179,400 |
| M512 RAM blocks | 104 | 202 | 329 | 488 | 699 | 930 |
| M4K RAM blocks | 78 | 144 | 255 | 408 | 609 | 768 |
| M-RAM blocks | 0 | 1 | 2 | 4 | 6 | 9 |
| Total RAM bits | 419,328 | 1,369,728 | 2,544,192 | 4,520,488 | 6,747,840 | 9,383,040 |
| DSP blocks | 12 | 16 | 36 | 48 | 63 | 96 |
| 18-bit × 18-bit multipliers *(3)* | 48 | 64 | 144 | 192 | 252 | 384 |
| Enhanced PLLs | 2 | 2 | 4 | 4 | 4 | 4 |
| Fast PLLs | 4 | 4 | 8 | 8 | 8 | 8 |
| Maximum user I/O pins | 366 | 500 | 718 | 902 | 1,126 | 1,170 |

*Notes to Table 1–1:*

(1) One ALM contains two ALUTs. The ALUT is the cell used in the Quartus® II software for logic synthesis.

(2) This is the equivalent number of LEs in a Stratix device (four-input LUT-based architecture).

(3) These multipliers are implemented using the DSP blocks.

Stratix II devices are available in up to three speed grades, -3, -4, and -5, with -3 being the fastest. Table 1–5 shows Stratix II device speed-grade offerings.

*Table 1–5. Stratix II Device Speed Grades*

| Device | Temperature Grade | 484-Pin FineLine BGA | 484-Pin Hybrid FineLine BGA | 672-Pin FineLine BGA | 780-Pin FineLine BGA | 1,020-Pin FineLine BGA | 1,508-Pin FineLine BGA |
|---|---|---|---|---|---|---|---|
| EP2S15 | Commercial | -3, -4, -5 | | -3, -4, -5 | | | |
| | Industrial | -4 | | -4 | | | |
| EP2S30 | Commercial | -3, -4, -5 | | -3, -4, -5 | | | |
| | Industrial | -4 | | -4 | | | |
| EP2S60 | Commercial | -3, -4, -5 | | -3, -4, -5 | | -3, -4, -5 | |
| | Industrial | -4 | | -4 | | -4 | |
| EP2S90 | Commercial | | -4, -5 | | -4, -5 | -3, -4, -5 | -3, -4, -5 |
| | Industrial | | | | | -4 | -4 |
| EP2S130 | Commercial | | | | -4, -5 | -3, -4, -5 | -3, -4, -5 |
| | Industrial | | | | | -4 | -4 |
| EP2S180 | Commercial | | | | | -3, -4, -5 | -3, -4, -5 |
| | Industrial | | | | | -4 | -4 |

## Document Revision History

Table 1–6 shows the revision history for this chapter.

*Table 1–6. Document Revision History*

| Date and Document Version | Changes Made | Summary of Changes |
|---|---|---|
| May 2007, v4.2 | Moved Document Revision History to the end of the chapter. | — |
| April 2006, v4.1 | • Updated “Features” section.<br>• Removed Note 4 from Table 1–2.<br>• Updated Table 1–4. | — |
| December 2005, v4.0 | • Updated Tables 1–2, 1–4, and 1–5.<br>• Updated Figure 2–43. | — |
| July 2005, v3.1 | • Added vertical migration information, including Table 1–4.<br>• Updated Table 1–5. | — |
| May 2005, v3.0 | • Updated “Features” section.<br>• Updated Table 1–2. | — |
| March 2005, v2.1 | Updated “Introduction” and “Features” sections. | — |
| January 2005, v2.0 | Added note to Table 1–2. | — |
| October 2004, v1.2 | Updated Tables 1–2, 1–3, and 1–5. | — |
| July 2004, v1.1 | • Updated Tables 1–1 and 1–2.<br>• Updated “Features” section. | — |
| February 2004, v1.0 | Added document to the Stratix II Device Handbook. | — |

synchronous load, and clock enable control for the register. These LAB-wide signals are available in all ALM modes. See the "LAB Control Signals" section for more information on the LAB-wide control signals.

The Quartus II software and supported third-party synthesis tools, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically choose the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which ALM operating mode to use for optimal performance.

### *Normal Mode*

The normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. The normal mode allows two functions to be implemented in one Stratix II ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs. Figure 2–7 shows the supported LUT combinations in normal mode.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (that is, TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[5..0]`.

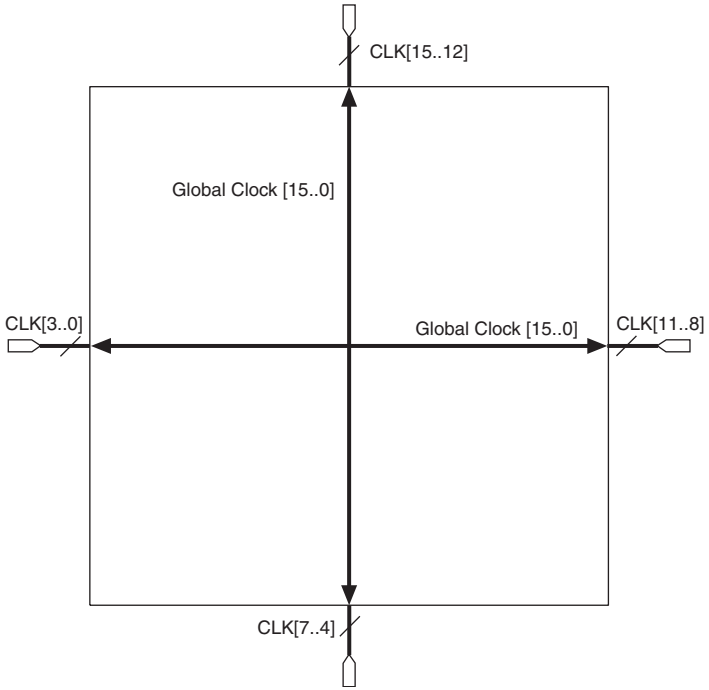
Table 2–2 shows the Stratix II device's routing scheme.

***Table 2–2. Stratix II Device Routing Scheme (Part 1 of 2)***

| Source | Destination | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Shared Arithmetic Chain | Carry Chain | Register Chain | Local Interconnect | Direct Link Interconnect | R4 Interconnect | R24 Interconnect | C4 Interconnect | C16 Interconnect | ALM | M512 RAM Block | M4K RAM Block | M-RAM Block | DSP Blocks | Column IOE | Row IOE |
| Shared arithmetic chain | | | | | | | | | | ✓ | | | | | | |
| Carry chain | | | | | | | | | | ✓ | | | | | | |
| Register chain | | | | | | | | | | ✓ | | | | | | |
| Local interconnect | | | | | | | | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Direct link interconnect | | | | ✓ | | | | | | | | | | | | |
| R4 interconnect | | | | ✓ | | ✓ | ✓ | ✓ | ✓ | | | | | | | |
| R24 interconnect | | | | | | ✓ | ✓ | ✓ | ✓ | | | | | | | |
| C4 interconnect | | | | ✓ | | ✓ | | ✓ | | | | | | | | |
| C16 interconnect | | | | | | ✓ | ✓ | ✓ | ✓ | | | | | | | |
| ALM | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | | | | | | | | |
| M512 RAM block | | | | ✓ | ✓ | ✓ | | ✓ | | | | | | | | |
| M4K RAM block | | | | ✓ | ✓ | ✓ | | ✓ | | | | | | | | |
| M-RAM block | | | | | ✓ | ✓ | ✓ | ✓ | | | | | | | | |
| DSP blocks | | | | | ✓ | ✓ | | ✓ | | | | | | | | |

global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–31 shows the 16 dedicated CLK pins driving global clock networks.

*Figure 2–31. Global Clocking*



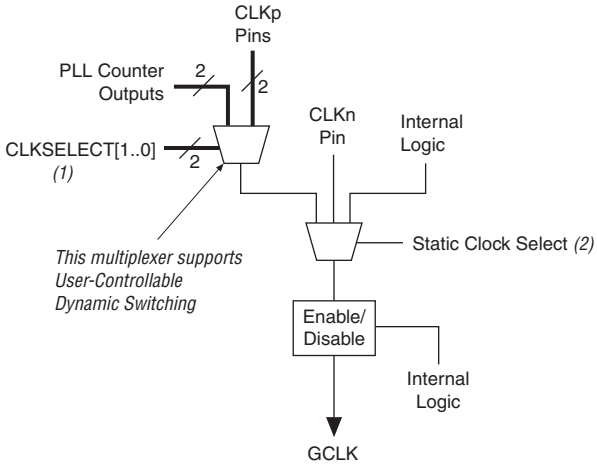

### Regional Clock Network

There are eight regional clock networks RCLK[7..0] in each quadrant of the Stratix II device that are driven by the dedicated CLK[15..0] input pins, by PLL outputs, or by internal logic. The regional clock networks provide the lowest clock delay and skew for logic contained in a single quadrant. The CLK clock pins symmetrically drive the RCLK networks in a particular quadrant, as shown in Figure 2–32.

When using the global or regional clock control blocks in Stratix II devices to select between multiple clocks or to enable and disable clock networks, be aware of possible narrow pulses or glitches when switching from one clock signal to another. A glitch or runt pulse has a width that is less than the width of the highest frequency input clock signal. To prevent logic errors within the FPGA, Altera recommends that you build circuits that filter out glitches and runt pulses.

Figures 2–37 through 2–39 show the clock control block for the global clock, regional clock, and PLL external clock output, respectively.

***Figure 2–37. Global Clock Control Blocks***

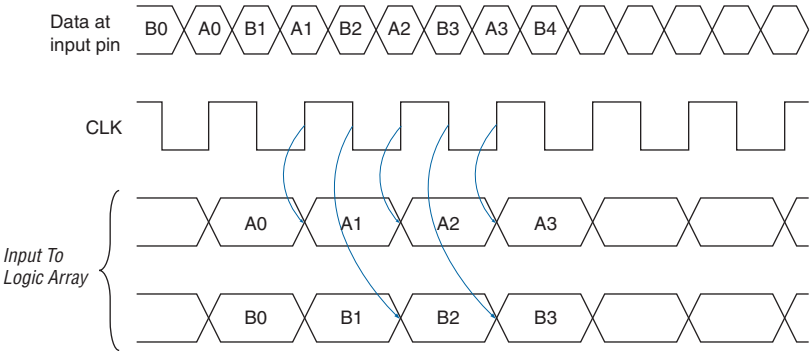



***Notes to Figure 2–37:***

(1) These clock select signals can be dynamically controlled through internal logic when the device is operating in user mode.

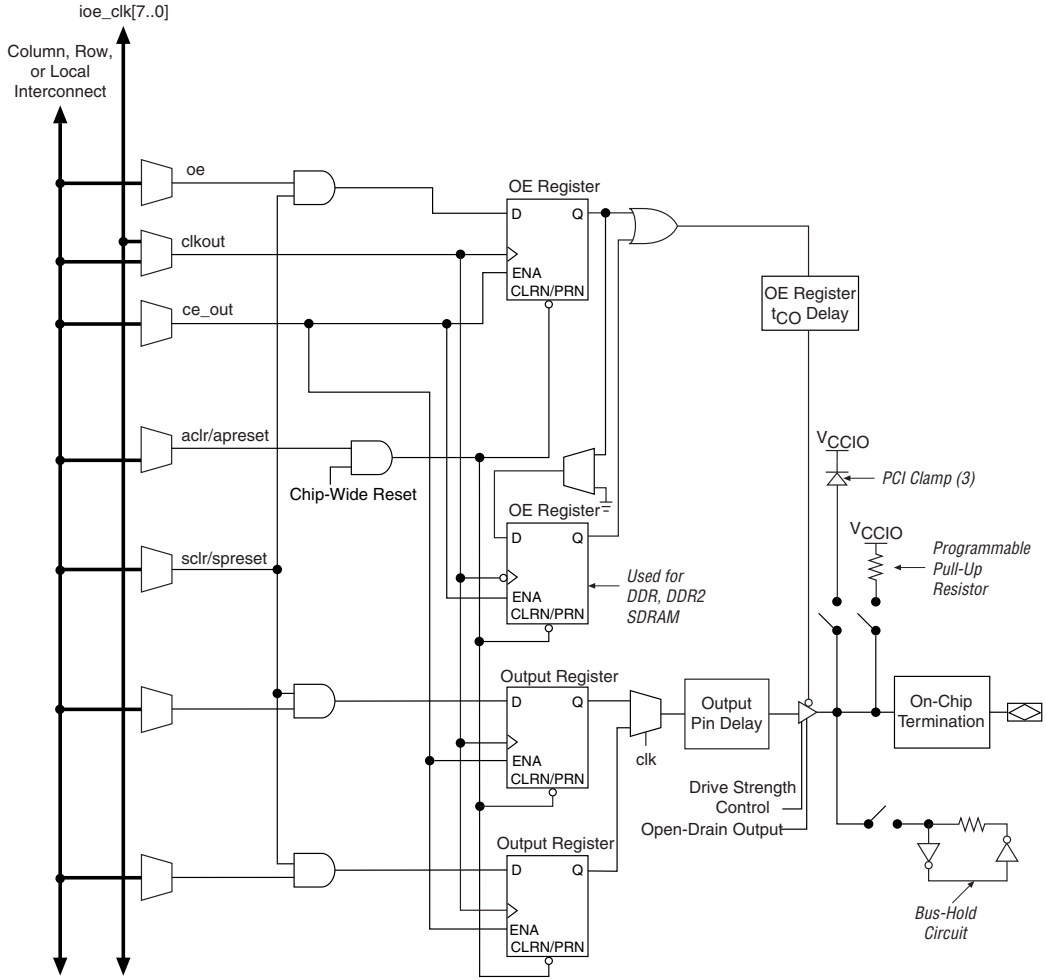
(2) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

*Figure 2–53. Input Timing Diagram in DDR Mode*




When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from ALMs on rising clock edges. These output registers are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 2–54 shows the IOE configured for DDR output. Figure 2–55 shows the DDR output timing diagram.

*Figure 2–54. Stratix II IOE in DDR Output I/O Configuration* *Notes (1), (2)*




*Notes to Figure 2–54:*

(1) All input signals to the IOE can be inverted at the IOE.

(2) The tri-state buffer is active low. The DDIO megafunction represents the tri-state buffer as active-high with an inverter at the OE register data port. Similarly, the `aclr` and `apreset` signals are also active-high at the input ports of the DDIO megafunction.

(3) The optional PCI clamp is only available on column I/O pins.

*Table 2–25. EP2S130 Differential Channels* *Note (1)*

| Package | Transmitter/ Receiver | Total Channels | Center Fast PLLs | | | | Corner Fast PLLs *(4)* | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | PLL 1 | PLL 2 | PLL 3 | PLL 4 | PLL 7 | PLL 8 | PLL 9 | PLL 10 |
| 780-pin FineLine BGA | Transmitter | 64 *(2)* | 16 | 16 | 16 | 16 | - | - | - | |
| | | *(3)* | 32 | 32 | 32 | 32 | - | - | - | - |
| | Receiver | 68 *(2)* | 17 | 17 | 17 | 17 | - | - | - | - |
| | | *(3)* | 34 | 34 | 34 | 34 | - | - | - | |
| 1,020-pin FineLine BGA | Transmitter | 88 *(2)* | 22 | 22 | 22 | 22 | 22 | 22 | 22 | 22 |
| | | *(3)* | 44 | 44 | 44 | 44 | - | - | - | - |
| | Receiver | 92 *(2)* | 23 | 23 | 23 | 23 | 23 | 23 | 23 | 23 |
| | | *(3)* | 46 | 46 | 46 | 46 | - | - | - | - |
| 1,508-pin FineLine BGA | Transmitter | 156 *(2)* | 37 | 41 | 41 | 37 | 37 | 41 | 41 | 37 |
| | | *(3)* | 78 | 78 | 78 | 78 | - | - | - | - |
| | Receiver | 156 *(2)* | 37 | 41 | 41 | 37 | 37 | 41 | 41 | 37 |
| | | *(3)* | 78 | 78 | 78 | 78 | - | - | - | - |

*Table 2–26. EP2S180 Differential Channels* *Note (1)*

| Package | Transmitter/ Receiver | Total Channels | Center Fast PLLs | | | | Corner Fast PLLs *(4)* | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | PLL 1 | PLL 2 | PLL 3 | PLL 4 | PLL 7 | PLL 8 | PLL 9 | PLL 10 |
| 1,020-pin FineLine BGA | Transmitter | 88 *(2)* | 22 | 22 | 22 | 22 | 22 | 22 | 22 | 22 |
| | | *(3)* | 44 | 44 | 44 | 44 | - | - | - | - |
| | Receiver | 92 *(2)* | 23 | 23 | 23 | 23 | 23 | 23 | 23 | 23 |
| | | *(3)* | 46 | 46 | 46 | 46 | - | - | - | - |
| 1,508-pin FineLine BGA | Transmitter | 156 *(2)* | 37 | 41 | 41 | 37 | 37 | 41 | 41 | 37 |
| | | *(3)* | 78 | 78 | 78 | 78 | - | - | - | - |
| | Receiver | 156 *(2)* | 37 | 41 | 41 | 37 | 37 | 41 | 41 | 37 |
| | | *(3)* | 78 | 78 | 78 | 78 | - | - | - | - |

***Notes to Tables 2–21 to 2–26:***

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

(2) This is the maximum number of channels the PLLs can directly drive.

(3) This is the maximum number of channels if the device uses cross bank channels from the adjacent center PLL.

(4) The channels accessible by the center fast PLL overlap with the channels accessible by the corner fast PLL. Therefore, the total number of channels is not the addition of the number of channels accessible by PLLs 1, 2, 3, and 4 with the number of channels accessible by PLLs 7, 8, 9, and 10.

*Table 5–2. Maximum Duty Cycles in Voltage Transitions*

| Symbol | Parameter | Condition | Maximum Duty Cycles | Unit |
|---|---|---|---|---|
| $V_I$ | Maximum duty cycles in voltage transitions | $V_I$ = 4.0 V | 100 | % |
| | | $V_I$ = 4.1 V | 90 | % |
| | | $V_I$ = 4.2 V | 50 | % |
| | | $V_I$ = 4.3 V | 30 | % |
| | | $V_I$ = 4.4 V | 17 | % |
| | | $V_I$ = 4.5 V | 10 | % |

## Recommended Operating Conditions

Table 5–3 contains the Stratix II device family recommended operating conditions.

*Table 5–3. Stratix II Device Recommended Operating Conditions (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic | 100 µs ≤ risetime ≤ 100 ms *(3)* | 1.15 | 1.25 | V |
| $V_{CCIO}$ | Supply voltage for input and output buffers, 3.3-V operation | 100 µs ≤ risetime ≤ 100 ms *(3)*, *(6)* | 3.135 (3.00) | 3.465 (3.60) | V |
| | Supply voltage for input and output buffers, 2.5-V operation | 100 µs ≤ risetime ≤ 100 ms *(3)* | 2.375 | 2.625 | V |
| | Supply voltage for input and output buffers, 1.8-V operation | 100 µs ≤ risetime ≤ 100 ms *(3)* | 1.71 | 1.89 | V |
| | Supply voltage for output buffers, 1.5-V operation | 100 µs ≤ risetime ≤ 100 ms *(3)* | 1.425 | 1.575 | V |
| | Supply voltage for input and output buffers, 1.2-V operation | 100 µs ≤ risetime ≤ 100 ms *(3)* | 1.14 | 1.26 | V |
| $V_{CCPD}$ | Supply voltage for pre-drivers as well as configuration and JTAG I/O buffers. | 100 µs ≤ risetime ≤ 100 ms *(4)* | 3.135 | 3.465 | V |
| $V_{CCA}$ | Analog power supply for PLLs | 100 µs ≤ risetime ≤ 100 ms *(3)* | 1.15 | 1.25 | V |
| $V_{CCD}$ | Digital power supply for PLLs | 100 µs ≤ risetime ≤ 100 ms *(3)* | 1.15 | 1.25 | V |
| $V_I$ | Input voltage (see Table 5–2) | *(2)*, *(5)* | –0.5 | 4.0 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |

*Table 5–19. SSTL-2 Class I Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 2.375 | 2.500 | 2.625 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{REF}$ | Reference voltage | | 1.188 | 1.250 | 1.313 | V |
| $V_{IH}$ (DC) | High-level DC input voltage | | $V_{REF}$ + 0.18 | | 3.00 | V |
| $V_{IL}$ (DC) | Low-level DC input voltage | | –0.30 | | $V_{REF}$ – 0.18 | V |
| $V_{IH}$ (AC) | High-level AC input voltage | | $V_{REF}$ + 0.35 | | | V |
| $V_{IL}$ (AC) | Low-level AC input voltage | | | | $V_{REF}$ - 0.35 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –8.1 mA *(1)* | $V_{TT}$ + 0.57 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8.1 mA *(1)* | | | $V_{TT}$ – 0.57 | V |

***Note to Table 5–19:***

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

*Table 5–20. SSTL-2 Class II Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 2.375 | 2.500 | 2.625 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{REF}$ | Reference voltage | | 1.188 | 1.250 | 1.313 | V |
| $V_{IH}$ (DC) | High-level DC input voltage | | $V_{REF}$ + 0.18 | | $V_{CCIO}$ + 0.30 | V |
| $V_{IL}$ (DC) | Low-level DC input voltage | | –0.30 | | $V_{REF}$ – 0.18 | V |
| $V_{IH}$ (AC) | High-level AC input voltage | | $V_{REF}$ + 0.35 | | | V |
| $V_{IL}$ (AC) | Low-level AC input voltage | | | | $V_{REF}$ - 0.35 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –16.4 mA *(1)* | $V_{TT}$ + 0.76 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 16.4 mA *(1)* | | | $V_{TT}$ – 0.76 | V |

***Note to Table 5–20:***

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

### *EP2S90 Clock Timing Parameters*

Tables 5–56 through 5–59 show the maximum clock timing parameters for EP2S90 devices.

***Table 5–56. EP2S90 Column Pins Regional Clock Timing Parameters***

| Parameter | Minimum Timing | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|---|---|---|---|---|---|---|
| | Industrial | Commercial | | | | |
| $t_{CIN}$ | 1.768 | 1.850 | 3.033 | 3.473 | 4.040 | ns |
| $t_{COUT}$ | 1.611 | 1.685 | 2.791 | 3.195 | 3.716 | ns |
| $t_{PLLCIN}$ | -0.127 | -0.117 | 0.125 | 0.129 | 0.144 | ns |
| $t_{PLLCOUT}$ | -0.284 | -0.282 | -0.117 | -0.149 | -0.18 | ns |

***Table 5–57. EP2S90 Column Pins Global Clock Timing Parameters***

| Parameter | Minimum Timing | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|---|---|---|---|---|---|---|
| | Industrial | Commercial | | | | |
| $t_{CIN}$ | 1.783 | 1.868 | 3.058 | 3.502 | 4.070 | ns |
| $t_{COUT}$ | 1.626 | 1.703 | 2.816 | 3.224 | 3.746 | ns |
| $t_{PLLCIN}$ | -0.137 | -0.127 | 0.115 | 0.119 | 0.134 | ns |
| $t_{PLLCOUT}$ | -0.294 | -0.292 | -0.127 | -0.159 | -0.19 | ns |

***Table 5–58. EP2S90 Row Pins Regional Clock Timing Parameters***

| Parameter | Minimum Timing | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|---|---|---|---|---|---|---|
| | Industrial | Commercial | | | | |
| $t_{CIN}$ | 1.566 | 1.638 | 2.731 | 3.124 | 3.632 | ns |
| $t_{COUT}$ | 1.571 | 1.643 | 2.727 | 3.120 | 3.627 | ns |
| $t_{PLLCIN}$ | -0.326 | -0.326 | -0.178 | -0.218 | -0.264 | ns |
| $t_{PLLCOUT}$ | -0.321 | -0.321 | -0.182 | -0.222 | -0.269 | ns |

*Table 5–74. Stratix II I/O Input Delay for Row Pins (Part 2 of 2)*

| I/O Standard | Parameter | Minimum Timing | | -3 Speed Grade (1) | -3 Speed Grade (2) | -4 Speed Grade | -5 Speed Grade | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Industrial | Commercial | | | | | |
| 1.5-V HSTL Class II | $t_{PI}$ | 602 | 631 | 1056 | 1107 | 1212 | 1413 | ps |
| | $t_{PCOUT}$ | 278 | 292 | 529 | 555 | 608 | 708 | ps |
| 1.8-V HSTL Class I | $t_{PI}$ | 577 | 605 | 960 | 1006 | 1101 | 1285 | ps |
| | $t_{PCOUT}$ | 253 | 266 | 433 | 454 | 497 | 580 | ps |
| 1.8-V HSTL Class II | $t_{PI}$ | 577 | 605 | 960 | 1006 | 1101 | 1285 | ps |
| | $t_{PCOUT}$ | 253 | 266 | 433 | 454 | 497 | 580 | ps |
| LVDS | $t_{PI}$ | 515 | 540 | 948 | 994 | 1088 | 1269 | ps |
| | $t_{PCOUT}$ | 191 | 201 | 421 | 442 | 484 | 564 | ps |
| HyperTransport | $t_{PI}$ | 515 | 540 | 948 | 994 | 1088 | 1269 | ps |
| | $t_{PCOUT}$ | 191 | 201 | 421 | 442 | 484 | 564 | ps |

*Notes for Table 5–74:*
(1) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(2) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

*Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 1 of 8)*

| I/O Standard | Drive Strength | Parameter | Minimum Timing | | -3 Speed Grade (3) | -3 Speed Grade (4) | -4 Speed Grade | -5 Speed Grade | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | | | | | |
| LVTTL | 4 mA | $t_{OP}$ | 1178 | 1236 | 2351 | 2467 | 2702 | 2820 | ps |
| | | $t_{DIP}$ | 1198 | 1258 | 2417 | 2537 | 2778 | 2910 | ps |
| | 8 mA | $t_{OP}$ | 1041 | 1091 | 2036 | 2136 | 2340 | 2448 | ps |
| | | $t_{DIP}$ | 1061 | 1113 | 2102 | 2206 | 2416 | 2538 | ps |
| | 12 mA | $t_{OP}$ | 976 | 1024 | 2036 | 2136 | 2340 | 2448 | ps |
| | | $t_{DIP}$ | 996 | 1046 | 2102 | 2206 | 2416 | 2538 | ps |
| | 16 mA | $t_{OP}$ | 951 | 998 | 1893 | 1986 | 2176 | 2279 | ps |
| | | $t_{DIP}$ | 971 | 1020 | 1959 | 2056 | 2252 | 2369 | ps |
| | 20 mA | $t_{OP}$ | 931 | 976 | 1787 | 1875 | 2054 | 2154 | ps |
| | | $t_{DIP}$ | 951 | 998 | 1853 | 1945 | 2130 | 2244 | ps |
| | 24 mA (1) | $t_{OP}$ | 924 | 969 | 1788 | 1876 | 2055 | 2156 | ps |
| | | $t_{DIP}$ | 944 | 991 | 1854 | 1946 | 2131 | 2246 | ps |

*Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 5 of 8)*

| I/O Standard | Drive Strength | Parameter | Minimum Timing | | -3 Speed Grade (3) | -3 Speed Grade (4) | -4 Speed Grade | -5 Speed Grade | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | | | | | |
| 1.8-V HSTL Class II | 16 mA | $t_{OP}$ | 877 | 919 | 1385 | 1453 | 1591 | 1680 | ps |
| | | $t_{DIP}$ | 897 | 941 | 1451 | 1523 | 1667 | 1770 | ps |
| | 18 mA | $t_{OP}$ | 879 | 921 | 1394 | 1462 | 1602 | 1691 | ps |
| | | $t_{DIP}$ | 899 | 943 | 1460 | 1532 | 1678 | 1781 | ps |
| | 20 mA (1) | $t_{OP}$ | 879 | 921 | 1402 | 1471 | 1611 | 1700 | ps |
| | | $t_{DIP}$ | 899 | 943 | 1468 | 1541 | 1687 | 1790 | ps |
| 1.5-V HSTL Class I | 4 mA | $t_{OP}$ | 912 | 956 | 1607 | 1686 | 1847 | 1942 | ps |
| | | $t_{DIP}$ | 932 | 978 | 1673 | 1756 | 1923 | 2032 | ps |
| | 6 mA | $t_{OP}$ | 917 | 961 | 1588 | 1666 | 1825 | 1920 | ps |
| | | $t_{DIP}$ | 937 | 983 | 1654 | 1736 | 1901 | 2010 | ps |
| | 8 mA | $t_{OP}$ | 899 | 943 | 1590 | 1668 | 1827 | 1922 | ps |
| | | $t_{DIP}$ | 919 | 965 | 1656 | 1738 | 1903 | 2012 | ps |
| | 10 mA | $t_{OP}$ | 900 | 943 | 1592 | 1670 | 1829 | 1924 | ps |
| | | $t_{DIP}$ | 920 | 965 | 1658 | 1740 | 1905 | 2014 | ps |
| | 12 mA (1) | $t_{OP}$ | 893 | 937 | 1590 | 1668 | 1827 | 1922 | ps |
| | | $t_{DIP}$ | 913 | 959 | 1656 | 1738 | 1903 | 2012 | ps |
| 1.5-V HSTL Class II | 16 mA | $t_{OP}$ | 881 | 924 | 1431 | 1501 | 1644 | 1734 | ps |
| | | $t_{DIP}$ | 901 | 946 | 1497 | 1571 | 1720 | 1824 | ps |
| | 18 mA | $t_{OP}$ | 884 | 927 | 1439 | 1510 | 1654 | 1744 | ps |
| | | $t_{DIP}$ | 904 | 949 | 1505 | 1580 | 1730 | 1834 | ps |
| | 20 mA (1) | $t_{OP}$ | 886 | 929 | 1450 | 1521 | 1666 | 1757 | ps |
| | | $t_{DIP}$ | 906 | 951 | 1516 | 1591 | 1742 | 1847 | ps |
| 1.2-V HSTL | | $t_{OP}$ | 958 | 1004 | 1602 | 1681 | - | - | ps |
| | | $t_{DIP}$ | 978 | 1026 | 1668 | 1751 | - | - | ps |
| PCI | | $t_{OP}$ | 1028 | 1082 | 1956 | 2051 | 2244 | 2070 | ps |
| | | $t_{DIP}$ | 1048 | 1104 | 2022 | 2121 | 2320 | 2160 | ps |
| PCI-X | | $t_{OP}$ | 1028 | 1082 | 1956 | 2051 | 2244 | 2070 | ps |
| | | $t_{DIP}$ | 1048 | 1104 | 2022 | 2121 | 2320 | 2160 | ps |

*Table 5–76. Stratix II I/O Output Delay for Row Pins (Part 2 of 3)*

| I/O Standard | Drive Strength | Parameter | Minimum Timing | | -3 Speed Grade (2) | -3 Speed Grade (3) | -4 Speed Grade | -5 Speed Grade | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | | | | | |
| 2.5 V | 4 mA | $t_{OP}$ | 1128 | 1183 | 2091 | 2194 | 2403 | 2523 | ps |
| | | $t_{DIP}$ | 1086 | 1140 | 2036 | 2137 | 2340 | 2450 | ps |
| | 8 mA | $t_{OP}$ | 1030 | 1080 | 1872 | 1964 | 2152 | 2265 | ps |
| | | $t_{DIP}$ | 988 | 1037 | 1817 | 1907 | 2089 | 2192 | ps |
| | 12 mA (1) | $t_{OP}$ | 1012 | 1061 | 1775 | 1862 | 2040 | 2151 | ps |
| | | $t_{DIP}$ | 970 | 1018 | 1720 | 1805 | 1977 | 2078 | ps |
| 1.8 V | 2 mA | $t_{OP}$ | 1196 | 1253 | 2954 | 3100 | 3396 | 3542 | ps |
| | | $t_{DIP}$ | 1154 | 1210 | 2899 | 3043 | 3333 | 3469 | ps |
| | 4 mA | $t_{OP}$ | 1184 | 1242 | 2294 | 2407 | 2637 | 2763 | ps |
| | | $t_{DIP}$ | 1142 | 1199 | 2239 | 2350 | 2574 | 2690 | ps |
| | 6 mA | $t_{OP}$ | 1079 | 1131 | 2039 | 2140 | 2344 | 2462 | ps |
| | | $t_{DIP}$ | 1037 | 1088 | 1984 | 2083 | 2281 | 2389 | ps |
| | 8 mA (1) | $t_{OP}$ | 1049 | 1100 | 1942 | 2038 | 2232 | 2348 | ps |
| | | $t_{DIP}$ | 1007 | 1057 | 1887 | 1981 | 2169 | 2275 | ps |
| 1.5 V | 2 mA | $t_{OP}$ | 1158 | 1213 | 2530 | 2655 | 2908 | 3041 | ps |
| | | $t_{DIP}$ | 1116 | 1170 | 2475 | 2598 | 2845 | 2968 | ps |
| | 4 mA | $t_{OP}$ | 1055 | 1106 | 2020 | 2120 | 2322 | 2440 | ps |
| | | $t_{DIP}$ | 1013 | 1063 | 1965 | 2063 | 2259 | 2367 | ps |
| SSTL-2 Class I | 8 mA | $t_{OP}$ | 1002 | 1050 | 1759 | 1846 | 2022 | 2104 | ps |
| | | $t_{DIP}$ | 960 | 1007 | 1704 | 1789 | 1959 | 2031 | ps |
| SSTL-2 Class II | 16 mA (1) | $t_{OP}$ | 947 | 992 | 1581 | 1659 | 1817 | 1897 | ps |
| | | $t_{DIP}$ | 905 | 949 | 1526 | 1602 | 1754 | 1824 | ps |
| SSTL-18 Class I | 4 mA | $t_{OP}$ | 990 | 1038 | 1709 | 1793 | 1964 | 2046 | ps |
| | | $t_{DIP}$ | 948 | 995 | 1654 | 1736 | 1901 | 1973 | ps |
| | 6 mA | $t_{OP}$ | 994 | 1042 | 1648 | 1729 | 1894 | 1975 | ps |
| | | $t_{DIP}$ | 952 | 999 | 1593 | 1672 | 1831 | 1902 | ps |
| | 8 mA | $t_{OP}$ | 970 | 1018 | 1633 | 1713 | 1877 | 1958 | ps |
| | | $t_{DIP}$ | 928 | 975 | 1578 | 1656 | 1814 | 1885 | ps |
| | 10 mA (1) | $t_{OP}$ | 974 | 1021 | 1615 | 1694 | 1856 | 1937 | ps |
| | | $t_{DIP}$ | 932 | 978 | 1560 | 1637 | 1793 | 1864 | ps |

*Table 5–80. Maximum DCD for Non-DDIO Output on Row I/O Pins (Part 2 of 2)* *Note (1)*

| Row I/O Output Standard | Maximum DCD for Non-DDIO Output | | |
|---|---|---|---|
| | -3 Devices | -4 & -5 Devices | Unit |
| 1.8 V | 180 | 180 | ps |
| 1.5-V LVCMOS | 165 | 195 | ps |
| SSTL-2 Class I | 115 | 145 | ps |
| SSTL-2 Class II | 95 | 125 | ps |
| SSTL-18 Class I | 55 | 85 | ps |
| 1.8-V HSTL Class I | 80 | 100 | ps |
| 1.5-V HSTL Class I | 85 | 115 | ps |
| LVDS/ HyperTransport technology | 55 | 80 | ps |

***Note to Table 5–80:***

(1) The DCD specification is based on a no logic array noise condition.

Here is an example for calculating the DCD as a percentage for a non-DDIO output on a row I/O on a -3 device:

If the non-DDIO output I/O standard is SSTL-2 Class II, the maximum DCD is 95 ps (see Table 5–80). If the clock frequency is 267 MHz, the clock period T is:

$$T = 1/ f = 1 / 267 \text{ MHz} = 3.745 \text{ ns} = 3745 \text{ ps}$$

To calculate the DCD as a percentage:

$$(T/2 - DCD) / T = (3745ps/2 - 95ps) / 3745ps = 47.5\% \text{ (for low boundary)}$$

$$(T/2 + DCD) / T = (3745ps/2 + 95ps) / 3745ps = 52.5\% \text{ (for high boundary)}$$