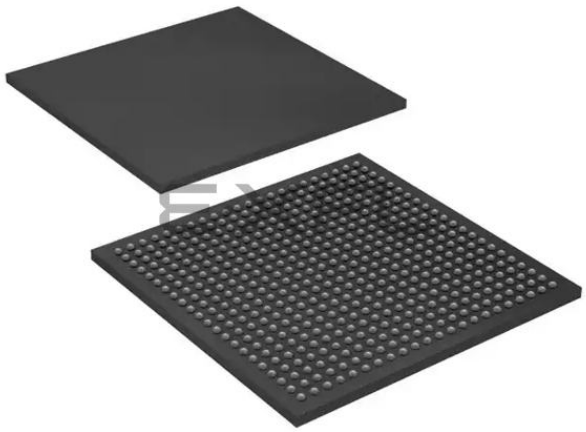

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1694
Number of Logic Elements/Cells	33880
Total RAM Bits	1369728
Number of I/O	342
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s30f484i4

Chapter 3. Configuration & Testing

Chapter 4. Hot Socketing & Power-On Reset

Chapter 5. DC & Switching Characteristics

Stratix II devices are available in space-saving FineLine BGA® packages (see Tables 1–2 and 1–3).

Table 1–2. Stratix II Package Options & I/O Pin Counts *Notes (1), (2)*

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	342		366			
EP2S30	342		500			
EP2S60 *(3)*	334		492		718	
EP2S90 *(3)*		308		534	758	902
EP2S130 *(3)*				534	742	1,126
EP2S180 *(3)*					742	1,170

Notes to Table 1–2:

(1) All I/O pin counts include eight dedicated clock input pins (`clk1p`, `clk1n`, `clk3p`, `clk3n`, `clk9p`, `clk9n`, `clk11p`, and `clk11n`) that can be used for data inputs.

(2) The Quartus II software I/O pin counts include one additional pin, `PLL_ENA`, which is not available as general-purpose I/O pins. The `PLL_ENA` pin can only be used to enable the PLLs within the device.

(3) The I/O pin counts for the EP2S60, EP2S90, EP2S130, and EP2S180 devices in the 1020-pin and 1508-pin packages include eight dedicated fast PLL clock inputs (`FPLL7CLKp/n`, `FPLL8CLKp/n`, `FPLL9CLKp/n`, and `FPLL10CLKp/n`) that can be used for data inputs.

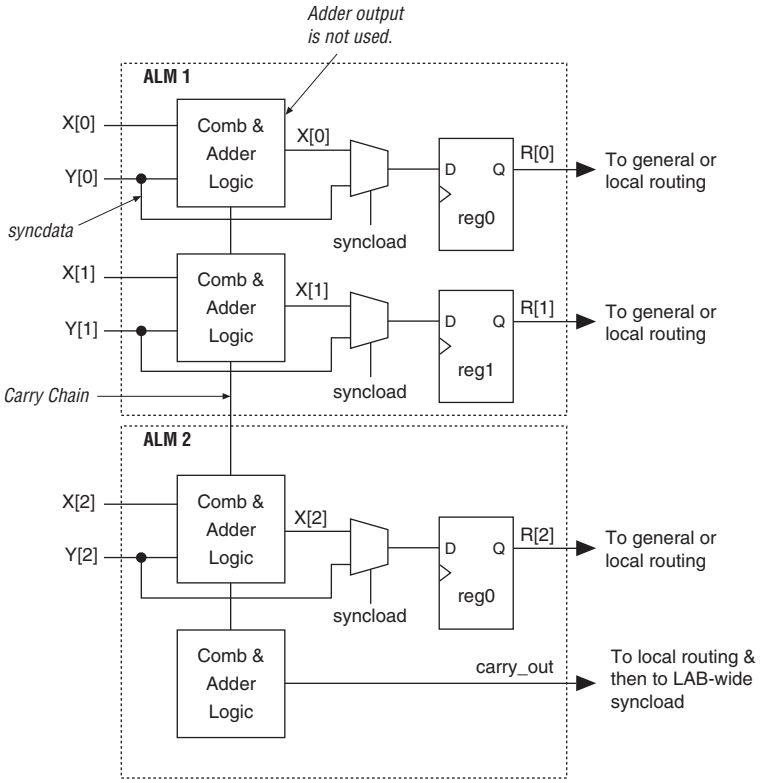
Table 1–3. Stratix II FineLine BGA Package Sizes

Dimension	484 Pin	484-Pin Hybrid	672 Pin	780 Pin	1,020 Pin	1,508 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00
Area (mm2)	529	729	729	841	1,089	1,600
Length × width (mm × mm)	23 × 23	27 × 27	27 × 27	29 × 29	33 × 33	40 × 40

All Stratix II devices support vertical migration within the same package (for example, you can migrate between the EP2S15, EP2S30, and EP2S60 devices in the 672-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

To ensure that a board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus II software (Assignments menu > Device > Migration Devices).

Figure 2–12. Conditional Operation Example



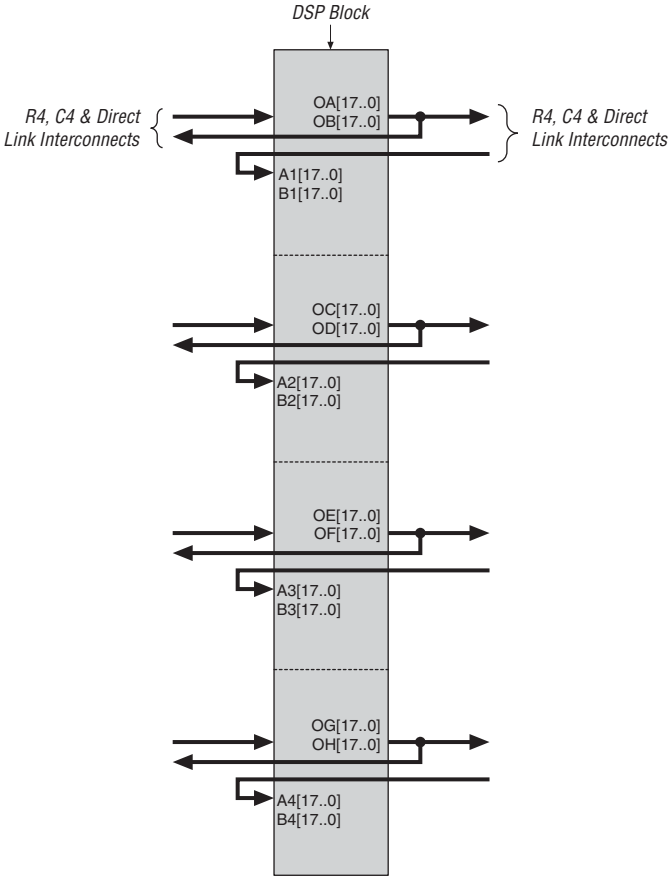
The arithmetic mode also offers clock enable, counter enable, synchronous up/down control, add/subtract control, synchronous clear, synchronous load. The LAB local interconnect data inputs generate the clock enable, counter enable, synchronous up/down and add/subtract control signals. These control signals are good candidates for the inputs that are shared between the four LUTs in the ALM. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Carry Chain

The carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. Carry chains can begin in either the first ALM or the fifth ALM in an LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

The DSP block is divided into four block units that interface with four LAB rows on the left and right. Each block unit can be considered one complete 18 × 18-bit multiplier with 36 inputs and 36 outputs. A local interconnect region is associated with each DSP block. Like an LAB, this interconnect region can be fed with 16 direct link interconnects from the LAB to the left or right of the DSP block in the same row. R4 and C4 routing resources can access the DSP block's local interconnect region. The outputs also work similarly to LAB outputs as well. Eighteen outputs from the DSP block can drive to the left LAB through direct link interconnects and eighteen can drive to the right LAB though direct link interconnects. All 36 outputs can drive to R4 and C4 routing interconnects. Outputs can drive right- or left-column routing. Figures 2–29 and 2–30 show the DSP block interfaces to LAB rows.

Figure 2–29. DSP Block Interconnect Interface



PLLs & Clock Networks

Stratix II devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global & Hierarchical Clocking

Stratix II devices provide 16 dedicated global clock networks and 32 regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to 24 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains in Stratix II devices.

There are 16 dedicated clock pins (CLK[15..0]) to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in Figures 2–31 and 2–32. Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block, which controls the selection of the clock source and dynamically enables/disables the clock to reduce power consumption. Table 2–8 shows global and regional clock features.

Table 2–8. Global & Regional Clock Features

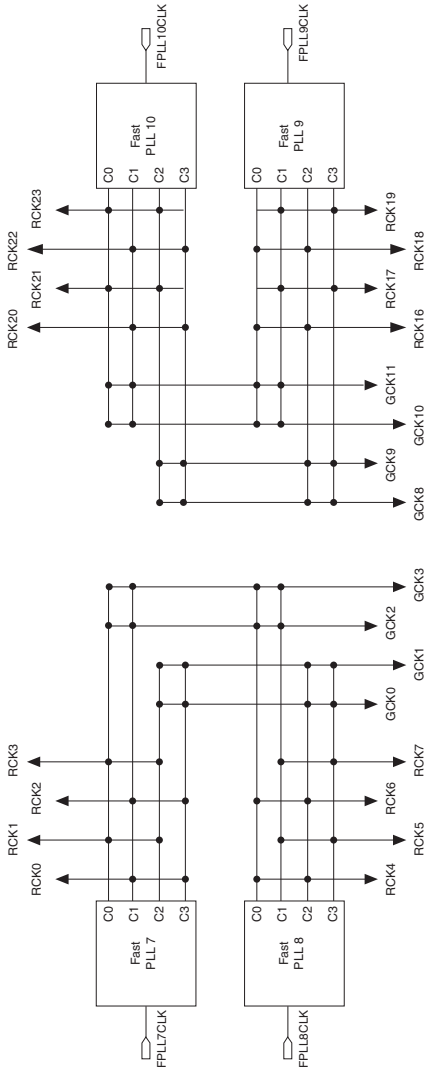
Feature	Global Clocks	Regional Clocks
Number per device	16	32
Number available per quadrant	16	8
Sources	CLK pins, PLL outputs, or internal logic	CLK pins, PLL outputs, or internal logic
Dynamic clock source selection	✓ (1)	
Dynamic enable/disable	✓	✓

Note to Table 2–8:
(1) Dynamic source clock selection is supported for selecting between CLKp pins and PLL outputs only.

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources in the device-IOEs, ALMs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The

Figure 2–42. Global & Regional Clock Connections from Corner Clock Pins & Fast PLL Outputs *Note (1)*



Note to Figure 2–42:

(1) The corner fast PLLs can also be driven through the global or regional clock networks. The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

The Stratix II device IOE includes programmable delays that can be activated to ensure input IOE register-to-logic array register transfers, input pin-to-logic array register transfers, or output IOE register-to-pin transfers.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output and/or output enable registers. Programmable delays are no longer required to ensure zero hold times for logic array register-to-IOE register transfers. The Quartus II Compiler can create the zero hold time for these transfers. Table 2–13 shows the programmable delays for Stratix II devices.

Table 2–13. Stratix II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin
Output enable register t_{CO} delay	Delay to output enable pin

The IOE registers in Stratix II devices share the same source for clear or preset. You can program preset or clear for each individual IOE. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

Double Data Rate I/O Pins

Stratix II devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Stratix II devices support DDR inputs, DDR outputs, and bidirectional DDR modes.

- 1.5-V HSTL Class I and II
- 1.8-V HSTL Class I and II
- 1.2-V HSTL
- SSTL-2 Class I and II
- SSTL-18 Class I and II

Table 2–16 describes the I/O standards supported by Stratix II devices.

Table 2–16. Stratix II Supported I/O Standards (Part 1 of 2)

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	-	3.3	-
LVCMOS	Single-ended	-	3.3	-
2.5 V	Single-ended	-	2.5	-
1.8 V	Single-ended	-	1.8	-
1.5-V LVCMOS	Single-ended	-	1.5	-
3.3-V PCI	Single-ended	-	3.3	-
3.3-V PCI-X mode 1	Single-ended	-	3.3	-
LVDS	Differential	-	2.5 *(3)*	-
LVPECL *(1)*	Differential	-	3.3	-
HyperTransport technology	Differential	-	2.5	-
Differential 1.5-V HSTL Class I and II *(2)*	Differential	0.75	1.5	0.75
Differential 1.8-V HSTL Class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-18 Class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-2 Class I and II *(2)*	Differential	1.25	2.5	1.25
1.2-V HSTL*(4)*	Voltage-referenced	0.6	1.2	0.6
1.5-V HSTL Class I and II	Voltage-referenced	0.75	1.5	0.75
1.8-V HSTL Class I and II	Voltage-referenced	0.9	1.8	0.9
SSTL-18 Class I and II	Voltage-referenced	0.90	1.8	0.90

Table 2–16. Stratix II Supported I/O Standards (Part 2 of 2)

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
SSTL-2 Class I and II	Voltage-referenced	1.25	2.5	1.25

Notes to Table 2–16:

(1) This I/O standard is only available on input and output column clock pins.

(2) This I/O standard is only available on input clock pins and DQS pins in I/O banks 3, 4, 7, and 8, and output clock pins in I/O banks 9,10, 11, and 12.

(3) V_{CCIO} is 3.3 V when using this I/O standard in input and output column clock pins (in I/O banks 9, 10, 11, and 12). The clock input pins supporting LVDS on banks 3, 4, 7, and 8 use V_{CCINT} for LVDS input operations and have no dependency on the V_{CCIO} level of the bank.

(4) 1.2-V HSTL is only supported in I/O banks 4,7, and 8.

For more information on I/O standards supported by Stratix II I/O banks, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

Stratix II devices contain eight I/O banks and four enhanced PLL external clock output banks, as shown in Figure 2–57. The four I/O banks on the right and left of the device contain circuitry to support high-speed differential I/O for LVDS and HyperTransport inputs and outputs. These banks support all Stratix II I/O standards except PCI or PCI-X I/O pins, and SSTL-18 Class II and HSTL outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, enhanced PLL external clock output banks allow clock output capabilities such as differential support for SSTL and HSTL.

Table 3–1. Stratix II JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring a Stratix II device via the JTAG port with a USB Blaster, MasterBlaster™, ByteBlasterMV™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Notes to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information on using the CONFIG_IO instruction, see the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper.*

Configuring Stratix II FPGAs with the MicroBlaster Driver

The MicroBlaster™ software driver supports an RBF programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems. For more information on the MicroBlaster software driver, see the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *Configuring the MicroBlaster Passive Serial Software Driver White Paper* on the Altera web site (**www.altera.com**).

PLL Reconfiguration

The phase-locked loops (PLLs) in the Stratix II device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.

See the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information on Stratix II PLLs.

Temperature Sensing Diode (TSD)

Stratix II devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device. These devices steer bias current through the Stratix II diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus sign). The external device's output represents the junction temperature of the Stratix II device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix II device to connect to the external temperature-sensing device, as shown in Figure 3–1. The temperature sensing diode is a passive element and therefore can be used before the Stratix II device is powered.

Table 5–14. 3.3-V PCI Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low-level input voltage		–0.3		$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–15. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.30		$0.35 \times V_{CCIO}$	V
V_{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–16. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Reference voltage		0.855	0.900	0.945	V
V_{TT}	Termination voltage		$V_{REF} – 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{IH} (DC)	High-level DC input voltage		$V_{REF} + 0.125$			V
V_{IL} (DC)	Low-level DC input voltage				$V_{REF} – 0.125$	V
V_{IH} (AC)	High-level AC input voltage		$V_{REF} + 0.25$			V
V_{IL} (AC)	Low-level AC input voltage				$V_{REF} – 0.25$	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	$V_{TT} + 0.475$			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*			$V_{TT} – 0.475$	V

Note to Table 5–16:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–38. IOE Internal Timing Microparameters

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min (3)	Max	Min (3)	Max	Min (4)	Max	Min (3)	Max	
t_{SU}	IOE input and output register setup time before clock	122		128		140 140		163		ps
t_{H}	IOE input and output register hold time after clock	72		75		82 82		96		ps
t_{CO}	IOE input and output register clock-to-output delay	101	169	101	177	97 101	194	101	226	ps
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinational output	410	760	410	798	391 410	873	410	1,018	ps
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinational output	428	787	428	825	408 428	904	428	1,054	ps
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinational output pin	1,101	2,026	1,101	2,127	1,049 1,101	2,329	1,101	2,439	ps
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinational output pin	991	1,854	991	1,946	944 991	2,131	991	2,246	ps
t_{CLR}	Minimum clear pulse width	200		210		229 229		268		ps
t_{PRE}	Minimum preset pulse width	200		210		229 229		268		ps
t_{CLKL}	Minimum clock low time	600		630		690 690		804		ps
t_{CLKH}	Minimum clock high time	600		630		690 690		804		ps

Notes to Table 5–38:

(1) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.

(2) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

(3) For the -3 and -5 speed grades, the minimum timing is for the commercial temperature grade. Only -4 speed grade devices offer the industrial temperature grade.

(4) For the -4 speed grade, the first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.

Table 5–50. EP2S30 Row Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.304	1.184	1.966	2.251	2.616	ns
t_{COUT}	1.309	1.189	1.962	2.247	2.611	ns
t_{PLLCIN}	-0.135	–0.158	–0.208	–0.254	–0.302	ns
$t_{PLLCOUT}$	-0.13	–0.153	–0.212	–0.258	–0.307	ns

Table 5–51. EP2S30 Row Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.289	1.352	2.238	2.567	2.990	ns
t_{COUT}	1.294	1.357	2.234	2.563	2.985	ns
t_{PLLCIN}	-0.14	-0.154	-0.169	-0.205	-0.254	ns
$t_{PLLCOUT}$	-0.135	-0.149	-0.173	-0.209	-0.259	ns

EP2S60 Clock Timing Parameters

Tables 5–52 through 5–55 show the maximum clock timing parameters for EP2S60 devices.

Table 5–52. EP2S60 Column Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.681	1.762	2.945	3.381	3.931	ns
t_{COUT}	1.524	1.597	2.703	3.103	3.607	ns
t_{PLLCIN}	0.066	0.064	0.279	0.311	0.348	ns
$t_{PLLCOUT}$	-0.091	-0.101	0.037	0.033	0.024	ns

Table 5–70. Stratix II IOE Programmable Delay on Row Pins *Note (1)*

Parameter	Paths Affected	Available Settings	Minimum Timing *(2)*		-3 Speed Grade *(3)*		-4 Speed Grade		-5 Speed Grade	
			Min Offset (ps)	Max Offset (ps)	Min Offset (ps)	Max Offset (ps)	Min Offset (ps)	Max Offset (ps)	Min Offset (ps)	Max Offset (ps)
Input delay from pin to internal cells	Pad to I/O dataout to logic array	8	0 0	1,697 1,782	0 0	2,876 3,020	0	3,308	0	3,853
Input delay from pin to input register	Pad to I/O input register	64	0 0	1,956 2,054	0 0	3,270 3,434	0	3,761	0	4,381
Delay from output register to output pin	I/O output register to pad	2	0 0	316 332	0 0	525 525	0	575	0	670
Output enable pin delay	t_{XZ}, t_{ZX}	2	0 0	305 320	0 0	507 507	0	556	0	647

Notes to Table 5–70:

(1) The incremental values for the settings are generally linear. For the exact delay associated with each setting, use the latest version of the Quartus II software.

(2) The first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.

(3) The first number applies to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices. The second number applies to -3 speed grade EP2S130 and EP2S180 devices.

Default Capacitive Loading of Different I/O Standards

See Table 5–71 for default capacitive loading of different I/O standards.

Table 5–71. Default Loading of Different I/O Standards for Stratix II (Part 1 of 2)

I/O Standard	Capacitive Load	Unit
LVTTL	0	pF
LVCMOS	0	pF
2.5 V	0	pF
1.8 V	0	pF
1.5 V	0	pF
PCI	10	pF
PCI-X	10	pF
SSTL-2 Class I	0	pF

Table 5–73. Stratix II I/O Input Delay for Column Pins (Part 2 of 3)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
1.5-V HSTL Class II	t_{PI}	560	587	993	1041	1141	1329	ps
	t_{PCOUT}	294	308	557	584	640	746	ps
1.8-V HSTL Class I	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.8-V HSTL Class II	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
PCI	t_{PI}	679	712	1214	1273	1395	1625	ps
	t_{PCOUT}	413	433	778	816	894	1042	ps
PCI-X	t_{PI}	679	712	1214	1273	1395	1625	ps
	t_{PCOUT}	413	433	778	816	894	1042	ps
Differential SSTL-2 Class I (1)	t_{PI}	507	530	818	857	939	1094	ps
	t_{PCOUT}	241	251	382	400	438	511	ps
Differential SSTL-2 Class II (1)	t_{PI}	507	530	818	857	939	1094	ps
	t_{PCOUT}	241	251	382	400	438	511	ps
Differential SSTL-18 Class I (1)	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
Differential SSTL-18 Class II (1)	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.8-V Differential HSTL Class I (1)	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.8-V Differential HSTL Class II (1)	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.5-V Differential HSTL Class I (1)	t_{PI}	560	587	993	1041	1141	1329	ps
	t_{PCOUT}	294	308	557	584	640	746	ps
1.5-V Differential HSTL Class II (1)	t_{PI}	560	587	993	1041	1141	1329	ps
	t_{PCOUT}	294	308	557	584	640	746	ps

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 2 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
LVCMOS	4 mA	t_{OP}	1041	1091	2036	2136	2340	2448	ps
		t_{DIP}	1061	1113	2102	2206	2416	2538	ps
	8 mA	t_{OP}	952	999	1786	1874	2053	2153	ps
		t_{DIP}	972	1021	1852	1944	2129	2243	ps
	12 mA	t_{OP}	926	971	1720	1805	1977	2075	ps
		t_{DIP}	946	993	1786	1875	2053	2165	ps
	16 mA	t_{OP}	933	978	1693	1776	1946	2043	ps
		t_{DIP}	953	1000	1759	1846	2022	2133	ps
	20 mA	t_{OP}	921	965	1677	1759	1927	2025	ps
		t_{DIP}	941	987	1743	1829	2003	2115	ps
	24 mA (1)	t_{OP}	909	954	1659	1741	1906	2003	ps
		t_{DIP}	929	976	1725	1811	1982	2093	ps
2.5 V	4 mA	t_{OP}	1004	1053	2063	2165	2371	2480	ps
		t_{DIP}	1024	1075	2129	2235	2447	2570	ps
	8 mA	t_{OP}	955	1001	1841	1932	2116	2218	ps
		t_{DIP}	975	1023	1907	2002	2192	2308	ps
	12 mA	t_{OP}	934	980	1742	1828	2002	2101	ps
		t_{DIP}	954	1002	1808	1898	2078	2191	ps
	16 mA (1)	t_{OP}	918	962	1679	1762	1929	2027	ps
		t_{DIP}	938	984	1745	1832	2005	2117	ps

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 1 of 5) *Note (1)*

I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVTTL	4 mA	270	225	210	270	225	210	270	225	210
	8 mA	435	355	325	435	355	325	435	355	325
	12 mA	580	475	420	580	475	420	580	475	420
	16 mA	720	594	520	-	-	-	720	594	520
	20 mA	875	700	610	-	-	-	875	700	610
	24 mA	1,030	794	670	-	-	-	1,030	794	670
3.3-V LVCMOS	4 mA	290	250	230	290	250	230	290	250	230
	8 mA	565	480	440	565	480	440	565	480	440
	12 mA	790	710	670	-	-	-	790	710	670
	16 mA	1,020	925	875	-	-	-	1,020	925	875
	20 mA	1,066	985	935	-	-	-	1,066	985	935
	24 mA	1,100	1,040	1,000	-	-	-	1,100	1,040	1,000
2.5-V LVTTL/LVCMOS	4 mA	230	194	180	230	194	180	230	194	180
	8 mA	430	380	380	430	380	380	430	380	380
	12 mA	630	575	550	630	575	550	630	575	550
	16 mA	930	845	820	-	-	-	930	845	820
1.8-V LVTTL/LVCMOS	2 mA	120	109	104	120	109	104	120	109	104
	4 mA	285	250	230	285	250	230	285	250	230
	6 mA	450	390	360	450	390	360	450	390	360
	8 mA	660	570	520	660	570	520	660	570	520
	10 mA	905	805	755	-	-	-	905	805	755
	12 mA	1,131	1,040	990	-	-	-	1,131	1,040	990
1.5-V LVTTL/LVCMOS	2 mA	244	200	180	244	200	180	244	200	180
	4 mA	470	370	325	470	370	325	470	370	325
	6 mA	550	430	375	-	-	-	550	430	375
	8 mA	625	495	420	-	-	-	625	495	420
SSTL-2 Class I	8 mA	400	300	300	-	-	-	400	300	300
	12 mA	400	400	350	400	350	350	400	400	350
SSTL-2 Class II	16 mA	350	350	300	350	350	300	350	350	300
	20 mA	400	350	350	-	-	-	400	350	350
	24 mA	400	400	350	-	-	-	400	400	350

Table 5–85. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -4 & -5 Devices (Part 2 of 2) *Notes (1), (2)*

DDIO Column Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)				Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	
SSTL-18 Class I	335	390	65	65	ps
SSTL-18 Class II	320	375	70	80	ps
1.8-V HSTL Class I	330	385	60	70	ps
1.8-V HSTL Class II	330	385	60	70	ps
1.5-V HSTL Class I	330	390	60	70	ps
1.5-V HSTL Class II	330	360	90	100	ps
1.2-V HSTL	420	470	155	165	ps
LVPECL	180	180	180	180	ps

Notes to Table 5–85:
(1) Table 5–85 assumes the input clock has zero DCD.
(2) The DCD specification is based on a no logic array noise condition.

Table 5–86. Maximum DCD for DDIO Output on Row I/O Pins with PLL in the Clock Path (Part 1 of 2) *Note (1)*

Row DDIO Output I/O Standard	Maximum DCD (PLL Output Clock Feeding DDIO Clock Port)		Unit
	-3 Device	-4 & -5 Device	
3.3-V LVTTL	110	105	ps
3.3-V LVCMOS	65	75	ps
2.5V	75	90	ps
1.8V	85	100	ps
1.5-V LVCMOS	105	100	ps
SSTL-2 Class I	65	75	ps
SSTL-2 Class II	60	70	ps
SSTL-18 Class I	50	65	ps
1.8-V HSTL Class I	50	70	ps
1.5-V HSTL Class I	55	70	ps

Table 5–100. DQS Phase Offset Delay Per Stage Notes (1), (2), (3)			
Speed Grade	**Min**	**Max**	**Unit**
-3	9	14	ps
-4	9	14	ps
-5	9	15	ps

Notes to Table 5–100:
(1) The delay settings are linear.
(2) The valid settings for phase offset are -64 to +63 for frequency mode 0 and -32 to +31 for frequency modes 1, 2, and 3.
(3) The typical value equals the average of the minimum and maximum values.

Table 5–101. DDIO Outputs Half-Period Jitter Notes (1), (2)			
Name	**Description**	**Max**	**Unit**
$t_{OUTHALFJITTER}$	Half-period jitter (PLL driving DDIO outputs)	200	ps

Notes to Table 5–101:
(1) The worst-case half period is equal to the ideal half period subtracted by the DCD and half-period jitter values.
(2) The half-period jitter was characterized using a PLL driving DDIO outputs.

JTAG Timing Specifications

Figure 5–10 shows the timing requirements for the JTAG signals.

Figure 5–10. Stratix II JTAG Waveforms