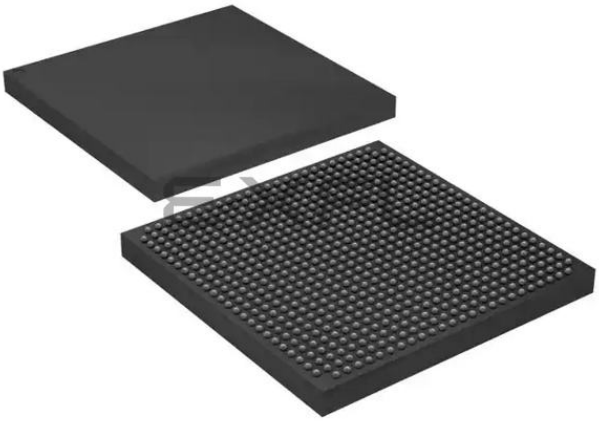
Intel - EP2S30F672I4 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1694
Number of Logic Elements/Cells	33880
Total RAM Bits	1369728
Number of I/O	500
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s30f672i4

The number of M512 RAM, M4K RAM, and DSP blocks varies by device along with row and column numbers and M-RAM blocks. Table 2–1 lists the resources available in Stratix II devices.

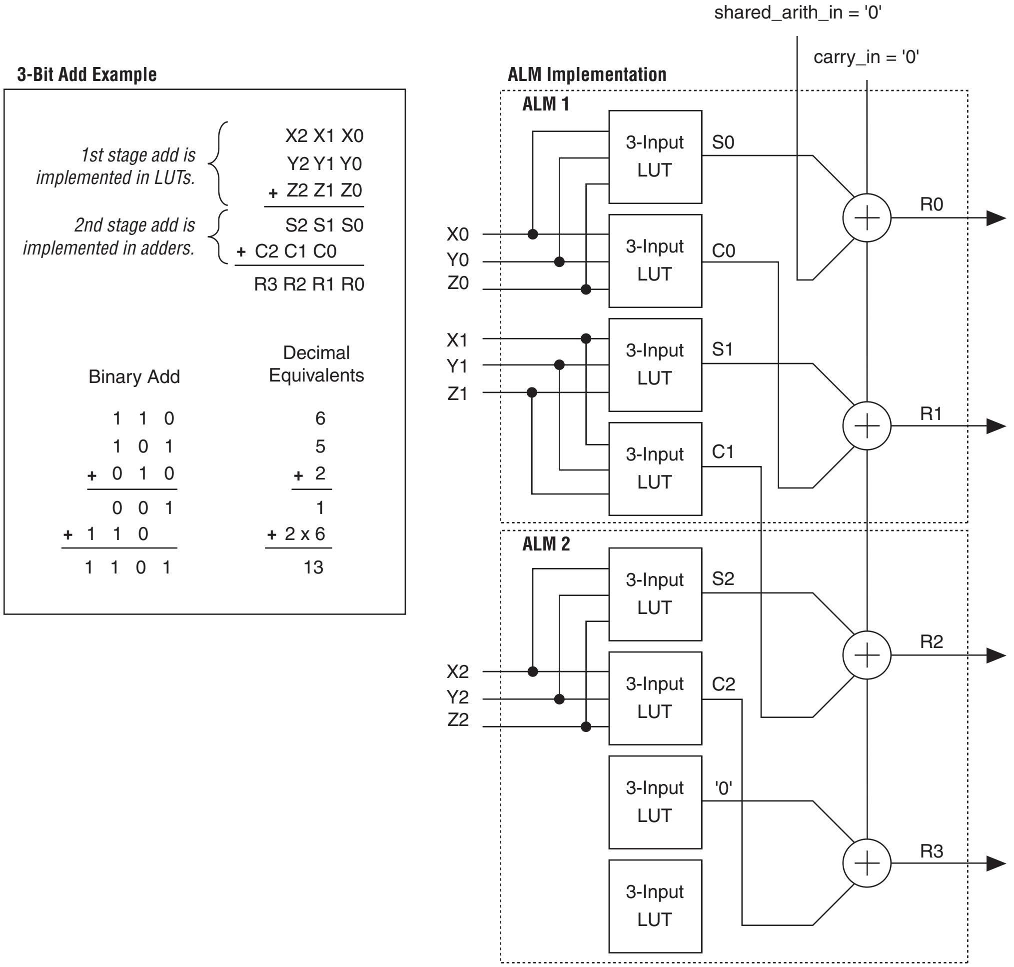
Table 2–1. Stratix II Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks	LAB Columns	LAB Rows
EP2S15	4 / 104	3 / 78	0	2 / 12	30	26
EP2S30	6 / 202	4 / 144	1	2 / 16	49	36
EP2S60	7 / 329	5 / 255	2	3 / 36	62	51
EP2S90	8 / 488	6 / 408	4	3 / 48	71	68
EP2S130	9 / 699	7 / 609	6	3 / 63	81	87
EP2S180	11 / 930	8 / 768	9	4 / 96	100	96

Logic Array Blocks

Each LAB consists of eight ALMs, carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines. The local interconnect transfers signals between ALMs in the same LAB. Register chain connections transfer the output of an ALM register to the adjacent ALM register in an LAB. The Quartus® II Compiler places associated logic in an LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency. Figure 2–2 shows the Stratix II LAB structure.

Figure 2–14. Example of a 3-bit Add Utilizing Shared Arithmetic Mode



Shared Arithmetic Chain

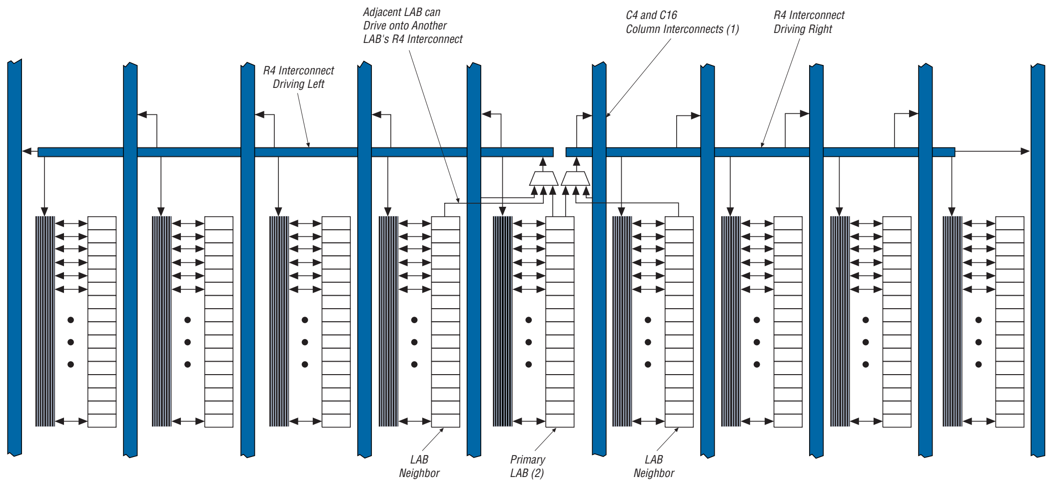
In addition to the dedicated carry chain routing, the shared arithmetic chain available in shared arithmetic mode allows the ALM to implement a three-input add. This significantly reduces the resources necessary to implement large adder trees or correlator functions.

The shared arithmetic chains can begin in either the first or fifth ALM in an LAB. The Quartus II Compiler creates shared arithmetic chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long shared

The direct link interconnect allows an LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself. This provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–16 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by DSP blocks and RAM blocks and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

Figure 2–16. R4 Interconnect Connections *Notes (1), (2), (3)*



Notes to Figure 2–16:
(1) C4 and C16 interconnects can drive R4 interconnects.
(2) This pattern is repeated for every LAB in the LAB row.
(3) The LABs in Figure 2–16 show the 16 possible logical outputs per LAB.

Figure 2–26. M-RAM Row Unit Interface to Interconnect

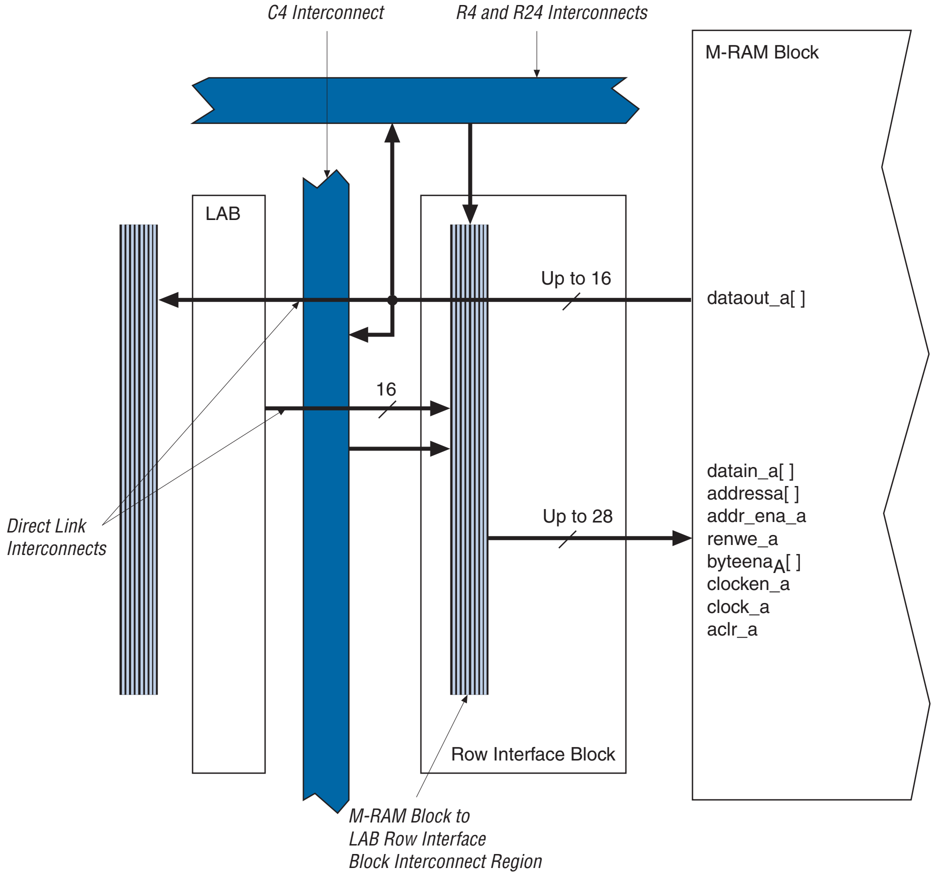


Table 2–4 shows the input and output data signal connections along with the address and control signal input connections to the row unit interfaces (L0 to L5 and R0 to R5).

The Quartus II software enables the PLLs and their features without requiring any external devices. Table 2–9 shows the PLLs available for each Stratix II device and their type.

Table 2–9. Stratix II Device PLL Availability

Device	Fast PLLs								Enhanced PLLs			
	1	2	3	4	7	8	9	10	5	6	11	12
EP2S15	✓	✓	✓	✓					✓	✓		
EP2S30	✓	✓	✓	✓					✓	✓		
EP2S60 *(1)*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S90 *(2)*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S130 *(3)*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S180	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes to Table 2–9:

(1) EP2S60 devices in the 1020-pin package contain 12 PLLs. EP2S60 devices in the 484-pin and 672-pin packages contain fast PLLs 1–4 and enhanced PLLs 5 and 6.

(2) EP2S90 devices in the 1020-pin and 1508-pin packages contain 12 PLLs. EP2S90 devices in the 484-pin and 780-pin packages contain fast PLLS 1–4 and enhanced PLLs 5 and 6.

(3) EP2S130 devices in the 1020-pin and 1508-pin packages contain 12PLLs. The EP2S130 device in the 780-pin package contains fast PLLs 1–4 and enhanced PLLs 5 and 6.

Table 2–10 shows the enhanced PLL and fast PLL features in Stratix II devices.

Table 2–10. Stratix II PLL Features

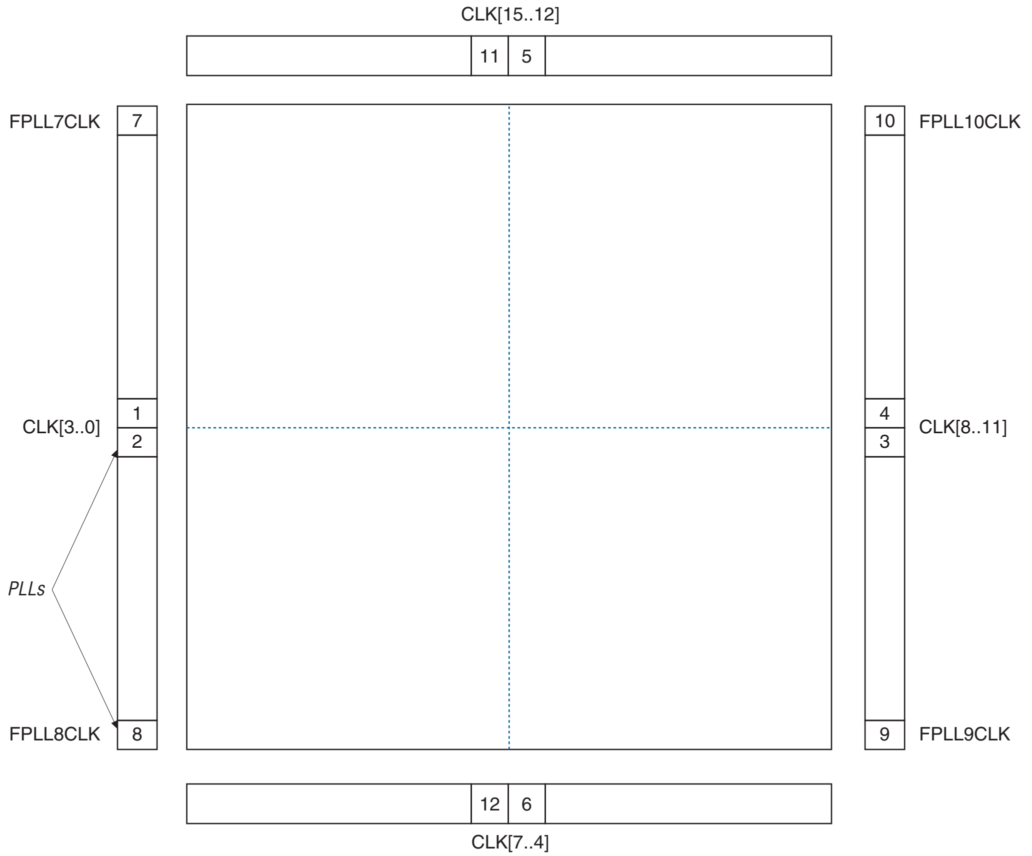
Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	*m*/(*n* × post-scale counter) *(1)*	*m*/(*n* × post-scale counter) *(2)*
Phase shift	Down to 125-ps increments *(3)*, *(4)*	Down to 125-ps increments *(3)*, *(4)*
Clock switchover	✓	✓ *(5)*
PLL reconfiguration	✓	✓
Reconfigurable bandwidth	✓	✓
Spread spectrum clocking	✓	
Programmable duty cycle	✓	✓
Number of internal clock outputs	6	4
Number of external clock outputs	Three differential/six single-ended	*(6)*
Number of feedback clock inputs	One single-ended or differential *(7)*, *(8)*	

Notes to Table 2–10:

(1) For enhanced PLLs, *m* ranges from 1 to 256, while *n* and post-scale counters range from 1 to 512 with 50% duty cycle.
(2) For fast PLLs, *m*, and post-scale counters range from 1 to 32. The *n* counter ranges from 1 to 4.
(3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by 8.
(4) For degree increments, Stratix II devices can shift all output frequencies in increments of at least 45. Smaller degree increments are possible depending on the frequency and divide parameters.
(5) Stratix II fast PLLs only support manual clock switchover.
(6) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate txclkout.
(7) If the feedback input is used, you lose one (or two, if FBIN is differential) external clock output pin.
(8) Every Stratix II device has at least two enhanced PLLs with one single-ended or differential external feedback input per PLL.

Figure 2–40 shows a top-level diagram of the Stratix II device and PLL floorplan.

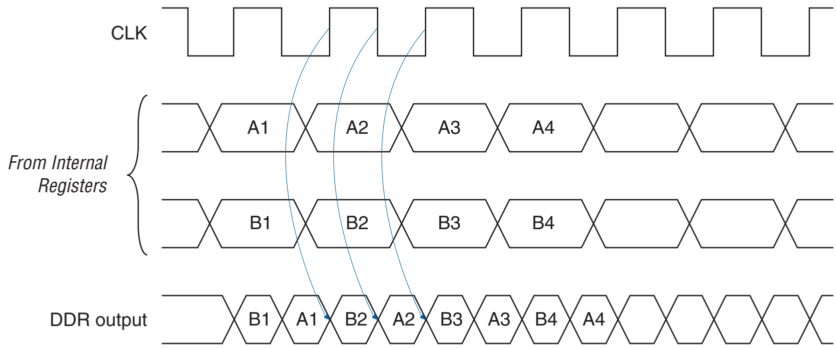
Figure 2–40. PLL Locations



Figures 2–41 and 2–42 shows the global and regional clocking from the fast PLL outputs and the side clock pins.

Figure 2–43 shows the global and regional clocking from enhanced PLL outputs and top and bottom CLK pins. The connections to the global and regional clocks from the top clock pins and enhanced PLL outputs is shown in Table 2–11. The connections to the clocks from the bottom clock pins is shown in Table 2–12.

Figure 2–55. Output TIming Diagram in DDR Mode



The Stratix II IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Stratix II devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces. Stratix II devices support DDR and DDR2 SDRAM, QDR II SRAM, RLDRAM II, and SDR SDRAM memory interfaces. In every Stratix II device, the I/O banks at the top (banks 3 and 4) and bottom (banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36. Table 2–14 shows the number of DQ and DQS buses that are supported per device.

Table 2–14. DQS & DQ Bus Mode Support (Part 1 of 2) Note (1)

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2S15	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
EP2S30	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
EP2S60	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
	1,020-pin FineLine BGA	36	18	8	4

Table 2–17. On-Chip Termination Support by I/O Banks (Part 2 of 2)

On-Chip Termination Support	I/O Standard Support	Top & Bottom Banks	Left & Right Banks
Series termination with calibration	3.3-V LVTTL	✓	
	3.3-V LVCMOS	✓	
	2.5-V LVTTL	✓	
	2.5-V LVCMOS	✓	
	1.8-V LVTTL	✓	
	1.8-V LVCMOS	✓	
	1.5-V LVTTL	✓	
	1.5-V LVCMOS	✓	
	SSTL-2 Class I and II	✓	
	SSTL-18 Class I and II	✓	
	1.8-V HSTL Class I	✓	
	1.8-V HSTL Class II	✓	
	1.5-V HSTL Class I	✓	
	1.2-V HSTL	✓	
Parallel termination with calibration	SSTL-2 Class I and II	✓	
	SSTL-18 Class I and II	✓	
	1.8-V HSTL Class I	✓	
	1.8-V HSTL Class II	✓	
	1.5-V HSTL Class I and II	✓	
	1.2-V HSTL	✓	
Differential termination *(1)*	LVDS		✓
	HyperTransport technology		✓

Note to Table 2–17:

(1) Clock pins `CLK1`, `CLK3`, `CLK9`, `CLK11`, and pins `FPLL[7..10]CLK` do not support differential on-chip termination. Clock pins `CLK0`, `CLK2`, `CLK8`, and `CLK10` do support differential on-chip termination. Clock pins in the top and bottom banks (`CLK[4..7, 12..15]`) do not support differential on-chip termination.

Table 2–18 summarizes Stratix II MultiVolt I/O support.

Table 2–18. Stratix II MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal (V)					Output Signal (V)					
	1.2	1.5	1.8	2.5	3.3	1.2	1.5	1.8	2.5	3.3	5.0
1.2	*(4)*	✓ *(2)*	✓ *(2)*	✓ *(2)*	✓ *(2)*	✓ *(4)*					
1.5	*(4)*	✓	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓				
1.8	*(4)*	✓	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓ *(3)*	✓			
2.5	*(4)*			✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓		
3.3	*(4)*			✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	✓

Notes to Table 2–18:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and select the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.

(2) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable Stratix II V_{IL} maximum and V_{IH} minimum voltage specifications.

(3) Although V_{CCIO} specifies the voltage necessary for the Stratix II device to drive out, a receiving device powered at a different level can still interface with the Stratix II device if it has inputs that tolerate the V_{CCIO} value.

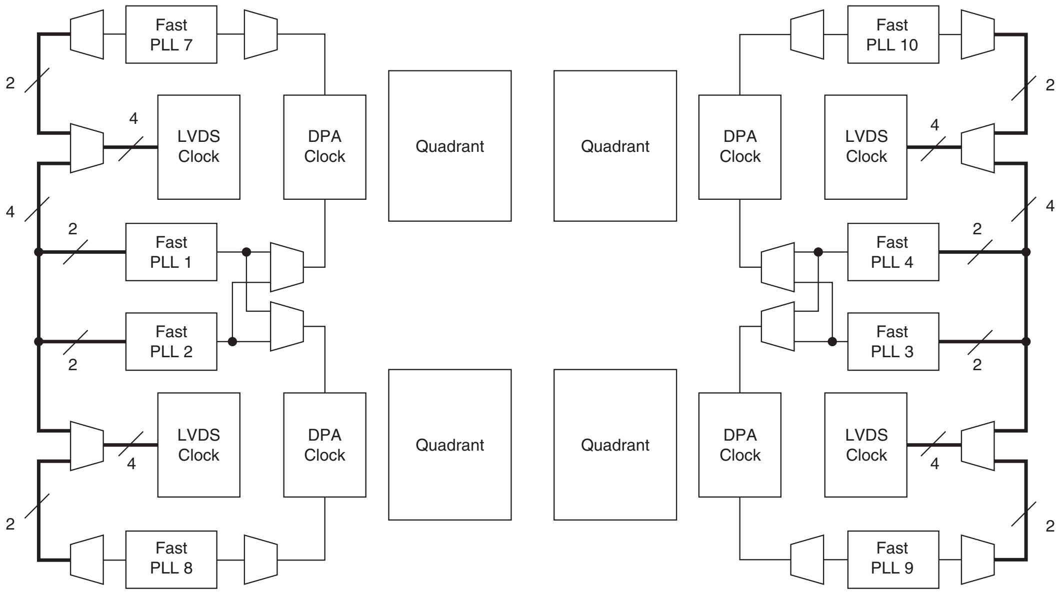
(4) Stratix II devices do not support 1.2-V LVTTL and 1.2-V LVCMOS. Stratix II devices support 1.2-V HSTL.

The `TDO` and `nCEO` pins are powered by V_{CCIO} of the bank that they reside in. `TDO` is in I/O bank 4 and `nCEO` is in I/O bank 7.

Ideally, the V_{CC} supplies for the I/O buffers of any two connected pins are at the same voltage level. This may not always be possible depending on the V_{CCIO} level of `TDO` and `nCEO` pins on master devices and the configuration voltage level chosen by `VCCSEL` on slave devices. Master and slave devices can be in any position in the chain. Master indicates that it is driving out `TDO` or `nCEO` to a slave device.

For multi-device passive configuration schemes, the `nCEO` pin of the master device drives the `nCE` pin of the slave device. The `VCCSEL` pin on the slave device selects which input buffer is used for `nCE`. When `VCCSEL` is logic high, it selects the 1.8-V/1.5-V buffer powered by V_{CCIO}. When `VCCSEL` is logic low it selects the 3.3-V/2.5-V input buffer powered by V_{CCPD}. The ideal case is to have the V_{CCIO} of the `nCEO` bank in a master device match the `VCCSEL` settings for the `nCE` input buffer of the slave device it is connected to, but that may not be possible depending on the application. Table 2–19 contains board design recommendations to ensure that `nCEO` can successfully drive `nCE` for all power supply combinations.

Figure 2–61. Fast PLL & Channel Layout in the EP2S60 to EP2S180 Devices Note (1)



Note to Figure 2–61:

(1) See Tables 2–22 through 2–26 for the number of channels each device supports.

For more information on JTAG, see the following documents:

- The *IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing for Stratix II & Stratix II GX Devices* chapter of the *Stratix II Device Handbook, Volume 2* or the *Stratix II GX Device Handbook, Volume 2*
- Jam Programming & Test Language Specification

SignalTap II Embedded Logic Analyzer

Stratix II devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA® packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Stratix II architecture are configured with CMOS SRAM elements. Altera® FPGA devices are reconfigurable and every device is tested with a high coverage production test program so you do not have to perform fault testing and can instead focus on simulation and design verification.

Stratix II devices are configured at system power-up with data stored in an Altera configuration device or provided by an external controller (e.g., a MAX® II device or microprocessor). Stratix II devices can be configured using the fast passive parallel (FPP), active serial (AS), passive serial (PS), passive parallel asynchronous (PPA), and JTAG configuration schemes. The Stratix II device’s optimized interface allows microprocessors to configure it serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat Stratix II devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy.

In addition to the number of configuration methods supported, Stratix II devices also offer the design security, decompression, and remote system upgrade features. The design security feature, using configuration bitstream encryption and AES technology, provides a mechanism to protect your designs. The decompression feature allows Stratix II FPGAs to receive a compressed configuration bitstream and decompress this data in real-time, reducing storage requirements and configuration time. The remote system upgrade feature allows real-time system upgrades from remote locations of your Stratix II designs. For more information, see “Configuration Schemes” on page 3–7.

Figure 5–1. Receiver Input Waveforms for Differential I/O Standards

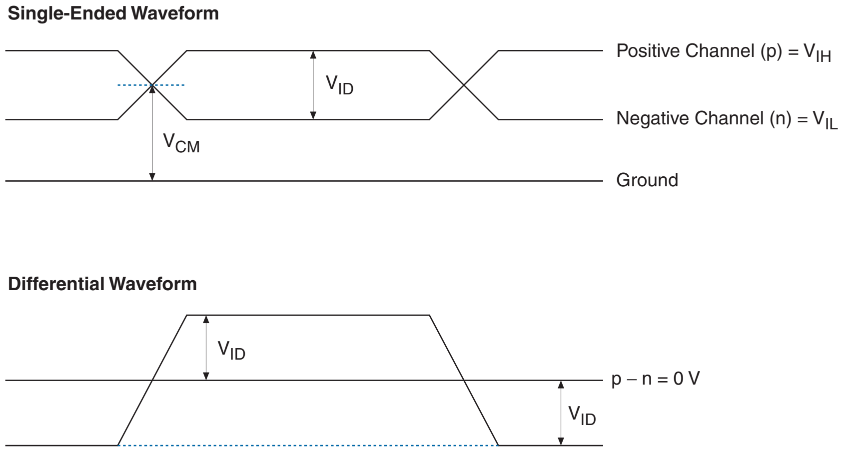


Figure 5–2. Transmitter Output Waveforms for Differential I/O Standards

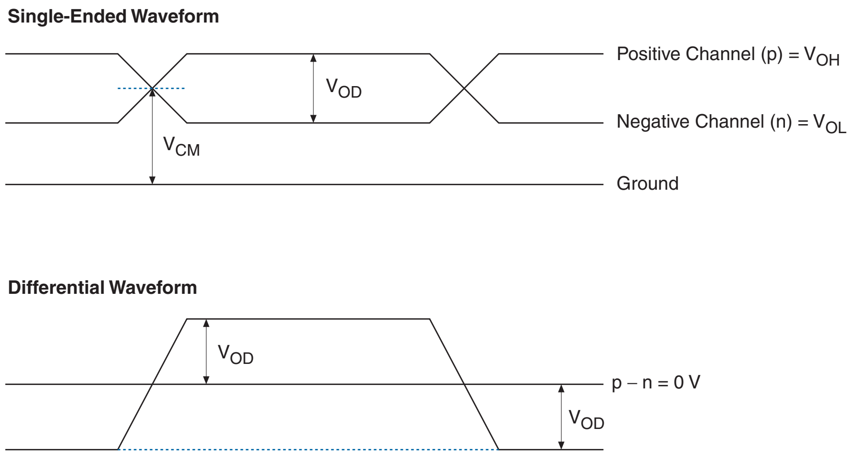


Table 5–10. 2.5-V LVDS I/O Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)		2.375	2.500	2.625	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250		450	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.125		1.375	V
R_L	Receiver differential input discrete resistor (external to Stratix II devices)		90	100	110	Ω

Table 5–11. 3.3-V LVDS I/O Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO} *(1)*	I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12)		3.135	3.300	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250		710	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	840		1,570	mV
R_L	Receiver differential input discrete resistor (external to Stratix II devices)		90	100	110	Ω

Note to Table 5–11:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by `VCC_PLL_OUT`. For differential clock output/feedback operation, `VCC_PLL_OUT` should be connected to 3.3 V.

Table 5–31. Series & Differential On-Chip Termination Specification for Left & Right I/O Banks					
Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25-Ω R_S 3.3/2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	±30	%
50-Ω R_S 3.3/2.5/1.8	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5/1.8 V	±30	±30	%
50-Ω R_S 1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±36	±36	%
R_D	Internal differential termination for LVDS or HyperTransport technology (100-Ω setting)	V_{CCIO} = 2.5 V	±20	±25	%

Pin Capacitance

Table 5–32 shows the Stratix II device family pin capacitance.

Table 5–32. Stratix II Device Capacitance *Note (1)*			
Symbol	Parameter	Typical	Unit
C_{IOTB}	Input capacitance on I/O pins in I/O banks 3, 4, 7, and 8.	5.0	pF
C_{IOLR}	Input capacitance on I/O pins in I/O banks 1, 2, 5, and 6, including high-speed differential receiver and transmitter pins.	6.1	pF
C_{CLKTB}	Input capacitance on top/bottom clock input pins: `CLK[4..7]` and `CLK[12..15]`.	6.0	pF
C_{CLKLR}	Input capacitance on left/right clock inputs: `CLK0`, `CLK2`, `CLK8`, `CLK10`.	6.1	pF
C_{CLKLR+}	Input capacitance on left/right clock inputs: `CLK1`, `CLK3`, `CLK9`, and `CLK11`.	3.3	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins in PLL banks 9, 10, 11, and 12.	6.7	pF

Note to Table 5–32:

(1) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within ±0.5pF

IOE Programmable Delay

See Tables 5–69 and 5–70 for IOE programmable delay.

Table 5–69. Stratix II IOE Programmable Delay on Column Pins Note (1)

Parameter	Paths Affected	Available Settings	Minimum Timing (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade	
			Min Offset (ps)	Max Offset (ps)	Min Offset (ps)	Max Offset (ps)	Min Offset (ps)	Max Offset (ps)	Min Offset (ps)	Max Offset (ps)
Input delay from pin to internal cells	Pad to I/O dataout to logic array	8	0 0	1,696 1,781	0 0	2,881 3,025	0	3,313	0	3,860
Input delay from pin to input register	Pad to I/O input register	64	0 0	1,955 2,053	0 0	3,275 3,439	0	3,766	0	4,388
Delay from output register to output pin	I/O output register to pad	2	0 0	316 332	0 0	500 525	0	575	0	670
Output enable pin delay	t_{XZ}, t_{ZX}	2	0 0	305 320	0 0	483 507	0	556	0	647

Notes to Table 5–69:

(1) The incremental values for the settings are generally linear. For the exact delay associated with each setting, use the latest version of the Quartus II software.

(2) The first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.

(3) The first number applies to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices. The second number applies to -3 speed grade EP2S130 and EP2S180 devices.

Table 5–76. Stratix II I/O Output Delay for Row Pins (Part 3 of 3)									
I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
1.8-V HSTL Class I	4 mA	t_{OP}	972	1019	1610	1689	1850	1956	ps
		t_{DIP}	930	976	1555	1632	1787	1883	ps
	6 mA	t_{OP}	975	1022	1580	1658	1816	1920	ps
		t_{DIP}	933	979	1525	1601	1753	1847	ps
	8 mA	t_{OP}	958	1004	1576	1653	1811	1916	ps
		t_{DIP}	916	961	1521	1596	1748	1843	ps
	10 mA	t_{OP}	962	1008	1567	1644	1801	1905	ps
		t_{DIP}	920	965	1512	1587	1738	1832	ps
	12 mA (1)	t_{OP}	953	999	1566	1643	1800	1904	ps
		t_{DIP}	911	956	1511	1586	1737	1831	ps
1.5-V HSTL Class I	4 mA	t_{OP}	970	1018	1591	1669	1828	1933	ps
		t_{DIP}	928	975	1536	1612	1765	1860	ps
	6 mA	t_{OP}	974	1021	1579	1657	1815	1919	ps
		t_{DIP}	932	978	1524	1600	1752	1846	ps
	8 mA (1)	t_{OP}	960	1006	1572	1649	1807	1911	ps
		t_{DIP}	918	963	1517	1592	1744	1838	ps
LVDS		t_{OP}	1018	1067	1723	1808	1980	2089	ps
		t_{DIP}	976	1024	1668	1751	1917	2016	ps
HyperTransport		t_{OP}	1005	1053	1723	1808	1980	2089	ps
		t_{DIP}	963	1010	1668	1751	1917	2016	ps

Notes to Table 5–76:
(1) This is the default setting in the Quartus II software.
(2) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(3) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

Maximum Input & Output Clock Toggle Rate

Maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 2 of 5) Note (1)										
I/O Standard	**Drive Strength**	**Column I/O Pins (MHz)**			**Row I/O Pins (MHz)**			**Clock Outputs (MHz)**		
		-3	**-4**	**-5**	**-3**	**-4**	**-5**	**-3**	**-4**	**-5**
SSTL-18 Class I	4 mA	200	150	150	200	150	150	200	150	150
	6 mA	350	250	200	350	250	200	350	250	200
	8 mA	450	300	300	450	300	300	450	300	300
	10 mA	500	400	400	500	400	400	500	400	400
	12 mA	700	550	400	-	-	-	650	550	400
SSTL-18 Class II	8 mA	200	200	150	-	-	-	200	200	150
	16 mA	400	350	350	-	-	-	400	350	350
	18 mA	450	400	400	-	-	-	450	400	400
	20 mA	550	500	450	-	-	-	550	500	450
1.8-V HSTL Class I	4 mA	300	300	300	300	300	300	300	300	300
	6 mA	500	450	450	500	450	450	500	450	450
	8 mA	650	600	600	650	600	600	650	600	600
	10 mA	700	650	600	700	650	600	700	650	600
	12 mA	700	700	650	700	700	650	700	700	650
1.8-V HSTL Class II	16 mA	500	500	450	-	-	-	500	500	450
	18 mA	550	500	500	-	-	-	550	500	500
	20 mA	650	550	550	-	-	-	550	550	550
1.5-V HSTL Class I	4 mA	350	300	300	350	300	300	350	300	300
	6 mA	500	500	450	500	500	450	500	500	450
	8 mA	700	650	600	700	650	600	700	650	600
	10 mA	700	700	650	-	-	-	700	700	650
	12 mA	700	700	700	-	-	-	700	700	700
1.5-V HSTL Class II	16 mA	600	600	550	-	-	-	600	600	550
	18 mA	650	600	600	-	-	-	650	600	600
	20 mA	700	650	600	-	-	-	700	650	600
Differential SSTL-2 Class I *(3)*	8 mA	400	300	300	400	300	300	400	300	300
	12 mA	400	400	350	400	400	350	400	400	350
Differential SSTL-2 Class II *(3)*	16 mA	350	350	300	350	350	300	350	350	300
	20 mA	400	350	350	350	350	297	400	350	350
	24 mA	400	400	350	-	-	-	400	400	350