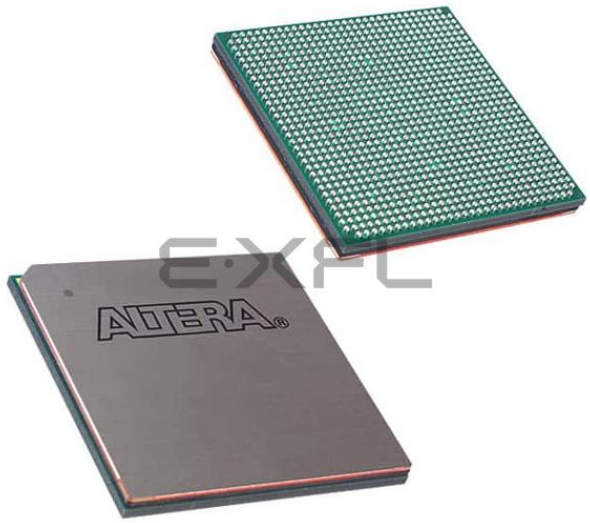

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	718
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s60f1020c4

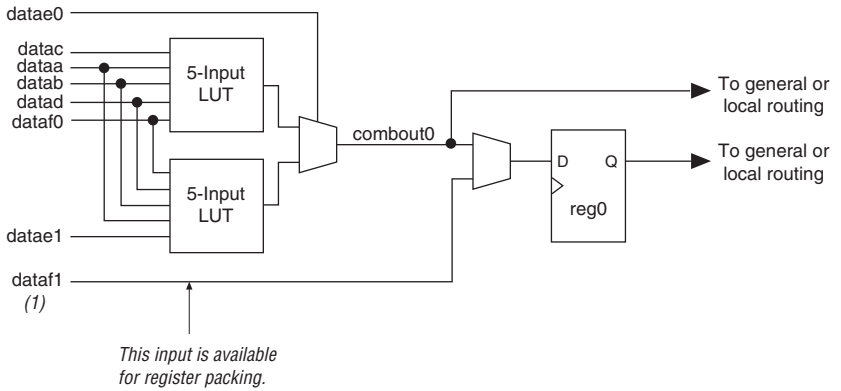
Document Revision History

Table 1–6 shows the revision history for this chapter.

Table 1–6. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007, v4.2	Moved Document Revision History to the end of the chapter.	—
April 2006, v4.1	• Updated "Features" section. • Removed Note 4 from Table 1–2. • Updated Table 1–4.	—
December 2005, v4.0	• Updated Tables 1–2, 1–4, and 1–5. • Updated Figure 2–43.	—
July 2005, v3.1	• Added vertical migration information, including Table 1–4. • Updated Table 1–5.	—
May 2005, v3.0	• Updated "Features" section. • Updated Table 1–2.	—
March 2005, v2.1	Updated "Introduction" and "Features" sections.	—
January 2005, v2.0	Added note to Table 1–2.	—
October 2004, v1.2	Updated Tables 1–2, 1–3, and 1–5.	—
July 2004, v1.1	• Updated Tables 1–1 and 1–2. • Updated "Features" section.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

Figure 2–10. Template for Supported Seven-Input Functions in Extended LUT Mode



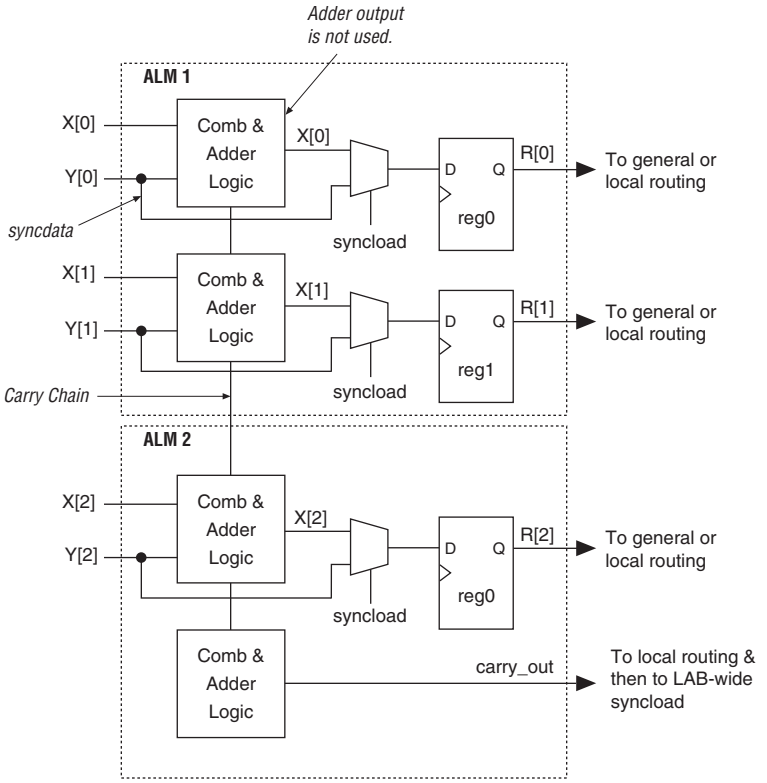
Note to Figure 2–10:

(1) If the seven-input function is unregistered, the unused eighth input is available for register packing. The second register, `reg1`, is not available.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An ALM in arithmetic mode uses two sets of two four-input LUTs along with two dedicated full adders. The dedicated adders allow the LUTs to be available to perform pre-adder logic; therefore, each adder can add the output of two four-input functions. The four LUTs share the `dataa` and `datab` inputs. As shown in Figure 2–11, the carry-in signal feeds to `adder0`, and the carry-out from `adder0` feeds to carry-in of `adder1`. The carry-out from `adder1` drives to `adder0` of the next ALM in the LAB. ALMs in arithmetic mode can drive out registered and/or unregistered versions of the adder outputs.

Figure 2–12. Conditional Operation Example

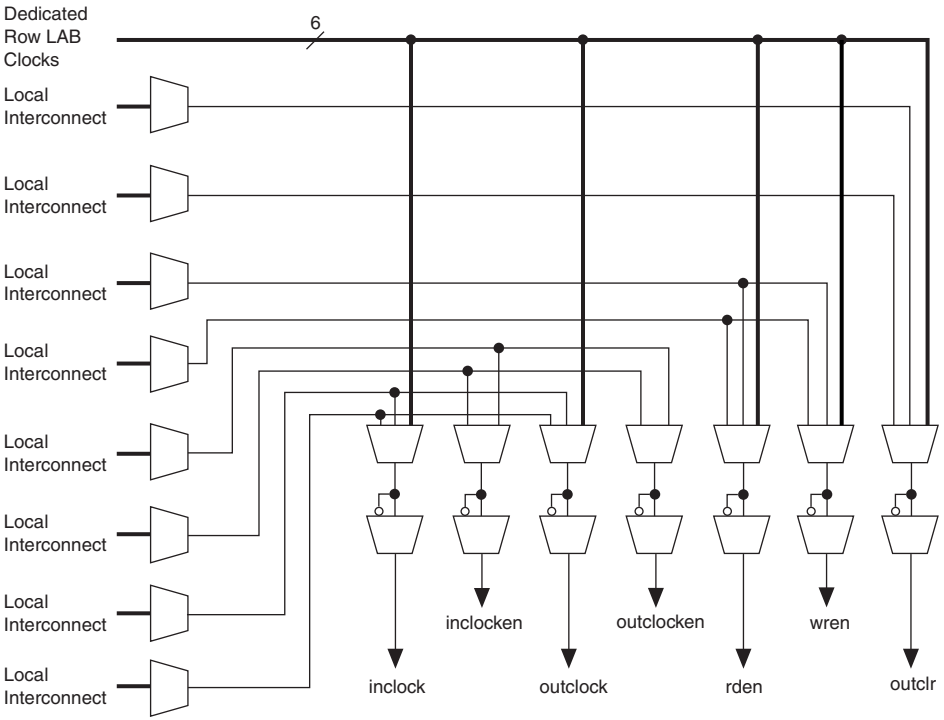


The arithmetic mode also offers clock enable, counter enable, synchronous up/down control, add/subtract control, synchronous clear, synchronous load. The LAB local interconnect data inputs generate the clock enable, counter enable, synchronous up/down and add/subtract control signals. These control signals are good candidates for the inputs that are shared between the four LUTs in the ALM. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Carry Chain

The carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. Carry chains can begin in either the first ALM or the fifth ALM in an LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

Figure 2–19. M512 RAM Block Control Signals



PLLs & Clock Networks

Stratix II devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global & Hierarchical Clocking

Stratix II devices provide 16 dedicated global clock networks and 32 regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to 24 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains in Stratix II devices.

There are 16 dedicated clock pins (CLK[15..0]) to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in Figures 2–31 and 2–32. Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block, which controls the selection of the clock source and dynamically enables/disables the clock to reduce power consumption. Table 2–8 shows global and regional clock features.

Table 2–8. Global & Regional Clock Features

Feature	Global Clocks	Regional Clocks
Number per device	16	32
Number available per quadrant	16	8
Sources	CLK pins, PLL outputs, or internal logic	CLK pins, PLL outputs, or internal logic
Dynamic clock source selection	✓ (1)	
Dynamic enable/disable	✓	✓

Note to Table 2–8:
(1) Dynamic source clock selection is supported for selecting between CLKp pins and PLL outputs only.

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources in the device-IOEs, ALMs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The

The Stratix II clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all the logic fed by the clock net is in an off-state thereby reducing the overall power consumption of the device.

The global and regional clock networks can be powered down statically through a setting in the configuration (**.sof** or **.pof**) file. Clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software.

The dynamic clock enable/disable feature allows the internal logic to control power up/down synchronously on GCLK and RCLK nets and PLL_OUT pins. This function is independent of the PLL and is applied directly on the clock network or PLL_OUT pin, as shown in Figures 2–37 through 2–39.

The following restrictions for the input clock pins apply:

- CLK0 pin -> inclk[0] of CLKCTRL
- CLK1 pin -> inclk[1] of CLKCTRL
- CLK2 pin -> inclk[0] of CLKCTRL
- CLK3 pin -> inclk[1] of CLKCTRL

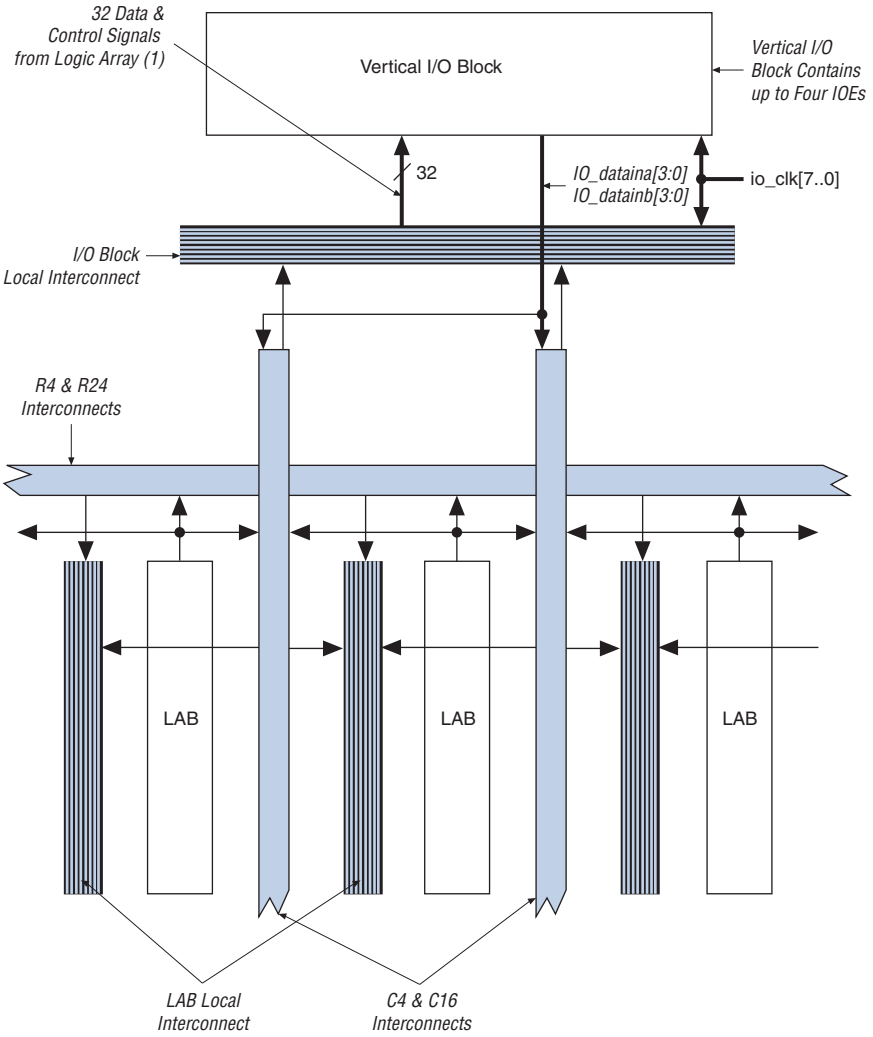
In general, even CLK numbers connect to the inclk[0] port of CLKCTRL, and odd CLK numbers connect to the inclk[1] port of CLKCTRL.

Failure to comply with these restrictions will result in a no-fit error.

Enhanced & Fast PLLs

Stratix II devices provide robust clock management and synthesis using up to four enhanced PLLs and eight fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock-frequency synthesis. With features such as clock switchover, spread-spectrum clocking, reconfigurable bandwidth, phase control, and reconfigurable phase shifting, the Stratix II device's enhanced PLLs provide you with complete control of clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix II high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

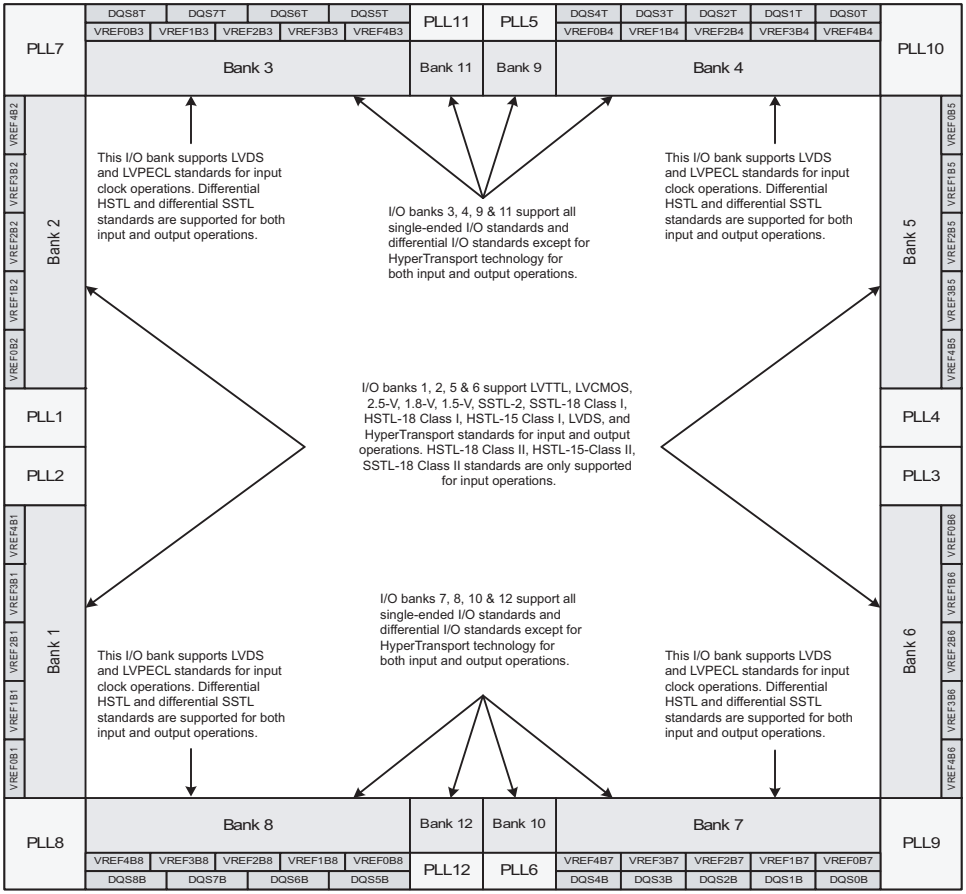
Figure 2–48. Column I/O Block Connection to the Interconnect *Note (1)*



Note to Figure 2–48:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

Figure 2–57. Stratix II I/O Banks *Notes (1), (2), (3), (4)*



Notes to Figure 2–57:

(1) Figure 2–57 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

(2) Depending on the size of the device, different device members have different numbers of V_{REF} groups. Refer to the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks. These PLL banks utilize the adjacent V_{REF} group when voltage-referenced standards are implemented. For example, if an SSTL input is implemented in PLL bank 10, the voltage level at VREFB7 is the reference voltage level for the SSTL input.

(4) Horizontal I/O banks feature SERDES and DPA circuitry for high speed differential I/O standards. See the *High Speed Differential I/O Interfaces in Stratix II & Stratix II GX Devices* chapter of the *Stratix II Device Handbook, Volume 2* or the *Stratix II GX Device Handbook, Volume 2* for more information on differential I/O standards.

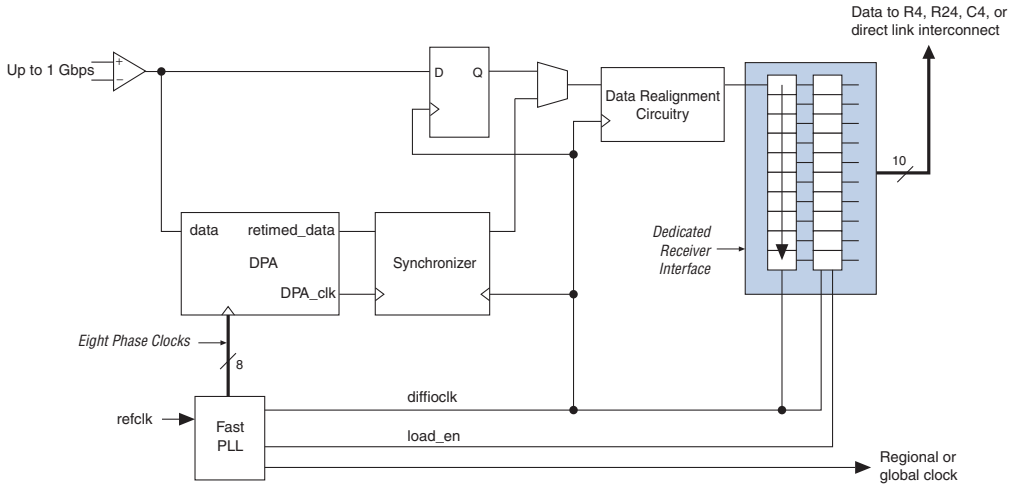
Table 2–23. EP2S60 Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs				Corner Fast PLLs *(4)*			
			PLL 1	PLL 2	PLL 3	PLL 4	PLL 7	PLL 8	PLL 9	PLL 10
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10	10	9	9	10
		(3)	19	19	19	19	-	-	-	-
	Receiver	42 *(2)*	11	10	10	11	11	10	10	11
		(3)	21	21	21	21	-	-	-	-
672-pin FineLine BGA	Transmitter	58 *(2)*	16	13	13	16	16	13	13	16
		(3)	29	29	29	29	-	-	-	-
	Receiver	62 *(2)*	17	14	14	17	17	14	14	17
		(3)	31	31	31	31	-	-	-	-
1,020-pin FineLine BGA	Transmitter	84 *(2)*	21	21	21	21	21	21	21	21
		(3)	42	42	42	42	-	-	-	-
	Receiver	84 *(2)*	21	21	21	21	21	21	21	21
		(3)	42	42	42	42	-	-	-	-

Table 2–24. EP2S90 Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs				Corner Fast PLLs *(4)*			
			PLL 1	PLL 2	PLL 3	PLL 4	PLL 7	PLL 8	PLL 9	PLL 10
484-pin Hybrid FineLine BGA	Transmitter	38 *(2)*	10	9	9	10	-	-	-	-
		(3)	19	19	19	19	-	-	-	-
	Receiver	42 *(2)*	11	10	10	11	-	-	-	-
		(3)	21	21	21	21	-	-	-	-
780-pin FineLine BGA	Transmitter	64 *(2)*	16	16	16	16	-	-	-	
		(3)	32	32	32	32	-	-	-	-
	Receiver	68 *(2)*	17	17	17	17	-	-	-	-
		(3)	34	34	34	34	-	-	-	
1,020-pin FineLine BGA	Transmitter	90 *(2)*	23	22	22	23	23	22	22	23
		(3)	45	45	45	45	-	-	-	-
	Receiver	94 *(2)*	23	24	24	23	23	24	24	23
		(3)	46	46	46	46	-	-	-	-
1,508-pin FineLine BGA	Transmitter	118 *(2)*	30	29	29	30	30	29	29	30
		(3)	59	59	59	59	-	-	-	-
	Receiver	118 *(2)*	30	29	29	30	30	29	29	30
		(3)	59	59	59	59	-	-	-	-

Figure 2–59. Stratix II Receiver Channel



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the VCO can feed to the DPA circuitry.

For more information on the fast PLL, see the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of the channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Since every channel utilizing the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

you need to support configuration input voltages of 1.8 V/1.5 V, you should set the VCCSEL to a logic high and the V_{CCIO} of the bank that contains the configuration inputs to 1.8 V/1.5 V.

For more information on multi-volt support, including information on using TDO and nCEO in multi-volt systems, refer to the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Configuration Schemes

You can load the configuration data for a Stratix II device with one of five configuration schemes (see Table 3–5), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix II device. A configuration device can automatically configure a Stratix II device at system power-up.

You can configure multiple Stratix II devices in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Stratix II FPGAs offer the following:

- Configuration data decompression to reduce configuration file storage
- Design security using configuration data encryption to protect your designs
- Remote system upgrades for remotely updating your Stratix II designs

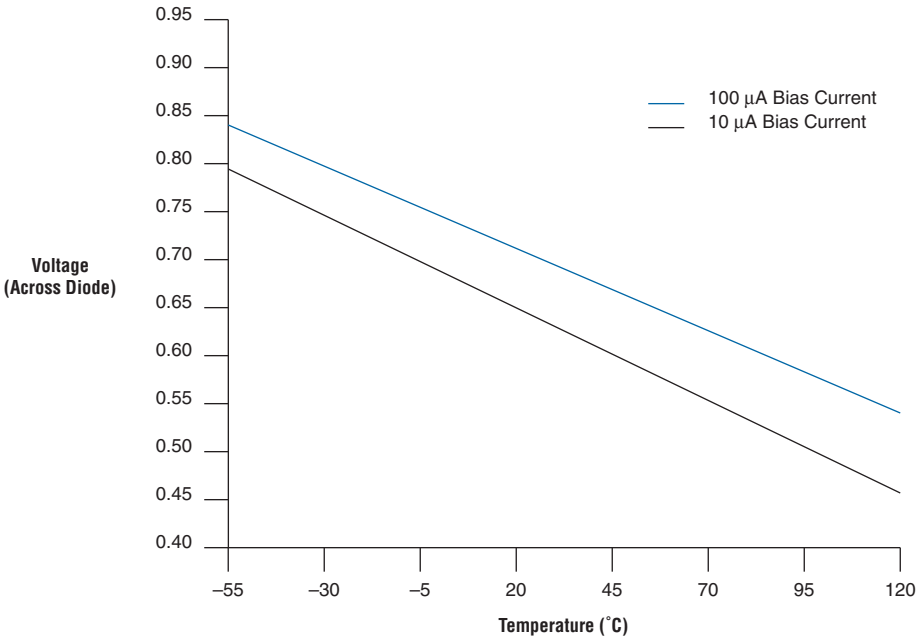
Table 3–5 summarizes which configuration features can be used in each configuration scheme.

Table 3–5. Stratix II Configuration Features (Part 1 of 2)

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
FPP	MAX II device or microprocessor and flash device	✓ *(1)*	✓ *(1)*	✓
	Enhanced configuration device		✓ *(2)*	✓
AS	Serial configuration device	✓	✓	✓ *(3)*
PS	MAX II device or microprocessor and flash device	✓	✓	✓
	Enhanced configuration device	✓	✓	✓
	Download cable *(4)*	✓	✓	

The temperature-sensing diode works for the entire operating range, as shown in Figure 3–2.

Figure 3–2. Temperature vs. Temperature-Sensing Diode Voltage



The temperature sensing diode is a very sensitive circuit which can be influenced by noise coupled from other traces on the board, and possibly within the device package itself, depending on device usage. The interfacing device registers temperature based on milivolts of difference as seen at the TSD. Switching I/O near the TSD pins can affect the temperature reading. Altera recommends you take temperature readings during periods of no activity in the device (for example, standby mode where no clocks are toggling in the device), such as when the nearby I/Os are at a DC state, and disable clock networks in the device.

Automated Single Event Upset (SEU) Detection

Stratix II devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. Some applications that require the device to operate error free at high elevations or in close proximity to Earth's North or South Pole require periodic checks to ensure continued data integrity. The error detection cyclic redundancy check (CRC) feature controlled by

Table 5–2. Maximum Duty Cycles in Voltage Transitions				
Symbol	**Parameter**	**Condition**	**Maximum Duty Cycles**	**Unit**
V_I	Maximum duty cycles in voltage transitions	V_I = 4.0 V	100	%
		V_I = 4.1 V	90	%
		V_I = 4.2 V	50	%
		V_I = 4.3 V	30	%
		V_I = 4.4 V	17	%
		V_I = 4.5 V	10	%

Recommended Operating Conditions

Table 5–3 contains the Stratix II device family recommended operating conditions.

Table 5–3. Stratix II Device Recommended Operating Conditions (Part 1 of 2) Note (1)					
Symbol	**Parameter**	**Conditions**	**Minimum**	**Maximum**	**Unit**
V_{CCINT}	Supply voltage for internal logic	100 µs ≤ risetime ≤ 100 ms *(3)*	1.15	1.25	V
V_{CCIO}	Supply voltage for input and output buffers, 3.3-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*, *(6)*	3.135 (3.00)	3.465 (3.60)	V
	Supply voltage for input and output buffers, 2.5-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*	2.375	2.625	V
	Supply voltage for input and output buffers, 1.8-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*	1.425	1.575	V
	Supply voltage for input and output buffers, 1.2-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*	1.14	1.26	V
V_{CCPD}	Supply voltage for pre-drivers as well as configuration and JTAG I/O buffers.	100 µs ≤ risetime ≤ 100 ms *(4)*	3.135	3.465	V
V_{CCA}	Analog power supply for PLLs	100 µs ≤ risetime ≤ 100 ms *(3)*	1.15	1.25	V
V_{CCD}	Digital power supply for PLLs	100 µs ≤ risetime ≤ 100 ms *(3)*	1.15	1.25	V
V_I	Input voltage (see Table 5–2)	*(2)*, *(5)*	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V

Table 5–14. 3.3-V PCI Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low-level input voltage		–0.3		$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–15. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.30		$0.35 \times V_{CCIO}$	V
V_{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–16. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Reference voltage		0.855	0.900	0.945	V
V_{TT}	Termination voltage		$V_{REF} – 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{IH} (DC)	High-level DC input voltage		$V_{REF} + 0.125$			V
V_{IL} (DC)	Low-level DC input voltage				$V_{REF} – 0.125$	V
V_{IH} (AC)	High-level AC input voltage		$V_{REF} + 0.25$			V
V_{IL} (AC)	Low-level AC input voltage				$V_{REF} – 0.25$	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	$V_{TT} + 0.475$			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*			$V_{TT} – 0.475$	V

Note to Table 5–16:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–30. Series On-Chip Termination Specification for Top & Bottom I/O Banks (Part 2 of 2)
Notes (1), 2

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
50-Ω R_S 3.3/2.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	±30	%
50-Ω R_T 2.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
25-Ω R_S 1.8	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_S 1.8	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_T 1.8	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±10	±15	%
50–Ω R_S 1.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±36	±36	%
50-Ω R_T 1.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±10	±15	%
50–Ω R_S 1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±50	±50	%
50-Ω R_T 1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±10	±15	%

Notes for Table 5–30:
(1) The resistance tolerances for calibrated SOCT and POCT are for the moment of calibration. If the temperature or voltage changes over time, the tolerance may also change.
(2) On-chip parallel termination with calibration is only supported for input pins.

Table 5–31. Series & Differential On-Chip Termination Specification for Left & Right I/O Banks

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25-Ω R_S 3.3/2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	±30	%
50-Ω R_S 3.3/2.5/1.8	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5/1.8 V	±30	±30	%
50-Ω R_S 1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±36	±36	%
R_D	Internal differential termination for LVDS or HyperTransport technology (100-Ω setting)	V_{CCIO} = 2.5 V	±20	±25	%

Pin Capacitance

Table 5–32 shows the Stratix II device family pin capacitance.

Table 5–32. Stratix II Device Capacitance *Note (1)*

Symbol	Parameter	Typical	Unit
C_{IOTB}	Input capacitance on I/O pins in I/O banks 3, 4, 7, and 8.	5.0	pF
C_{IOLR}	Input capacitance on I/O pins in I/O banks 1, 2, 5, and 6, including high-speed differential receiver and transmitter pins.	6.1	pF
C_{CLKTB}	Input capacitance on top/bottom clock input pins: `CLK[4..7]` and `CLK[12..15]`.	6.0	pF
C_{CLKLR}	Input capacitance on left/right clock inputs: `CLK0`, `CLK2`, `CLK8`, `CLK10`.	6.1	pF
C_{CLKLR+}	Input capacitance on left/right clock inputs: `CLK1`, `CLK3`, `CLK9`, and `CLK11`.	3.3	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins in PLL banks 9, 10, 11, and 12.	6.7	pF

Note to Table 5–32:

(1) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within ±0.5pF

The performance numbers in Table 5–36 are extracted from the Quartus II software version 5.1 SP1.

Table 5–36. Stratix II Performance Notes (Part 1 of 6) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
LE	16-to-1 multiplexer *(4)*	21	0	0	654.87	625.0	523.83	460.4	MHz
	32-to-1 multiplexer *(4)*	38	0	0	519.21	473.26	464.25	384.17	MHz
	16-bit counter	16	0	0	566.57	538.79	489.23	421.05	MHz
	64-bit counter	64	0	0	244.31	232.07	209.11	181.38	MHz
TriMatrix Memory M512 block	Simple dual-port RAM 32 × 18 bit	0	1	0	500.00	476.19	434.02	373.13	MHz
	FIFO 32 x 18 bit	22	1	0	500.00	476.19	434.78	373.13	MHz
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36 bit *(8)*	0	1	0	540.54	515.46	469.48	401.60	MHz
	True dual-port RAM 128 × 18 bit *(8)*	0	1	0	540.54	515.46	469.48	401.60	MHz
	FIFO 128 × 36 bit	22	1	0	530.22	499.00	469.48	401.60	MHz
	Simple dual-port RAM 128 × 36 bit *(9)*	0	1	0	475.28	453.30	413.22	354.10	MHz
	True dual-port RAM 128 × 18 bit *(9)*	0	1	0	475.28	453.30	413.22	354.10	MHz

Table 5–50. EP2S30 Row Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.304	1.184	1.966	2.251	2.616	ns
t_{COUT}	1.309	1.189	1.962	2.247	2.611	ns
t_{PLLCIN}	-0.135	–0.158	–0.208	–0.254	–0.302	ns
$t_{PLLCOUT}$	-0.13	–0.153	–0.212	–0.258	–0.307	ns

Table 5–51. EP2S30 Row Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.289	1.352	2.238	2.567	2.990	ns
t_{COUT}	1.294	1.357	2.234	2.563	2.985	ns
t_{PLLCIN}	-0.14	-0.154	-0.169	-0.205	-0.254	ns
$t_{PLLCOUT}$	-0.135	-0.149	-0.173	-0.209	-0.259	ns

EP2S60 Clock Timing Parameters

Tables 5–52 through 5–55 show the maximum clock timing parameters for EP2S60 devices.

Table 5–52. EP2S60 Column Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.681	1.762	2.945	3.381	3.931	ns
t_{COUT}	1.524	1.597	2.703	3.103	3.607	ns
t_{PLLCIN}	0.066	0.064	0.279	0.311	0.348	ns
$t_{PLLCOUT}$	-0.091	-0.101	0.037	0.033	0.024	ns

Table 5–80. Maximum DCD for Non-DDIO Output on Row I/O Pins (Part 2 of 2) *Note (1)*

Row I/O Output Standard	Maximum DCD for Non-DDIO Output		
	-3 Devices	-4 & -5 Devices	Unit
1.8 V	180	180	ps
1.5-V LVCMOS	165	195	ps
SSTL-2 Class I	115	145	ps
SSTL-2 Class II	95	125	ps
SSTL-18 Class I	55	85	ps
1.8-V HSTL Class I	80	100	ps
1.5-V HSTL Class I	85	115	ps
LVDS/ HyperTransport technology	55	80	ps

Note to Table 5–80:
(1) The DCD specification is based on a no logic array noise condition.

Here is an example for calculating the DCD as a percentage for a non-DDIO output on a row I/O on a -3 device:

If the non-DDIO output I/O standard is SSTL-2 Class II, the maximum DCD is 95 ps (see Table 5–80). If the clock frequency is 267 MHz, the clock period T is:

T = 1/ f = 1 / 267 MHz = 3.745 ns = 3745 ps

To calculate the DCD as a percentage:

(T/2 – DCD) / T = (3745ps/2 – 95ps) / 3745ps = 47.5% (for low boundary)

(T/2 + DCD) / T = (3745ps/2 + 95ps) / 3745ps = 52.5% (for high boundary)