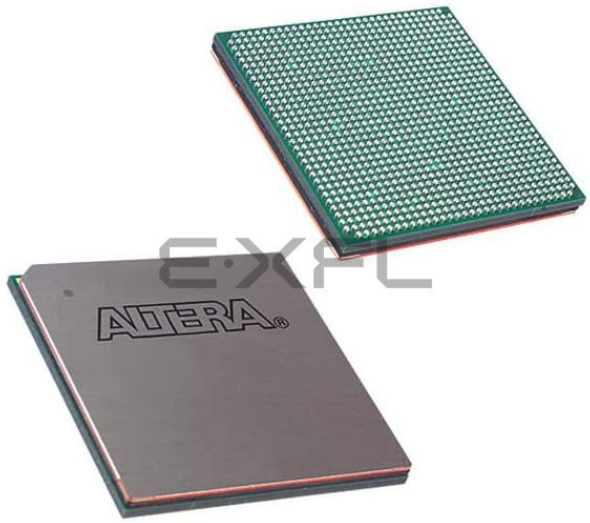

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	718
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s60f1020c5n

Chapter 3. Configuration & Testing

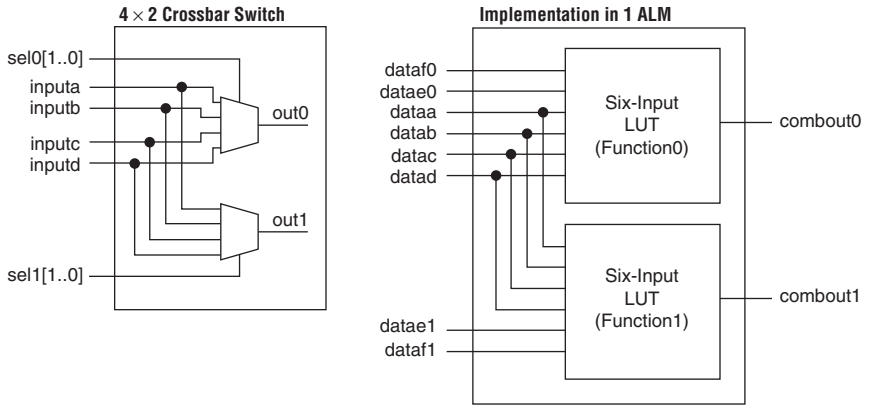
Chapter 4. Hot Socketing & Power-On Reset

Chapter 5. DC & Switching Characteristics

For the packing of two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are dataa and datab. The combination of a four-input function with a five-input function requires one common input (either dataa or datab).

In the case of implementing two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–8. The shared inputs are dataa, datab, datac, and datad, while the unique select lines are datae0 and dataf0 for function0, and datae1 and dataf1 for function1. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

Figure 2–8. 4 × 2 Crossbar Switch Example



In a sparsely used device, functions that could be placed into one ALM may be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically utilizes the full potential of the Stratix II ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments.

Any six-input function can be implemented utilizing inputs dataa, datab, datac, datad, and either datae0 and dataf0 or datae1 and dataf1. If datae0 and dataf0 are utilized, the output is driven to register0, and/or register0 is bypassed and the data drives out to the interconnect using the top set of output drivers (see Figure 2–9). If

The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column.

To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only utilize either the top half or the bottom half of the LAB before connecting to the next LAB. This leaves the other half of the ALMs in the LAB available for implementing narrower fan-in functions in normal mode. Carry chains that use the top four ALMs in the first LAB carry into the top half of the ALMs in the next LAB within the column. Carry chains that use the bottom four ALMs in the first LAB carry into the bottom half of the ALMs in the next LAB within the column. Every other column of LABs is top-half bypassable, while the other LAB columns are bottom-half bypassable.

See the "MultiTrack Interconnect" on page 2–22 section for more information on carry chain interconnect.

Shared Arithmetic Mode

In shared arithmetic mode, the ALM can implement a three-input add. In this mode, the ALM is configured with four 4-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder (either to `adder1` in the same ALM or to `adder0` of the next ALM in the LAB) via a dedicated connection called the shared arithmetic chain. This shared arithmetic chain can significantly improve the performance of an adder tree by reducing the number of summation stages required to implement an adder tree. Figure 2–13 shows the ALM in shared arithmetic mode.

Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Table 2–6 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, and 2D FIR filters, equalizers, IIR, correlators, matrix multiplication and many other functions. The DSP blocks also support mixed modes and mixed multiplier sizes in the same block. For example, half of one DSP block can implement one 18 × 18-bit multiplier in multiply-accumulator mode, while the other half of the DSP block implements four 9 × 9-bit multipliers in simple multiplier mode.

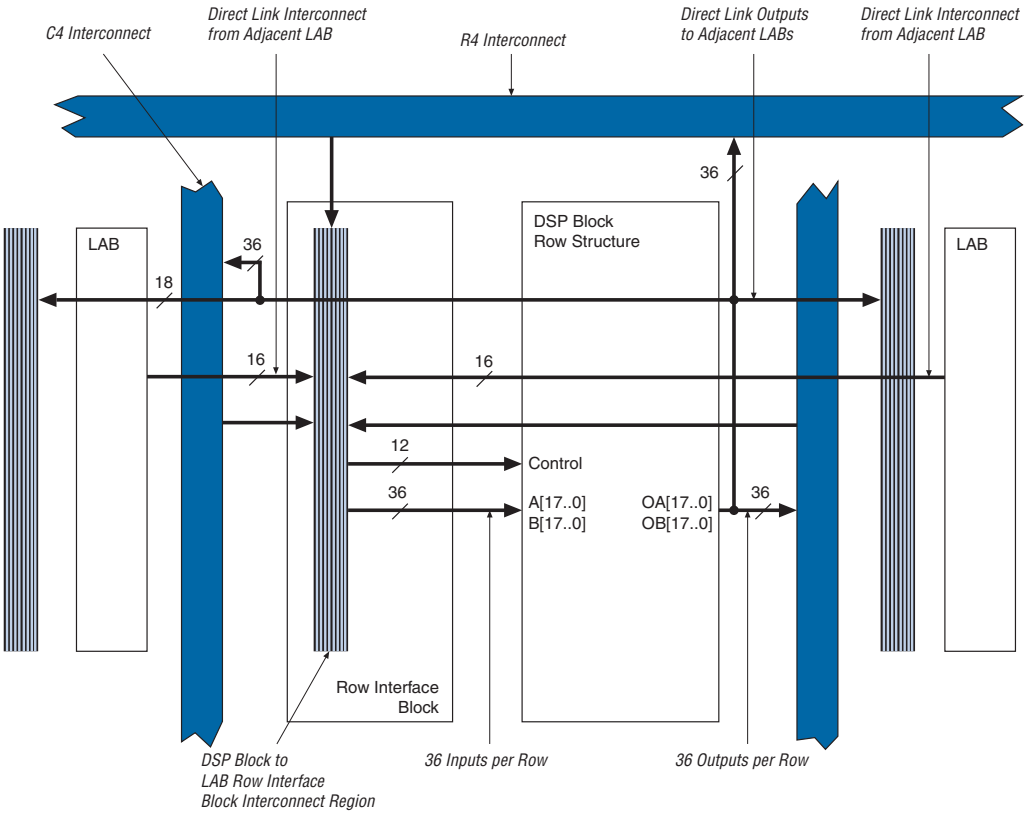
Table 2–6. Multiplier Size & Configurations per DSP Block

DSP Block Mode	9 × 9	18 × 18	36 × 36
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	-	Two 52-bit multiply-accumulate blocks	-
Two-multipliers adder	Four two-multiplier adder (two 9 × 9 complex multiply)	Two two-multiplier adder (one 18 × 18 complex multiply)	-
Four-multipliers adder	Two four-multiplier adder	One four-multiplier adder	-

DSP Block Interface

Stratix II device DSP block input registers can generate a shift register that can cascade down in the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade registers within multiple DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in ALMs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in ALMs. Each DSP block can route the shift register chain out of the block to cascade multiple columns of DSP blocks.

Figure 2–30. DSP Block Interface to Interconnect



A bus of 44 control signals feeds the entire DSP block. These signals include clocks, asynchronous clears, clock enables, signed/unsigned control signals, addition and subtraction control signals, rounding and saturation control signals, and accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface.

PLLs & Clock Networks

Stratix II devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global & Hierarchical Clocking

Stratix II devices provide 16 dedicated global clock networks and 32 regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to 24 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains in Stratix II devices.

There are 16 dedicated clock pins (CLK[15..0]) to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in Figures 2–31 and 2–32. Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block, which controls the selection of the clock source and dynamically enables/disables the clock to reduce power consumption. Table 2–8 shows global and regional clock features.

Table 2–8. Global & Regional Clock Features

Feature	Global Clocks	Regional Clocks
Number per device	16	32
Number available per quadrant	16	8
Sources	CLK pins, PLL outputs, or internal logic	CLK pins, PLL outputs, or internal logic
Dynamic clock source selection	✓ (1)	
Dynamic enable/disable	✓	✓

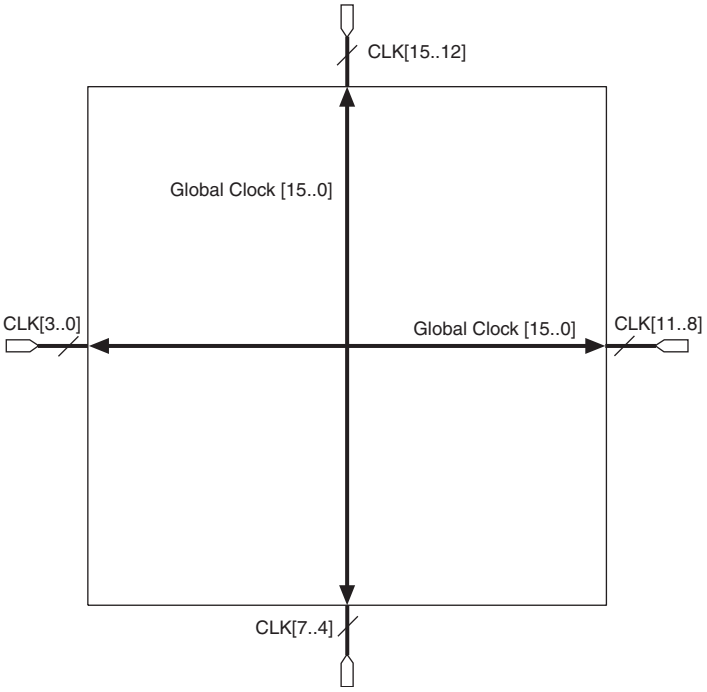
Note to Table 2–8:
(1) Dynamic source clock selection is supported for selecting between CLKp pins and PLL outputs only.

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources in the device-IOEs, ALMs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The

global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–31 shows the 16 dedicated CLK pins driving global clock networks.

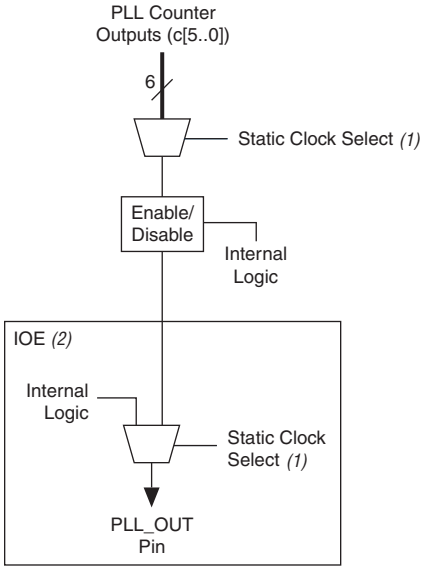
Figure 2–31. Global Clocking



Regional Clock Network

There are eight regional clock networks RCLK[7..0] in each quadrant of the Stratix II device that are driven by the dedicated CLK[15..0] input pins, by PLL outputs, or by internal logic. The regional clock networks provide the lowest clock delay and skew for logic contained in a single quadrant. The CLK clock pins symmetrically drive the RCLK networks in a particular quadrant, as shown in Figure 2–32.

Figure 2–39. External PLL Output Clock Control Blocks



Notes to Figure 2–39:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) The clock control block feeds to a multiplexer within the PLL_OUT pin's IOE. The PLL_OUT pin is a dual-purpose pin. Therefore, this multiplexer selects either an internal signal or the output of the clock control block.

For the global clock control block, the clock source selection can be controlled either statically or dynamically. The user has the option of statically selecting the clock source by using the Quartus II software to set specific configuration bits in the configuration file (**.sof** or **.pof**) or the user can control the selection dynamically by using internal logic to drive the multiplexor select inputs. When selecting statically, the clock source can be set to any of the inputs to the select multiplexor. When selecting the clock source dynamically, you can either select between two PLL outputs (such as the C0 or C1 outputs from one PLL), between two PLLs (such as the C0/C1 clock output of one PLL or the C0/C1 c1ock output of the other PLL), between two clock pins (such as CLK0 or CLK1), or between a combination of clock pins or PLL outputs. The clock outputs from corner PLLs cannot be dynamically selected through the global control block.

For the regional and PLL_OUT clock control block, the clock source selection can only be controlled statically using configuration bits. Any of the inputs to the clock select multiplexor can be set as the clock source.

Table 2–14. DQS & DQ Bus Mode Support (Part 2 of 2) *Note (1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2S90	484-pin Hybrid FineLine BGA	8	4	0	0
	780-pin FineLine BGA	18	8	4	0
	1,020-pin FineLine BGA	36	18	8	4
	1,508-pin FineLine BGA	36	18	8	4
EP2S130	780-pin FineLine BGA	18	8	4	0
	1,020-pin FineLine BGA	36	18	8	4
	1,508-pin FineLine BGA	36	18	8	4
EP2S180	1,020-pin FineLine BGA	36	18	8	4
	1,508-pin FineLine BGA	36	18	8	4

Notes to Table 2–14:
(1) Check the pin table for each DQS/DQ group in the different modes.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

The Stratix II device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed the phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits.

Figure 2–56 illustrates the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

For more information on tolerance specifications for on-chip termination with calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*.

On-Chip Parallel Termination with Calibration

Stratix II devices support on-chip parallel termination with calibration for column I/O pins only. There is one calibration circuit for the top I/O banks and one circuit for the bottom I/O banks. Each on-chip parallel termination calibration circuit compares the total impedance of each I/O buffer to the external 50-Ω resistors connected to the RUP and RDN pins and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.

On-chip parallel termination with calibration is only supported for input pins.

For more information on on-chip termination supported by Stratix II devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

For more information on tolerance specifications for on-chip termination with calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*.

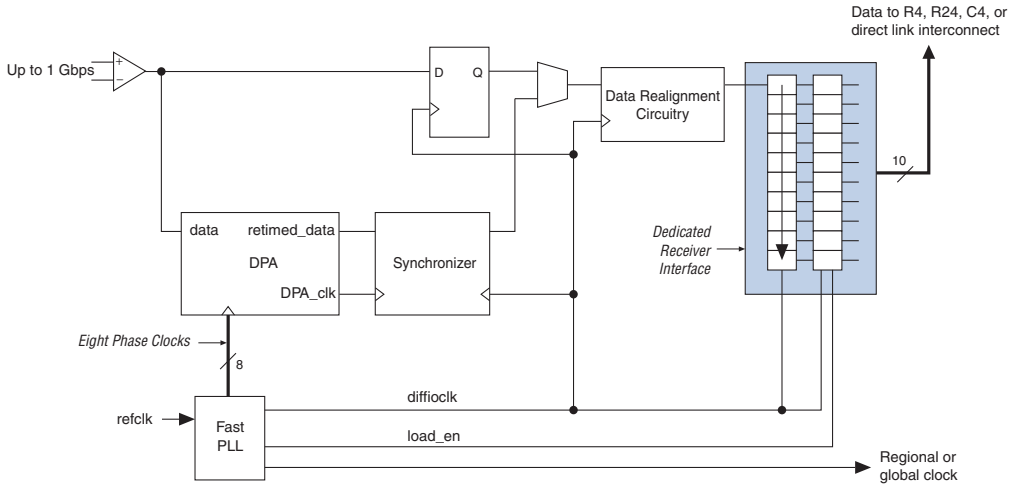
MultiVolt I/O Interface

The Stratix II architecture supports the MultiVolt I/O interface feature that allows Stratix II devices in all packages to interface with systems of different supply voltages.

The Stratix II VCCINT pins must always be connected to a 1.2-V power supply. With a 1.2-V V_{CCINT} level, input pins are 1.5-, 1.8-, 2.5-, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (for example, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems).

The Stratix II VCCPD power pins must be connected to a 3.3-V power supply. These power pins are used to supply the pre-driver power to the output buffers, which increases the performance of the output pins. The VCCPD pins also power configuration input pins and JTAG input pins.

Figure 2–59. Stratix II Receiver Channel



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the VCO can feed to the DPA circuitry.

For more information on the fast PLL, see the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of the channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Since every channel utilizing the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

Table 5–5. LVTTL Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(2)*		0.45	V

Notes to Tables 5–5:

(1) Stratix II devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–6. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		3.135	3.465	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA *(2)*	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA *(2)*		0.2	V

Notes to Table 5–6:

(1) Stratix II devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–7. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –1mA *(2)*	2.0		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA *(2)*		0.4	V

Notes to Table 5–7:

(1) Stratix II devices V_{CCIO} voltage level support of 2.5 ± -5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–17. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Reference voltage		0.855	0.900	0.945	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.125			V
V_{IL} (DC)	Low-level DC input voltage				V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.25			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{CCIO} – 0.28			V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*			0.28	V

Note to Table 5–17:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–18. SSTL-18 Class I & II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{SWING} (DC)	DC differential input voltage		0.25			V
V_X (AC)	AC differential input cross point voltage		(V_{CCIO}/2) – 0.175		(V_{CCIO}/2) + 0.175	V
V_{SWING} (AC)	AC differential input voltage		0.5			V
V_{ISO}	Input clock signal offset voltage			0.5 × V_{CCIO}		V
ΔV_{ISO}	Input clock signal offset voltage variation			±200		mV
V_{OX} (AC)	AC differential cross point voltage		(V_{CCIO}/2) – 0.125		(V_{CCIO}/2) + 0.125	V

Table 5–23. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 5–23:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–24. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Note to Table 5–24:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Internal Timing Parameters

See Tables 5–37 through 5–42 for internal timing parameters.

Table 5–37. LE_FF Internal Timing Microparameters

Symbol	Parameter	-3 Speed Grade *(1)*		-3 Speed Grade *(2)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min *(3)*	Max	Min *(3)*	Max	Min *(4)*	Max	Min *(3)*	Max	
t_{SU}	LE register setup time before clock	90		95		104 104		121		ps
t_{H}	LE register hold time after clock	149		157		172 172		200		ps
t_{CO}	LE register clock-to-output delay	62	94	62	99	59 62	109	62	127	ps
t_{CLR}	Minimum clear pulse width	204		214		234 234		273		ps
t_{PRE}	Minimum preset pulse width	204		214		234 234		273		ps
t_{CLKL}	Minimum clock low time	612		642		703 703		820		ps
t_{CLKH}	Minimum clock high time	612		642		703 703		820		ps
t_{LUT}		162	378	162	397	162 170	435	162	507	ps
t_{ADDER}		354	619	354	650	354 372	712	354	829	ps

Notes to Table 5–37:

(1) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.

(2) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

(3) For the -3 and -5 speed grades, the minimum timing is for the commercial temperature grade. Only -4 speed grade devices offer the industrial temperature grade.

(4) For the -4 speed grade, the first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.

EP2S90 Clock Timing Parameters

Tables 5–56 through 5–59 show the maximum clock timing parameters for EP2S90 devices.

Table 5–56. EP2S90 Column Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.768	1.850	3.033	3.473	4.040	ns
t_{COUT}	1.611	1.685	2.791	3.195	3.716	ns
t_{PLLCIN}	-0.127	-0.117	0.125	0.129	0.144	ns
$t_{PLLCOUT}$	-0.284	-0.282	-0.117	-0.149	-0.18	ns

Table 5–57. EP2S90 Column Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.783	1.868	3.058	3.502	4.070	ns
t_{COUT}	1.626	1.703	2.816	3.224	3.746	ns
t_{PLLCIN}	-0.137	-0.127	0.115	0.119	0.134	ns
$t_{PLLCOUT}$	-0.294	-0.292	-0.127	-0.159	-0.19	ns

Table 5–58. EP2S90 Row Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.566	1.638	2.731	3.124	3.632	ns
t_{COUT}	1.571	1.643	2.727	3.120	3.627	ns
t_{PLLCIN}	-0.326	-0.326	-0.178	-0.218	-0.264	ns
$t_{PLLCOUT}$	-0.321	-0.321	-0.182	-0.222	-0.269	ns

Table 5–62. EP2S130 Row Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.680	1.760	3.070	3.351	3.892	ns
t_{COUT}	1.685	1.765	3.066	3.347	3.887	ns
t_{PLLCIN}	-0.113	-0.124	-0.12	-0.138	-0.168	ns
$t_{PLLCOUT}$	-0.108	-0.119	-0.124	-0.142	-0.173	ns

Table 5–63. EP2S130 Row Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.690	1.770	3.075	3.362	3.905	ns
t_{COUT}	1.695	1.775	3.071	3.358	3.900	ns
t_{PLLCIN}	-0.087	-0.097	-0.075	-0.089	-0.11	ns
$t_{PLLCOUT}$	-0.082	-0.092	-0.079	-0.093	-0.115	ns

EP2S180 Clock Timing Parameters

Tables 5–64 through 5–67 show the maximum clock timing parameters for EP2S180 devices.

Table 5–64. EP2S180 Column Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	2.001	2.095	3.643	3.984	4.634	ns
t_{COUT}	1.844	1.930	3.389	3.706	4.310	ns
t_{PLLCIN}	-0.307	-0.297	0.053	0.046	0.048	ns
$t_{PLLCOUT}$	-0.464	-0.462	-0.201	-0.232	-0.276	ns

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 2 of 5) *Note (1)*

I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
SSTL-18 Class I	4 mA	200	150	150	200	150	150	200	150	150
	6 mA	350	250	200	350	250	200	350	250	200
	8 mA	450	300	300	450	300	300	450	300	300
	10 mA	500	400	400	500	400	400	500	400	400
	12 mA	700	550	400	-	-	-	650	550	400
SSTL-18 Class II	8 mA	200	200	150	-	-	-	200	200	150
	16 mA	400	350	350	-	-	-	400	350	350
	18 mA	450	400	400	-	-	-	450	400	400
	20 mA	550	500	450	-	-	-	550	500	450
1.8-V HSTL Class I	4 mA	300	300	300	300	300	300	300	300	300
	6 mA	500	450	450	500	450	450	500	450	450
	8 mA	650	600	600	650	600	600	650	600	600
	10 mA	700	650	600	700	650	600	700	650	600
	12 mA	700	700	650	700	700	650	700	700	650
1.8-V HSTL Class II	16 mA	500	500	450	-	-	-	500	500	450
	18 mA	550	500	500	-	-	-	550	500	500
	20 mA	650	550	550	-	-	-	550	550	550
1.5-V HSTL Class I	4 mA	350	300	300	350	300	300	350	300	300
	6 mA	500	500	450	500	500	450	500	500	450
	8 mA	700	650	600	700	650	600	700	650	600
	10 mA	700	700	650	-	-	-	700	700	650
	12 mA	700	700	700	-	-	-	700	700	700
1.5-V HSTL Class II	16 mA	600	600	550	-	-	-	600	600	550
	18 mA	650	600	600	-	-	-	650	600	600
	20 mA	700	650	600	-	-	-	700	650	600
Differential SSTL-2 Class I *(3)*	8 mA	400	300	300	400	300	300	400	300	300
	12 mA	400	400	350	400	400	350	400	400	350
Differential SSTL-2 Class II *(3)*	16 mA	350	350	300	350	350	300	350	350	300
	20 mA	400	350	350	350	350	297	400	350	350
	24 mA	400	400	350	-	-	-	400	400	350