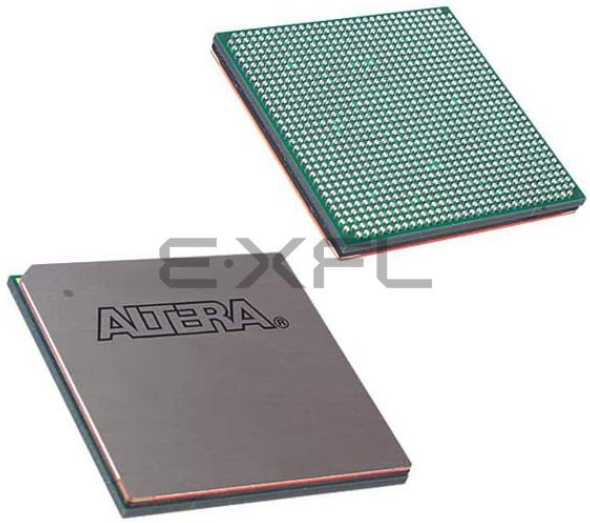

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	718
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s60f1020i4n

After compilation, check the information messages for a full list of I/O, DQ, LVDS, and other pins that are not available because of the selected migration path.

Table 1–4 lists the Stratix II device package offerings and shows the total number of non-migratable user I/O pins when migrating from one density device to a larger density device. Additional I/O pins may not be migratable if migrating from the larger device to the smaller density device.

When moving from one density to a larger density, the larger density device may have fewer user I/O pins. The larger device requires more power and ground pins to support the additional logic within the device. Use the Quartus II Pin Planner to determine which user I/O pins are migratable between the two devices.

Table 1–4. Total Number of Non-Migratable I/O Pins for Stratix II Vertical Migration Paths

Vertical Migration Path	484-Pin FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1020-Pin FineLine BGA	1508-Pin FineLine BGA
EP2S15 to EP2S30	0 *(1)*	0			
EP2S15 to EP2S60	8 *(1)*	0			
EP2S30 to EP2S60	8 *(1)*	8			
EP2S60 to EP2S90				0	
EP2S60 to EP2S130				0	
EP2S60 to EP2S180				0	
EP2S90 to EP2S130			0 *(1)*	16	17
EP2S90 to EP2S180				16	0
EP2S130 to EP2S180				0	0

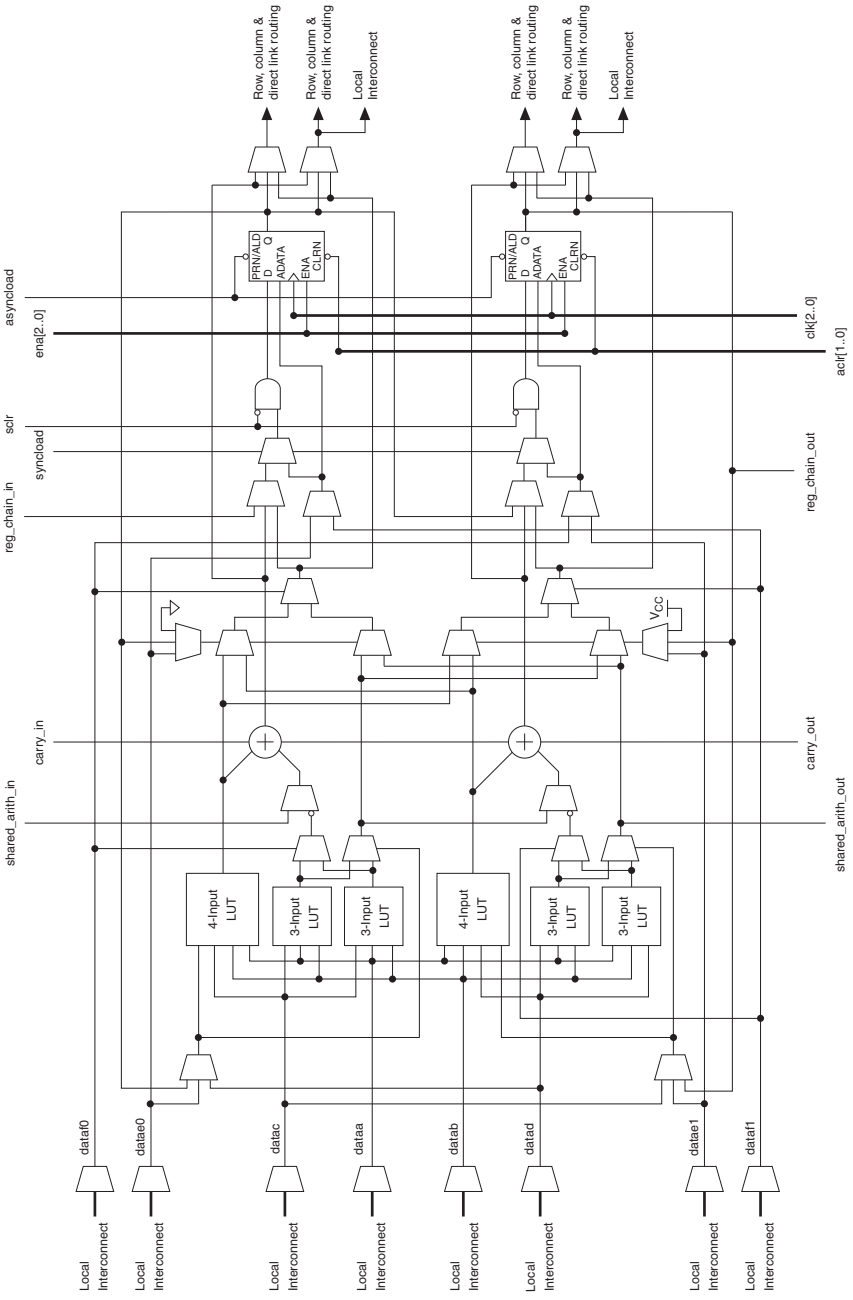
Note to Table 1–4:

(1) Some of the DQ/DQS pins are not migratable. Refer to the Quartus II software information messages for more detailed information.

To determine if your user I/O assignments are correct, run the I/O Assignment Analysis command in the Quartus II software (Processing > Start > Start I/O Assignment Analysis).

Refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook* for more information on pin migration.

Figure 2–6. Stratix II ALM Details



One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, asynchronous load data, and synchronous and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous load data. The asynchronous load data input comes from the `datae` or `dataf` input of the ALM, which are the same inputs that can be used for register packing. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of the ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers independently (see Figure 2–6). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.

See the *Performance & Logic Efficiency Analysis of Stratix II Devices White Paper* for more information on the efficiencies of the Stratix II ALM and comparisons with previous architectures.

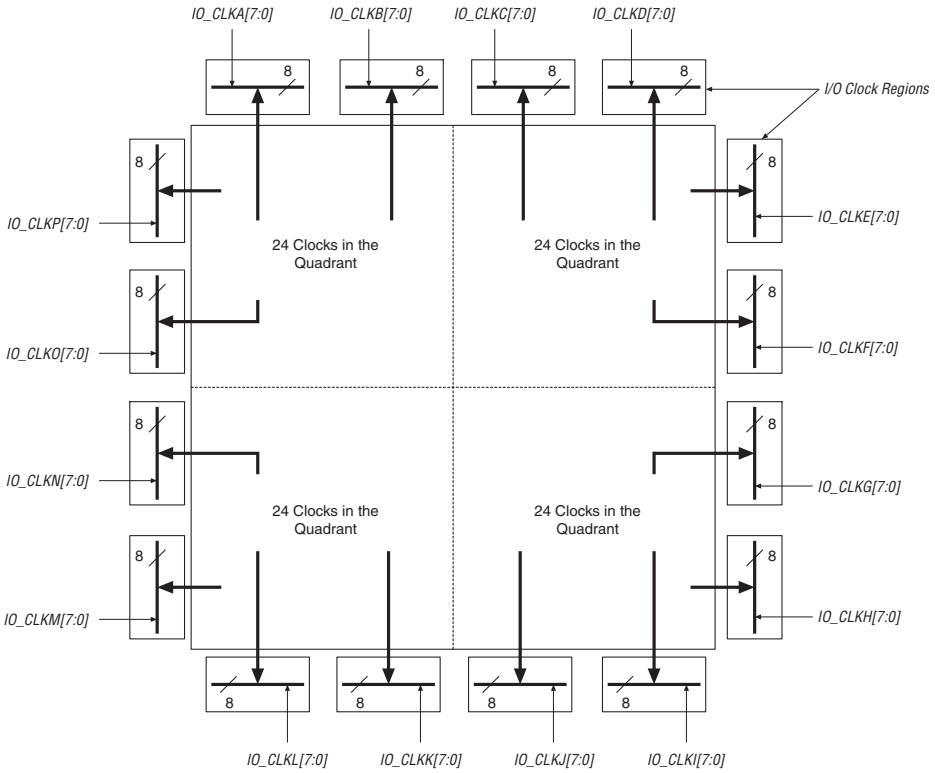
ALM Operating Modes

The Stratix II ALM can operate in one of the following modes:

- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

Each mode uses ALM resources differently. In each mode, eleven available inputs to the ALM--the eight data inputs from the LAB local interconnect; `carry-in` from the previous ALM or LAB; the shared arithmetic chain connection from the previous ALM or LAB; and the register chain connection--are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear,

Figure 2–36. EP2S60, EP2S90, EP2S130 & EP2S180 Device I/O Clock Groups



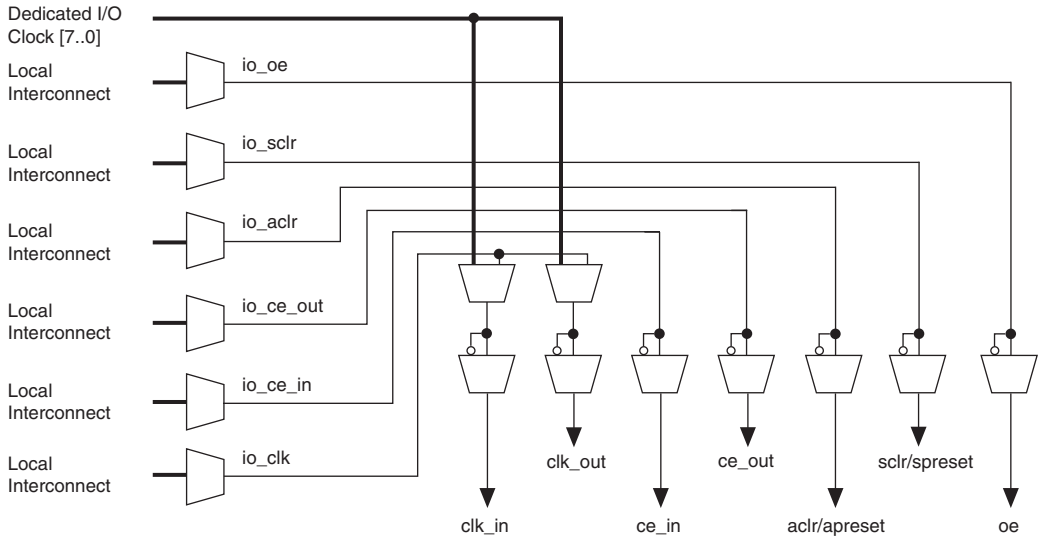
You can use the Quartus II software to control whether a clock input pin drives either a global, regional, or dual-regional clock network. The Quartus II software automatically selects the clocking resources if not specified.

Clock Control Block

Each global clock, regional clock, and PLL external clock output has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable/disable)

Figure 2–50. Control Signal Selection per IOE

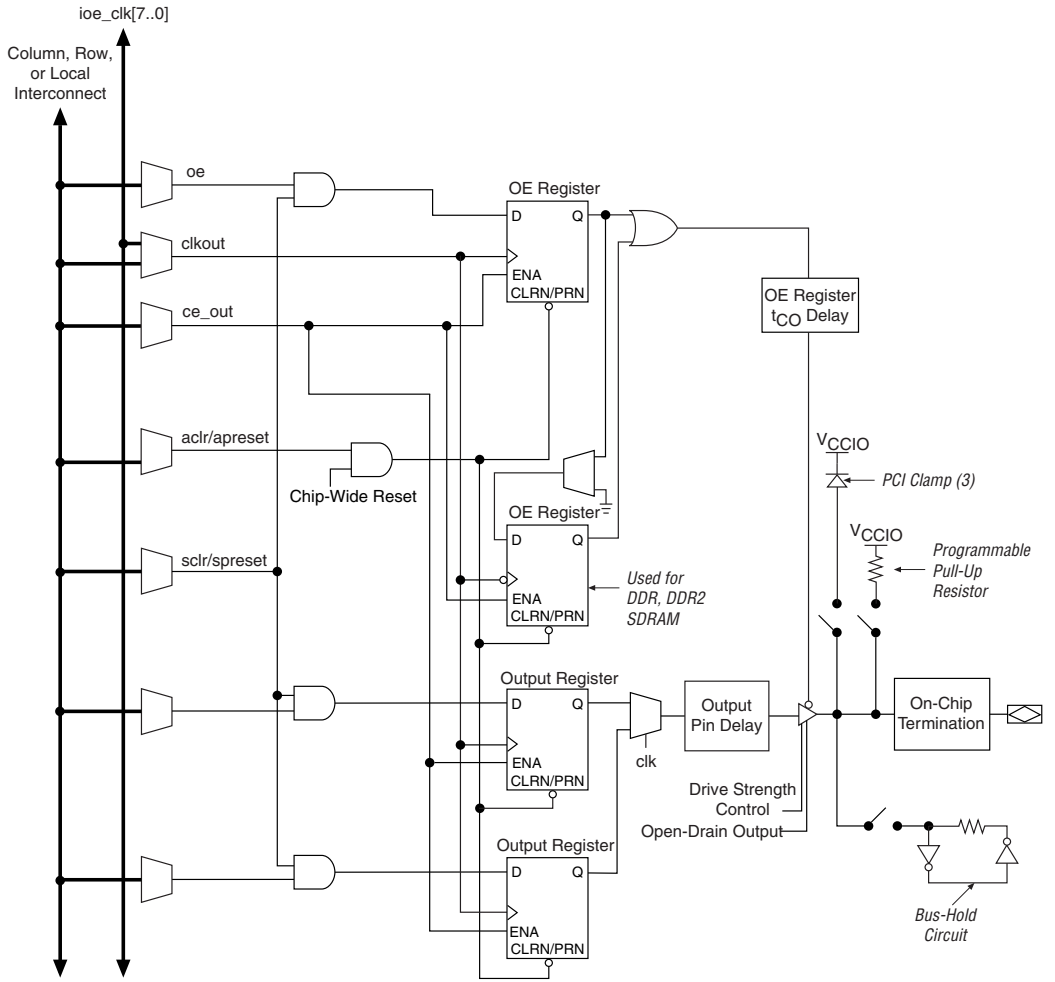


Notes to Figure 2–50:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects.

Figure 2–54. Stratix II IOE in DDR Output I/O Configuration *Notes (1), (2)*



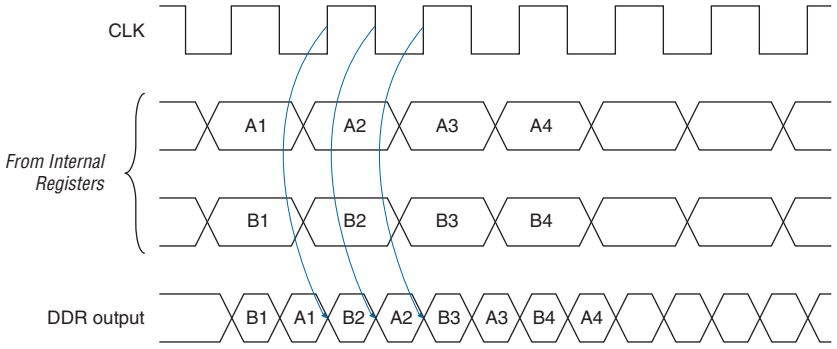
Notes to Figure 2–54:

(1) All input signals to the IOE can be inverted at the IOE.

(2) The tri-state buffer is active low. The DDIO megafunction represents the tri-state buffer as active-high with an inverter at the OE register data port. Similarly, the `aclr` and `apreset` signals are also active-high at the input ports of the DDIO megafunction.

(3) The optional PCI clamp is only available on column I/O pins.

Figure 2–55. Output TIming Diagram in DDR Mode



The Stratix II IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Stratix II devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces. Stratix II devices support DDR and DDR2 SDRAM, QDR II SRAM, RLDRAM II, and SDR SDRAM memory interfaces. In every Stratix II device, the I/O banks at the top (banks 3 and 4) and bottom (banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36. Table 2–14 shows the number of DQ and DQS buses that are supported per device.

Table 2–14. DQS & DQ Bus Mode Support (Part 1 of 2) *Note (1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2S15	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
EP2S30	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
EP2S60	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
	1,020-pin FineLine BGA	36	18	8	4

Differential On-Chip Termination

Stratix II devices support internal differential termination with a nominal resistance value of 100 Ω for LVDS or HyperTransport technology input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. Differential on-chip termination is supported across the full range of supported differential data rates as shown in the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*.

For more information on differential on-chip termination, refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

For more information on tolerance specifications for differential on-chip termination, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*.

On-Chip Series Termination Without Calibration

Stratix II devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Stratix II devices support on-chip series termination for single-ended I/O standards with typical R_S values of 25 and 50 Ω. Once matching impedance is selected, current drive strength is no longer selectable. Table 2–17 shows the list of output standards that support on-chip series termination without calibration.

On-Chip Series Termination with Calibration

Stratix II devices support on-chip series termination with calibration in column I/O pins in top and bottom banks. There is one calibration circuit for the top I/O banks and one circuit for the bottom I/O banks. Each on-chip series termination calibration circuit compares the total impedance of each I/O buffer to the external 25- or 50-Ω resistors connected to the `RUP` and `RDN` pins, and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.

For more information on series on-chip termination supported by Stratix II devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

Figure 3–1. External Temperature-Sensing Diode

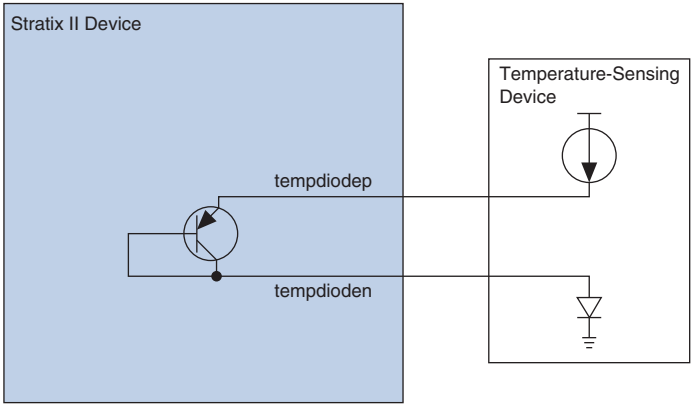


Table 3–6 shows the specifications for bias voltage and current of the Stratix II temperature sensing diode.

Table 3–6. Temperature-Sensing Diode Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
IBIAS high	80	100	120	µA
IBIAS low	8	10	12	µA
VBP - VBN	0.3		0.9	V
VBN		0.7		V
Series resistance			3	Ω

4. Hot Socketing & Power-On Reset

SII51004-3.2

Stratix® II devices offer hot socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a Stratix II board in a system during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot socketing feature also removes some of the difficulty when you use Stratix II devices on printed circuit boards (PCBs) that also contain a mixture of 5.0-, 3.3-, 2.5-, 1.8-, 1.5- and 1.2-V devices. With the Stratix II hot socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Stratix II hot socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter also discusses the power-on reset (POR) circuitry in Stratix II devices. The POR circuitry keeps the devices in the reset state until the V_{CC} is within operating range.

Stratix II Hot-Socketing Specifications

Stratix II devices offer hot socketing capability with all three features listed above without any external components or special design requirements. The hot socketing feature in Stratix II devices allows:

- The device can be driven before power-up without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO}, V_{CCPD}, or V_{CCINT} power supplies. External input signals to I/O pins of the device do not internally power the V_{CCIO} or V_{CCINT} power supplies of the device via internal paths within the device.

Table 5–14. 3.3-V PCI Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low-level input voltage		–0.3		$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–15. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.30		$0.35 \times V_{CCIO}$	V
V_{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–16. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Reference voltage		0.855	0.900	0.945	V
V_{TT}	Termination voltage		$V_{REF} – 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{IH} (DC)	High-level DC input voltage		$V_{REF} + 0.125$			V
V_{IL} (DC)	Low-level DC input voltage				$V_{REF} – 0.125$	V
V_{IH} (AC)	High-level AC input voltage		$V_{REF} + 0.25$			V
V_{IL} (AC)	Low-level AC input voltage				$V_{REF} – 0.25$	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	$V_{TT} + 0.475$			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*			$V_{TT} – 0.475$	V

Note to Table 5–16:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–17. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Reference voltage		0.855	0.900	0.945	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.125			V
V_{IL} (DC)	Low-level DC input voltage				V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.25			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{CCIO} – 0.28			V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*			0.28	V

Note to Table 5–17:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–18. SSTL-18 Class I & II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{SWING} (DC)	DC differential input voltage		0.25			V
V_X (AC)	AC differential input cross point voltage		(V_{CCIO}/2) – 0.175		(V_{CCIO}/2) + 0.175	V
V_{SWING} (AC)	AC differential input voltage		0.5			V
V_{ISO}	Input clock signal offset voltage			0.5 × V_{CCIO}		V
ΔV_{ISO}	Input clock signal offset voltage variation			±200		mV
V_{OX} (AC)	AC differential cross point voltage		(V_{CCIO}/2) – 0.125		(V_{CCIO}/2) + 0.125	V

Table 5–21. SSTL-2 Class I & II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.500	2.625	V
V_{SWING} (DC)	DC differential input voltage		0.36			V
V_X (AC)	AC differential input cross point voltage		$(V_{CCIO}/2) – 0.2$		$(V_{CCIO}/2) + 0.2$	V
V_{SWING} (AC)	AC differential input voltage		0.7			V
V_{ISO}	Input clock signal offset voltage			$0.5 \times V_{CCIO}$		V
ΔV_{ISO}	Input clock signal offset voltage variation			±200		mV
V_{OX} (AC)	AC differential output cross point voltage		$(V_{CCIO}/2) – 0.2$		$(V_{CCIO}/2) + 0.2$	V

Table 5–22. 1.2-V HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.14	1.20	1.26	V
V_{REF}	Reference voltage		$0.48 \times V_{CCIO}$	$0.50 \times V_{CCIO}$	$0.52 \times V_{CCIO}$	V
V_{IH} (DC)	High-level DC input voltage		$V_{REF} + 0.08$		$V_{CCIO} + 0.15$	V
V_{IL} (DC)	Low-level DC input voltage		–0.15		$V_{REF} – 0.08$	V
V_{IH} (AC)	High-level AC input voltage		$V_{REF} + 0.15$		$V_{CCIO} + 0.24$	V
V_{IL} (AC)	Low-level AC input voltage		–0.24		$V_{REF} – 0.15$	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA	$V_{REF} + 0.15$		$V_{CCIO} + 0.15$	V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA	–0.15		$V_{REF} – 0.15$	V

The performance numbers in Table 5–36 are extracted from the Quartus II software version 5.1 SP1.

Table 5–36. Stratix II Performance Notes (Part 1 of 6) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
LE	16-to-1 multiplexer *(4)*	21	0	0	654.87	625.0	523.83	460.4	MHz
	32-to-1 multiplexer *(4)*	38	0	0	519.21	473.26	464.25	384.17	MHz
	16-bit counter	16	0	0	566.57	538.79	489.23	421.05	MHz
	64-bit counter	64	0	0	244.31	232.07	209.11	181.38	MHz
TriMatrix Memory M512 block	Simple dual-port RAM 32 × 18 bit	0	1	0	500.00	476.19	434.02	373.13	MHz
	FIFO 32 x 18 bit	22	1	0	500.00	476.19	434.78	373.13	MHz
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36 bit *(8)*	0	1	0	540.54	515.46	469.48	401.60	MHz
	True dual-port RAM 128 × 18 bit *(8)*	0	1	0	540.54	515.46	469.48	401.60	MHz
	FIFO 128 × 36 bit	22	1	0	530.22	499.00	469.48	401.60	MHz
	Simple dual-port RAM 128 × 36 bit *(9)*	0	1	0	475.28	453.30	413.22	354.10	MHz
	True dual-port RAM 128 × 18 bit *(9)*	0	1	0	475.28	453.30	413.22	354.10	MHz

Table 5–36. Stratix II Performance Notes (Part 4 of 6) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
Larger designs	8-bit, 1024-point, single output, two parallel FFT engines, burst, three multiplier and five adders FFT function	1725	10	6	430.29	401.92	373.13	319.08	MHz
	8-bit, 1024-point, single output, two parallel FFT engines, burst, four multipliers and two adders FFT function	1594	10	8	422.65	407.33	373.13	329.10	MHz
	8-bit, 1024-point, quadrant output, one parallel FFT engine, burst, three multipliers and five adders FFT function	2361	10	9	315.45	342.81	325.73	284.25	MHz
	8-bit, 1024-point, quadrant output, one parallel FFT engine, burst, four multipliers and two adders FFT function	2165	10	12	373.13	369.54	317.96	256.14	MHz
	8-bit, 1024-point, quadrant output, two parallel FFT engines, burst, three multipliers and five adders FFT function	3996	14	18	378.50	367.10	332.33	288.68	MHz
	8-bit, 1024-point, quadrant output, two parallel FFT engines, burst, four multipliers and two adders FFT function	3604	14	24	391.38	361.14	340.25	280.89	MHz

Table 5–74. Stratix II I/O Input Delay for Row Pins (Part 2 of 2)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (1)	-3 Speed Grade (2)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
1.5-V HSTL Class II	t_{PI}	602	631	1056	1107	1212	1413	ps
	t_{PCOUT}	278	292	529	555	608	708	ps
1.8-V HSTL Class I	t_{PI}	577	605	960	1006	1101	1285	ps
	t_{PCOUT}	253	266	433	454	497	580	ps
1.8-V HSTL Class II	t_{PI}	577	605	960	1006	1101	1285	ps
	t_{PCOUT}	253	266	433	454	497	580	ps
LVDS	t_{PI}	515	540	948	994	1088	1269	ps
	t_{PCOUT}	191	201	421	442	484	564	ps
HyperTransport	t_{PI}	515	540	948	994	1088	1269	ps
	t_{PCOUT}	191	201	421	442	484	564	ps

Notes for Table 5–74:
(1) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(2) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 1 of 8)

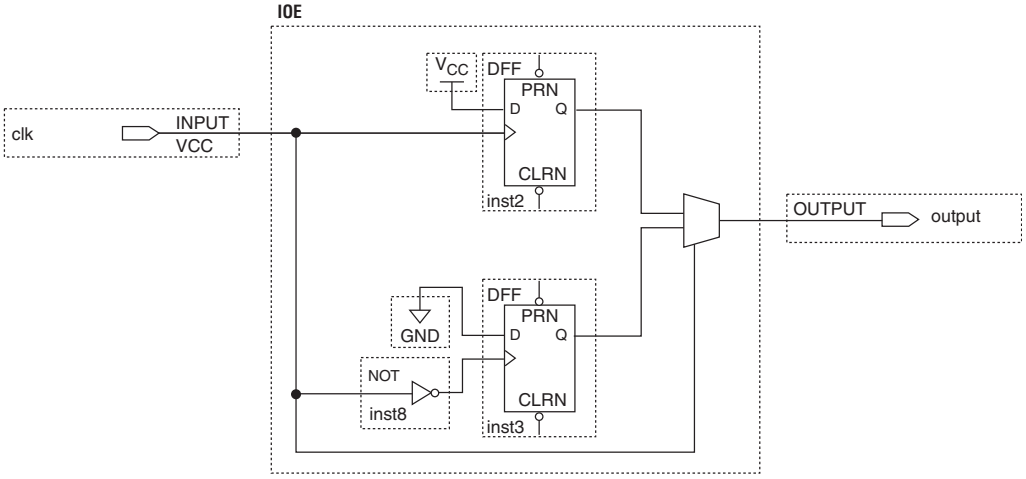
I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
LVTTL	4 mA	t_{OP}	1178	1236	2351	2467	2702	2820	ps
		t_{DIP}	1198	1258	2417	2537	2778	2910	ps
	8 mA	t_{OP}	1041	1091	2036	2136	2340	2448	ps
		t_{DIP}	1061	1113	2102	2206	2416	2538	ps
	12 mA	t_{OP}	976	1024	2036	2136	2340	2448	ps
		t_{DIP}	996	1046	2102	2206	2416	2538	ps
	16 mA	t_{OP}	951	998	1893	1986	2176	2279	ps
		t_{DIP}	971	1020	1959	2056	2252	2369	ps
	20 mA	t_{OP}	931	976	1787	1875	2054	2154	ps
		t_{DIP}	951	998	1853	1945	2130	2244	ps
	24 mA (1)	t_{OP}	924	969	1788	1876	2055	2156	ps
		t_{DIP}	944	991	1854	1946	2131	2246	ps

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 2 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
1.8-V LVTTL/LVCMOS	2 mA	951	1421	1421	951	1421	1421	904	1421	1421
	4 mA	405	516	516	405	516	516	393	516	516
	6 mA	261	325	325	261	325	325	253	325	325
	8 mA	223	274	274	223	274	274	224	274	274
	10 mA	194	236	236	-	-	-	199	236	236
	12 mA	174	209	209	-	-	-	180	209	209
1.5-V LVTTL/LVCMOS	2 mA	652	963	963	652	963	963	618	963	963
	4 mA	333	347	347	333	347	347	270	347	347
	6 mA	182	247	247	-	-	-	198	247	247
	8 mA	135	194	194	-	-	-	155	194	194
SSTL-2 Class I	8 mA	364	680	680	364	680	680	350	680	680
	12 mA	163	207	207	163	207	207	188	207	207
SSTL-2 Class II	16 mA	118	147	147	118	147	147	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116
SSTL-18 Class I	4 mA	458	570	570	458	570	570	505	570	570
	6 mA	305	380	380	305	380	380	336	380	380
	8 mA	225	282	282	225	282	282	248	282	282
	10 mA	167	220	220	167	220	220	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175
SSTL-18 Class II	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
SSTL-2 Class I	8 mA	364	680	680	364	680	680	350	680	680
	12 mA	163	207	207	163	207	207	188	207	207
SSTL-2 Class II	16 mA	118	147	147	118	147	147	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116

However, when the output is a double data rate input/output (DDIO) signal, both edges of the input clock signal (positive and negative) trigger output transitions (Figure 5–9). Therefore, any distortion on the input clock and the input clock buffer affect the output DCD.

Figure 5–9. DCD Measurement Technique for DDIO (Double-Data Rate) Outputs



When an FPGA PLL generates the internal clock, the PLL output clocks the IOE block. As the PLL only monitors the positive edge of the reference clock input and internally re-creates the output clock signal, any DCD present on the reference clock is filtered out. Therefore, the DCD for a DDIO output with PLL in the clock path is better than the DCD for a DDIO output without PLL in the clock path.

Tables 5–80 through 5–87 give the maximum DCD in absolution derivation for different I/O standards on Stratix II devices. Examples are also provided that show how to calculate DCD as a percentage.

Table 5–80. Maximum DCD for Non-DDIO Output on Row I/O Pins (Part 1 of 2) *Note (1)*

Row I/O Output Standard	Maximum DCD for Non-DDIO Output		
	-3 Devices	-4 & -5 Devices	Unit
3.3-V LVTTTL	245	275	ps
3.3-V LVCMOS	125	155	ps
2.5 V	105	135	ps

High-Speed I/O Specifications

Table 5–88 provides high-speed timing specifications definitions.

Table 5–88. High-Speed Timing Specifications & Definitions

High-Speed Timing Specifications	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
J	Deserialization factor (width of parallel data bus).
W	PLL multiplication factor.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter	Peak-to-peak input jitter on high-speed PLLs.
Output jitter	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Table 5–89 shows the high-speed I/O timing specifications for -3 speed grade Stratix II devices.

Table 5–89. High-Speed I/O Specifications for -3 Speed Grade (Part 1 of 2) *Notes (1), (2)*

Symbol	Conditions	-3 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (clock frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*	16		520	MHz
	W = 1 (SERDES bypass, LVDS only)	16		500	MHz
	W = 1 (SERDES used, LVDS only)	150		717	MHz

Table 5–97. DQS Phase Jitter Specifications for DLL-Delayed Clock (tDQS PHASE_JITTER) Note (1)

Number of DQS Delay Buffer Stages (2)	DQS Phase Jitter	Unit
1	30	ps
2	60	ps
3	90	ps
4	120	ps

Notes to Table 5–97:
(1) Peak-to-peak phase jitter on the phase shifted DDS clock (digital jitter is caused by DLL tracking).
(2) Delay stages used for requested DQS phase shift are reported in your project's Compilation Report in the Quartus II software.

Table 5–98. DQS Phase-Shift Error Specifications for DLL-Delayed Clock (tDQS_PSERR) (1)

Number of DQS Delay Buffer Stages (2)	–3 Speed Grade	–4 Speed Grade	–5 Speed Grade	Unit
1	25	30	35	ps
2	50	60	70	ps
3	75	90	105	ps
4	100	120	140	ps

Notes to Table 5–98:
(1) This error specification is the absolute maximum and minimum error. For example, skew on three delay buffer stages in a C3 speed grade is 75 ps or ± 37.5 ps.
(2) Delay stages used for requested DQS phase shift are reported in your project's Compilation Report in the Quartus II software.

Table 5–99. DQS Bus Clock Skew Adder Specifications (tDQS_CLOCK_SKEW_ADDER)

Mode	DQS Clock Skew Adder	Unit
×4 DQ per DQS	40	ps
×9 DQ per DQS	70	ps
×18 DQ per DQS	75	ps
×36 DQ per DQS	95	ps

Note to Table 5–99:
(1) This skew specification is the absolute maximum and minimum skew. For example, skew on a ×4 DQ group is 40 ps or ±20 ps.