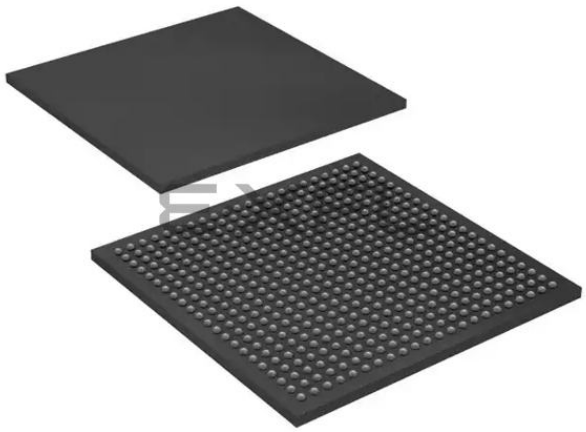

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

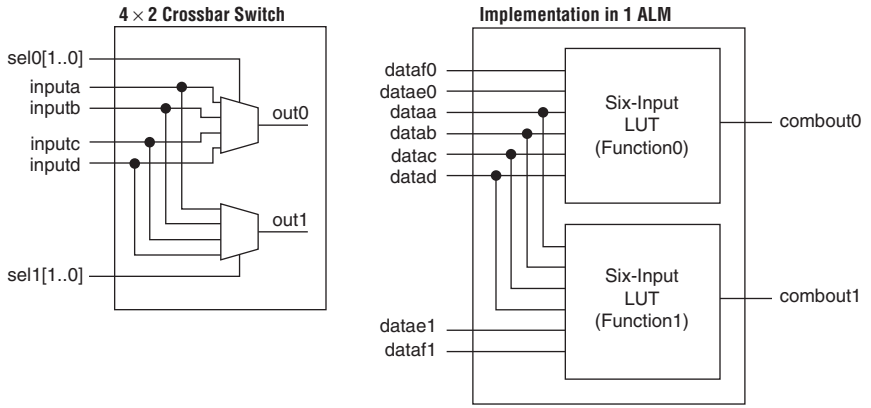
Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	334
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s60f484c5n

Chapter 6. Reference & Ordering Information

For the packing of two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are dataa and datab. The combination of a four-input function with a five-input function requires one common input (either dataa or datab).

In the case of implementing two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–8. The shared inputs are dataa, datab, datac, and datad, while the unique select lines are datae0 and dataf0 for function0, and datae1 and dataf1 for function1. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

Figure 2–8. 4 × 2 Crossbar Switch Example

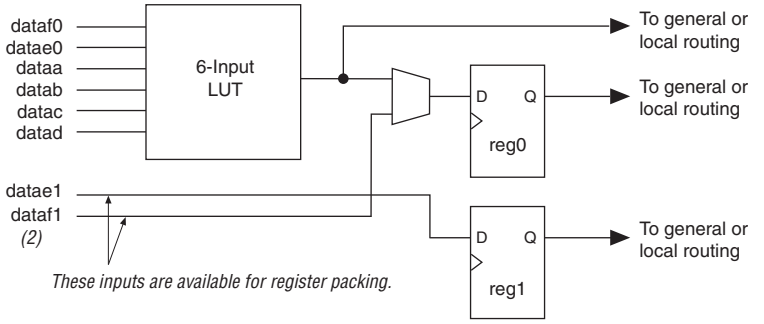


In a sparsely used device, functions that could be placed into one ALM may be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically utilizes the full potential of the Stratix II ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments.

Any six-input function can be implemented utilizing inputs dataa, datab, datac, datad, and either datae0 and dataf0 or datae1 and dataf1. If datae0 and dataf0 are utilized, the output is driven to register0, and/or register0 is bypassed and the data drives out to the interconnect using the top set of output drivers (see Figure 2–9). If

datae1 and dataf1 are utilized, the output drives to register1 and/or bypasses register1 and drives to the interconnect using the bottom set of output drivers. The Quartus II Compiler automatically selects the inputs to the LUT. Asynchronous load data for the register comes from the datae or dataf input of the ALM. ALMs in normal mode support register packing.

Figure 2–9. 6-Input Function in Normal Mode *Notes (1), (2)*



Notes to Figure 2–9:

(1) If datae1 and dataf1 are used as inputs to the six-input function, then datae0 and dataf0 are available for register packing.

(2) The dataf1 input is available for register packing only if the six-input function is un-registered.

Extended LUT Mode

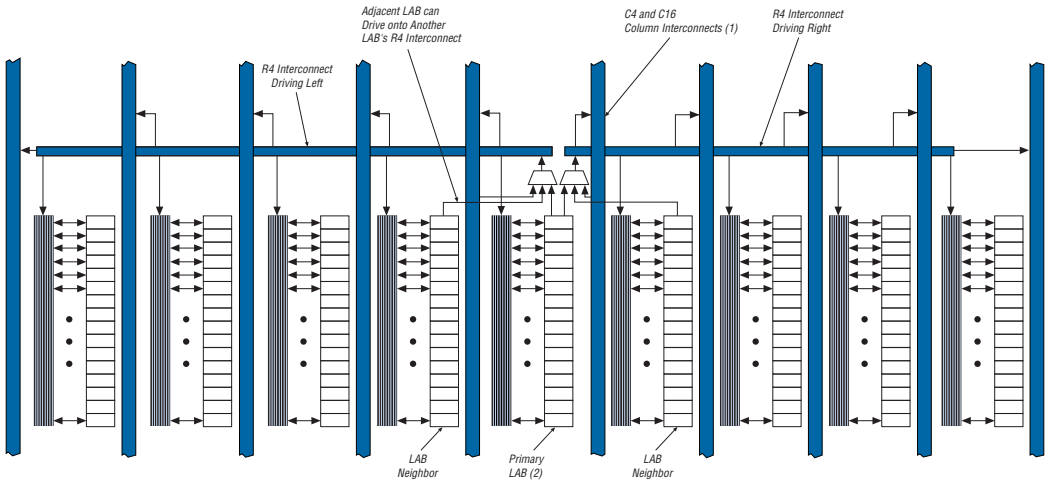
The extended LUT mode is used to implement a specific set of seven-input functions. The set must be a 2-to-1 multiplexer fed by two arbitrary five-input functions sharing four inputs. Figure 2–10 shows the template of supported seven-input functions utilizing extended LUT mode. In this mode, if the seven-input function is unregistered, the unused eighth input is available for register packing.

Functions that fit into the template shown in Figure 2–10 occur naturally in designs. These functions often appear in designs as "if-else" statements in Verilog HDL or VHDL code.

The direct link interconnect allows an LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself. This provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–16 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by DSP blocks and RAM blocks and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

Figure 2–16. R4 Interconnect Connections *Notes (1), (2), (3)*



Notes to Figure 2–16:

(1) C4 and C16 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

(3) The LABs in Figure 2–16 show the 16 possible logical outputs per LAB.

Table 2–3. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support		✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Output registers	Output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

Notes to Table 2–3:

(1) The M-RAM block does not support memory initializations. However, the M-RAM block can emulate a ROM function using a dual-port RAM bock. The Stratix II device must write to the dual-port memory once and then disable the write-enable ports afterwards.

Memory Block Size

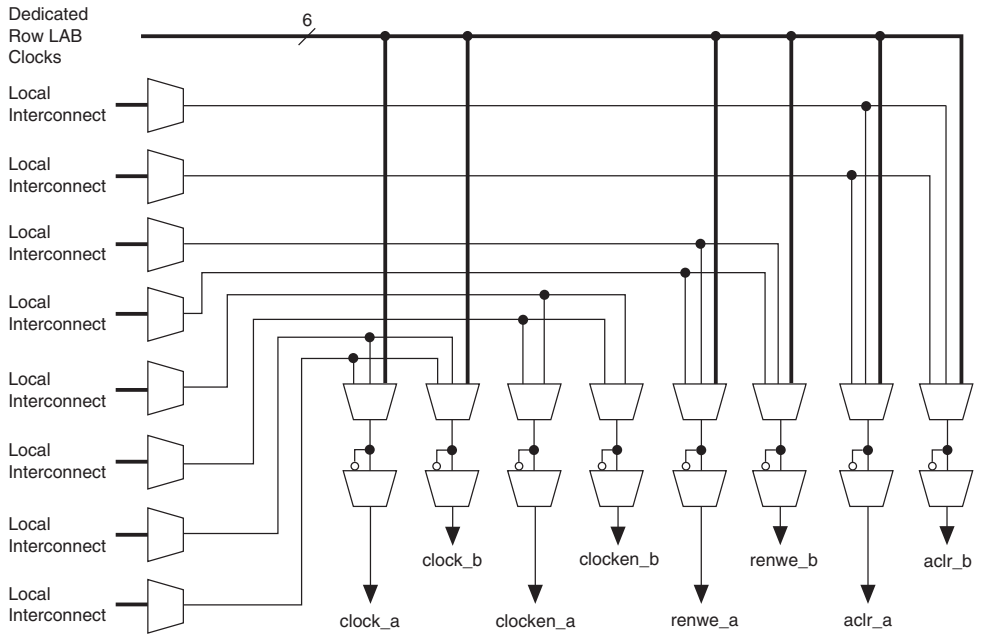
TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

When applied to input registers, the asynchronous clear signal for the TriMatrix embedded memory immediately clears the input registers. However, the output of the memory block does not show the effects until the next clock edge. When applied to output registers, the asynchronous clear signal clears the output registers and the effects are seen immediately.

The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (renwe, address, byte enable, datain, and output registers). Only the output register can be bypassed. The six `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–21.

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K RAM Block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–22 shows the M4K RAM block to logic array interface.

Figure 2–21. M4K RAM Block Control Signals



The LAB row source for control signals, data inputs, and outputs is shown in Table 2–7.

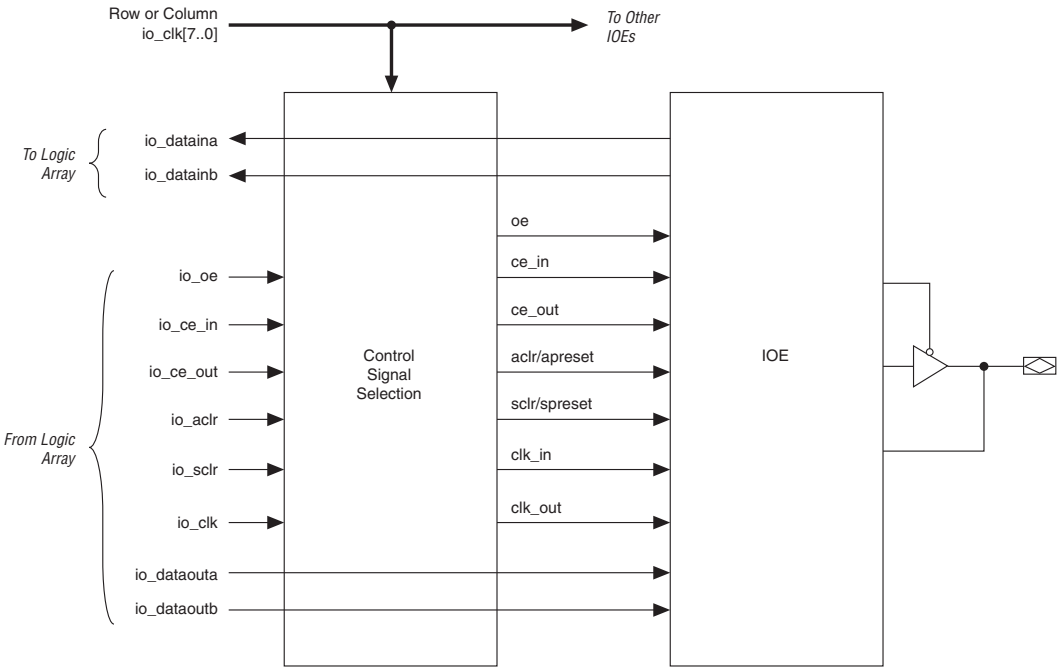
Table 2–7. DSP Block Signal Sources & Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1[17..0] B1[17..0]	OA[17..0] OB[17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2[17..0] B2[17..0]	OC[17..0] OD[17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3[17..0] B3[17..0]	OE[17..0] OF[17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4[17..0] B4[17..0]	OG[17..0] OH[17..0]

See the *DSP Blocks in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook,* for more information on DSP blocks.

There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks (see the "PLLs & Clock Networks" section). Figure 2–49 illustrates the signal paths through the I/O block.

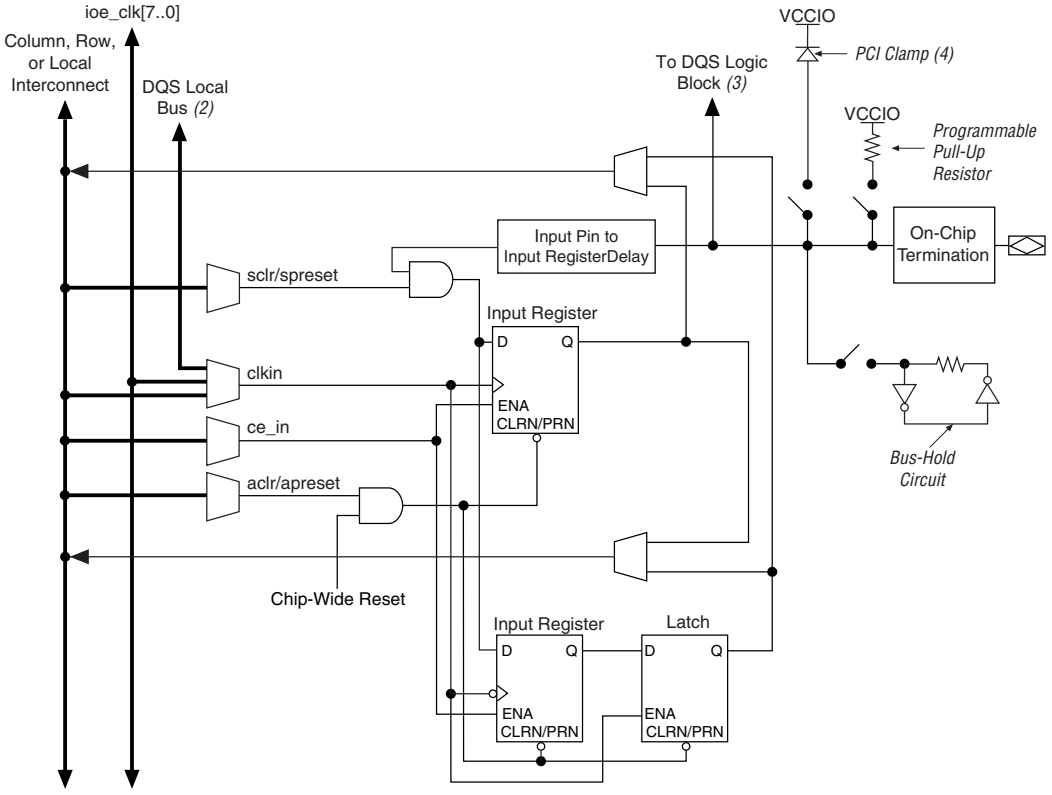
Figure 2–49. Signal Path through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–50 illustrates the control signal selection.

When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used in the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 2–52 shows an IOE configured for DDR input. Figure 2–53 shows the DDR input timing diagram.

Figure 2–52. Stratix II IOE in DDR Input I/O Configuration *Notes (1), (2), (3)*



Notes to Figure 2–52:

(1) All input signals to the IOE can be inverted at the IOE.
(2) This signal connection is only allowed on dedicated DQ function pins.
(3) This signal is for dedicated DQS function pins only.
(4) The optional PCI clamp is only available on column I/O pins.

Table 2–18 summarizes Stratix II MultiVolt I/O support.

Table 2–18. Stratix II MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal (V)					Output Signal (V)					
	1.2	1.5	1.8	2.5	3.3	1.2	1.5	1.8	2.5	3.3	5.0
1.2	(4)	✓ (2)	✓ (2)	✓ (2)	✓ (2)	✓ (4)					
1.5	(4)	✓	✓	✓ (2)	✓ (2)	✓ (3)	✓				
1.8	(4)	✓	✓	✓ (2)	✓ (2)	✓ (3)	✓ (3)	✓			
2.5	(4)			✓	✓	✓ (3)	✓ (3)	✓ (3)	✓		
3.3	(4)			✓	✓	✓ (3)	✓ (3)	✓ (3)	✓ (3)	✓	✓

Notes to Table 2–18:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and select the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.

(2) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable Stratix II V_{IL} maximum and V_{IH} minimum voltage specifications.

(3) Although V_{CCIO} specifies the voltage necessary for the Stratix II device to drive out, a receiving device powered at a different level can still interface with the Stratix II device if it has inputs that tolerate the V_{CCIO} value.

(4) Stratix II devices do not support 1.2-V LVTTL and 1.2-V LVCMOS. Stratix II devices support 1.2-V HSTL.

The TDO and nCEO pins are powered by V_{CCIO} of the bank that they reside in. TDO is in I/O bank 4 and nCEO is in I/O bank 7.

Ideally, the V_{CC} supplies for the I/O buffers of any two connected pins are at the same voltage level. This may not always be possible depending on the V_{CCIO} level of TDO and nCEO pins on master devices and the configuration voltage level chosen by VCCSEL on slave devices. Master and slave devices can be in any position in the chain. Master indicates that it is driving out TDO or nCEO to a slave device.

For multi-device passive configuration schemes, the nCEO pin of the master device drives the nCE pin of the slave device. The VCCSEL pin on the slave device selects which input buffer is used for nCE. When VCCSEL is logic high, it selects the 1.8-V/1.5-V buffer powered by V_{CCIO}. When VCCSEL is logic low it selects the 3.3-V/2.5-V input buffer powered by V_{CCPD}. The ideal case is to have the V_{CCIO} of the nCEO bank in a master device match the VCCSEL settings for the nCE input buffer of the slave device it is connected to, but that may not be possible depending on the application. Table 2–19 contains board design recommendations to ensure that nCEO can successfully drive nCE for all power supply combinations.

4. Hot Socketing & Power-On Reset

SII51004-3.2

Stratix® II devices offer hot socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a Stratix II board in a system during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot socketing feature also removes some of the difficulty when you use Stratix II devices on printed circuit boards (PCBs) that also contain a mixture of 5.0-, 3.3-, 2.5-, 1.8-, 1.5- and 1.2-V devices. With the Stratix II hot socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Stratix II hot socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter also discusses the power-on reset (POR) circuitry in Stratix II devices. The POR circuitry keeps the devices in the reset state until the V_{CC} is within operating range.

Stratix II Hot-Socketing Specifications

Stratix II devices offer hot socketing capability with all three features listed above without any external components or special design requirements. The hot socketing feature in Stratix II devices allows:

- The device can be driven before power-up without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO}, V_{CCPD}, or V_{CCINT} power supplies. External input signals to I/O pins of the device do not internally power the V_{CCIO} or V_{CCINT} power supplies of the device via internal paths within the device.

Figure 5–1. Receiver Input Waveforms for Differential I/O Standards

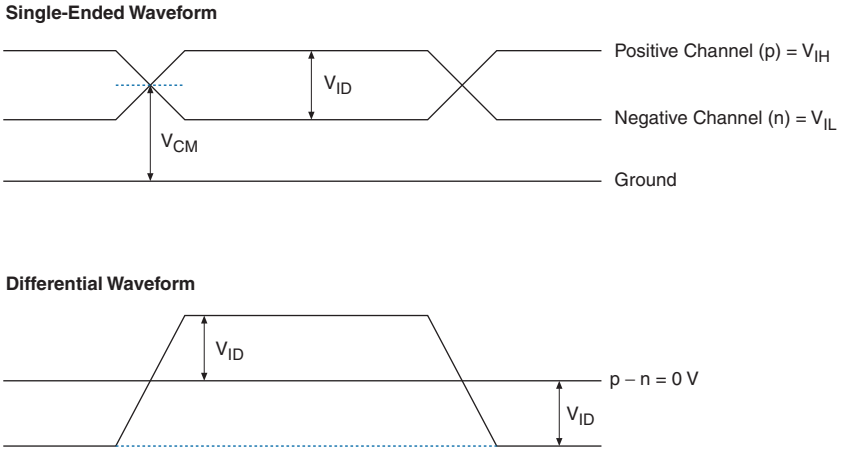


Figure 5–2. Transmitter Output Waveforms for Differential I/O Standards

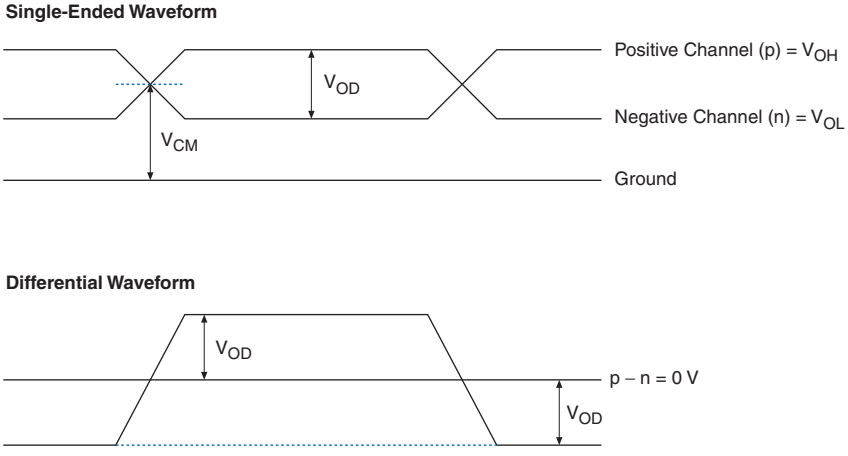


Table 5–17. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Reference voltage		0.855	0.900	0.945	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.125			V
V_{IL} (DC)	Low-level DC input voltage				V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.25			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{CCIO} – 0.28			V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*			0.28	V

Note to Table 5–17:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–18. SSTL-18 Class I & II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{SWING} (DC)	DC differential input voltage		0.25			V
V_X (AC)	AC differential input cross point voltage		(V_{CCIO}/2) – 0.175		(V_{CCIO}/2) + 0.175	V
V_{SWING} (AC)	AC differential input voltage		0.5			V
V_{ISO}	Input clock signal offset voltage			0.5 × V_{CCIO}		V
ΔV_{ISO}	Input clock signal offset voltage variation			±200		mV
V_{OX} (AC)	AC differential cross point voltage		(V_{CCIO}/2) – 0.125		(V_{CCIO}/2) + 0.125	V

The performance numbers in Table 5–36 are extracted from the Quartus II software version 5.1 SP1.

Table 5–36. Stratix II Performance Notes (Part 1 of 6) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
LE	16-to-1 multiplexer *(4)*	21	0	0	654.87	625.0	523.83	460.4	MHz
	32-to-1 multiplexer *(4)*	38	0	0	519.21	473.26	464.25	384.17	MHz
	16-bit counter	16	0	0	566.57	538.79	489.23	421.05	MHz
	64-bit counter	64	0	0	244.31	232.07	209.11	181.38	MHz
TriMatrix Memory M512 block	Simple dual-port RAM 32 × 18 bit	0	1	0	500.00	476.19	434.02	373.13	MHz
	FIFO 32 x 18 bit	22	1	0	500.00	476.19	434.78	373.13	MHz
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36 bit *(8)*	0	1	0	540.54	515.46	469.48	401.60	MHz
	True dual-port RAM 128 × 18 bit *(8)*	0	1	0	540.54	515.46	469.48	401.60	MHz
	FIFO 128 × 36 bit	22	1	0	530.22	499.00	469.48	401.60	MHz
	Simple dual-port RAM 128 × 36 bit *(9)*	0	1	0	475.28	453.30	413.22	354.10	MHz
	True dual-port RAM 128 × 18 bit *(9)*	0	1	0	475.28	453.30	413.22	354.10	MHz

Table 5–39. DSP Block Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min (3)	Max	Min (3)	Max	Min (4)	Max	Min (3)	Max	
t_{CLKL}	Minimum clock low time	1,190		1,249		1,368 1,368		1,594		ps
t_{CLKH}	Minimum clock high time	1,190		1,249		1,368 1,368		1,594		ps

Notes to Table 5–39:

(1) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(2) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.
(3) For the -3 and -5 speed grades, the minimum timing is for the commercial temperature grade. Only -4 speed grade devices offer the industrial temperature grade.
(4) For the -4 speed grade, the first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.

Table 5–40. M512 Block Internal Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min (4)	Max	Min (4)	Max	Min (5)	Max	Min (4)	Max	
t_{M512RC}	Synchronous read cycle time	2,089	2,318	2,089	2.433	1,989 2,089	2,664	2,089	3,104	ps
$t_{M512WERESU}$	Write or read enable setup time before clock	22		23		25 25		29		ps
$t_{M512WEREH}$	Write or read enable hold time after clock	203		213		233 233		272		ps
$t_{M512DATASU}$	Data setup time before clock	22		23		25 25		29		ps
$t_{M512DATAH}$	Data hold time after clock	203		213		233 233		272		ps
$t_{M512WADDRSU}$	Write address setup time before clock	22		23		25 25		29		ps
$t_{M512WADDRH}$	Write address hold time after clock	203		213		233 233		272		ps
$t_{M512RADDRSU}$	Read address setup time before clock	22		23		25 25		29		ps
$t_{M512RADDRH}$	Read address hold time after clock	203		213		233 233		272		ps

Clock Network Skew Adders

The Quartus II software models skew within dedicated clock networks such as global and regional clocks. Therefore, intra-clock network skew adder is not specified. Table 5–68 specifies the clock skew between any two clock networks driving registers in the IOE.

Table 5–68. Clock Network Specifications

Name	Description	Min	Typ	Max	Unit
Clock skew adder EP2S15, EP2S30, EP2S60 *(1)*	Inter-clock network, same side			±50	ps
	Inter-clock network, entire chip			±100	ps
Clock skew adder EP2S90 *(1)*	Inter-clock network, same side			±55	ps
	Inter-clock network, entire chip			±110	ps
Clock skew adder EP2S130 *(1)*	Inter-clock network, same side			±63	ps
	Inter-clock network, entire chip			±125	ps
Clock skew adder EP2S180 *(1)*	Inter-clock network, same side			±75	ps
	Inter-clock network, entire chip			±150	ps

Note to Table 5–68:
(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 3 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
1.8 V	2 mA	t_{OP}	1042	1093	2904	3048	3338	3472	ps
		t_{DIP}	1062	1115	2970	3118	3414	3562	ps
	4 mA	t_{OP}	1047	1098	2248	2359	2584	2698	ps
		t_{DIP}	1067	1120	2314	2429	2660	2788	ps
	6 mA	t_{OP}	974	1022	2024	2124	2326	2434	ps
		t_{DIP}	994	1044	2090	2194	2402	2524	ps
	8 mA	t_{OP}	976	1024	1947	2043	2238	2343	ps
		t_{DIP}	996	1046	2013	2113	2314	2433	ps
	10 mA	t_{OP}	933	978	1882	1975	2163	2266	ps
		t_{DIP}	953	1000	1948	2045	2239	2356	ps
	12 mA (1)	t_{OP}	934	979	1833	1923	2107	2209	ps
		t_{DIP}	954	1001	1899	1993	2183	2299	ps
1.5 V	2 mA	t_{OP}	1023	1073	2505	2629	2879	3002	ps
		t_{DIP}	1043	1095	2571	2699	2955	3092	ps
	4 mA	t_{OP}	963	1009	2023	2123	2325	2433	ps
		t_{DIP}	983	1031	2089	2193	2401	2523	ps
	6 mA	t_{OP}	966	1012	1923	2018	2210	2315	ps
		t_{DIP}	986	1034	1989	2088	2286	2405	ps
	8 mA (1)	t_{OP}	926	971	1878	1970	2158	2262	ps
		t_{DIP}	946	993	1944	2040	2234	2352	ps
SSTL-2 Class I	8 mA	t_{OP}	913	957	1715	1799	1971	2041	ps
		t_{DIP}	933	979	1781	1869	2047	2131	ps
	12 mA (1)	t_{OP}	896	940	1672	1754	1921	1991	ps
		t_{DIP}	916	962	1738	1824	1997	2081	ps
SSTL-2 Class II	16 mA	t_{OP}	876	918	1609	1688	1849	1918	ps
		t_{DIP}	896	940	1675	1758	1925	2008	ps
	20 mA	t_{OP}	877	919	1598	1676	1836	1905	ps
		t_{DIP}	897	941	1664	1746	1912	1995	ps
	24 mA (1)	t_{OP}	872	915	1596	1674	1834	1903	ps
		t_{DIP}	892	937	1662	1744	1910	1993	ps

Table 5–76. Stratix II I/O Output Delay for Row Pins (Part 3 of 3)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
1.8-V HSTL Class I	4 mA	t_{OP}	972	1019	1610	1689	1850	1956	ps
		t_{DIP}	930	976	1555	1632	1787	1883	ps
	6 mA	t_{OP}	975	1022	1580	1658	1816	1920	ps
		t_{DIP}	933	979	1525	1601	1753	1847	ps
	8 mA	t_{OP}	958	1004	1576	1653	1811	1916	ps
		t_{DIP}	916	961	1521	1596	1748	1843	ps
	10 mA	t_{OP}	962	1008	1567	1644	1801	1905	ps
		t_{DIP}	920	965	1512	1587	1738	1832	ps
	12 mA (1)	t_{OP}	953	999	1566	1643	1800	1904	ps
		t_{DIP}	911	956	1511	1586	1737	1831	ps
1.5-V HSTL Class I	4 mA	t_{OP}	970	1018	1591	1669	1828	1933	ps
		t_{DIP}	928	975	1536	1612	1765	1860	ps
	6 mA	t_{OP}	974	1021	1579	1657	1815	1919	ps
		t_{DIP}	932	978	1524	1600	1752	1846	ps
	8 mA (1)	t_{OP}	960	1006	1572	1649	1807	1911	ps
		t_{DIP}	918	963	1517	1592	1744	1838	ps
LVDS		t_{OP}	1018	1067	1723	1808	1980	2089	ps
		t_{DIP}	976	1024	1668	1751	1917	2016	ps
HyperTransport		t_{OP}	1005	1053	1723	1808	1980	2089	ps
		t_{DIP}	963	1010	1668	1751	1917	2016	ps

Notes to Table 5–76:
(1) This is the default setting in the Quartus II software.
(2) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(3) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

Maximum Input & Output Clock Toggle Rate

Maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 2 of 5) *Note (1)*

I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
SSTL-18 Class I	4 mA	200	150	150	200	150	150	200	150	150
	6 mA	350	250	200	350	250	200	350	250	200
	8 mA	450	300	300	450	300	300	450	300	300
	10 mA	500	400	400	500	400	400	500	400	400
	12 mA	700	550	400	-	-	-	650	550	400
SSTL-18 Class II	8 mA	200	200	150	-	-	-	200	200	150
	16 mA	400	350	350	-	-	-	400	350	350
	18 mA	450	400	400	-	-	-	450	400	400
	20 mA	550	500	450	-	-	-	550	500	450
1.8-V HSTL Class I	4 mA	300	300	300	300	300	300	300	300	300
	6 mA	500	450	450	500	450	450	500	450	450
	8 mA	650	600	600	650	600	600	650	600	600
	10 mA	700	650	600	700	650	600	700	650	600
	12 mA	700	700	650	700	700	650	700	700	650
1.8-V HSTL Class II	16 mA	500	500	450	-	-	-	500	500	450
	18 mA	550	500	500	-	-	-	550	500	500
	20 mA	650	550	550	-	-	-	550	550	550
1.5-V HSTL Class I	4 mA	350	300	300	350	300	300	350	300	300
	6 mA	500	500	450	500	500	450	500	500	450
	8 mA	700	650	600	700	650	600	700	650	600
	10 mA	700	700	650	-	-	-	700	700	650
	12 mA	700	700	700	-	-	-	700	700	700
1.5-V HSTL Class II	16 mA	600	600	550	-	-	-	600	600	550
	18 mA	650	600	600	-	-	-	650	600	600
	20 mA	700	650	600	-	-	-	700	650	600
Differential SSTL-2 Class I *(3)*	8 mA	400	300	300	400	300	300	400	300	300
	12 mA	400	400	350	400	400	350	400	400	350
Differential SSTL-2 Class II *(3)*	16 mA	350	350	300	350	350	300	350	350	300
	20 mA	400	350	350	350	350	297	400	350	350
	24 mA	400	400	350	-	-	-	400	400	350

Table 5–100. DQS Phase Offset Delay Per Stage Notes (1), (2), (3)			
Speed Grade	**Min**	**Max**	**Unit**
-3	9	14	ps
-4	9	14	ps
-5	9	15	ps

Notes to Table 5–100:
(1) The delay settings are linear.
(2) The valid settings for phase offset are -64 to +63 for frequency mode 0 and -32 to +31 for frequency modes 1, 2, and 3.
(3) The typical value equals the average of the minimum and maximum values.

Table 5–101. DDIO Outputs Half-Period Jitter Notes (1), (2)			
Name	**Description**	**Max**	**Unit**
$t_{OUTHALFJITTER}$	Half-period jitter (PLL driving DDIO outputs)	200	ps

Notes to Table 5–101:
(1) The worst-case half period is equal to the ideal half period subtracted by the DCD and half-period jitter values.
(2) The half-period jitter was characterized using a PLL driving DDIO outputs.

JTAG Timing Specifications

Figure 5–10 shows the timing requirements for the JTAG signals.

Figure 5–10. Stratix II JTAG Waveforms