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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	492
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s60f672c3

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After compilation, check the information messages for a full list of I/O, DQ, LVDS, and other pins that are not available because of the selected migration path.

Table 1–4 lists the Stratix II device package offerings and shows the total number of non-migratable user I/O pins when migrating from one density device to a larger density device. Additional I/O pins may not be migratable if migrating from the larger device to the smaller density device.



When moving from one density to a larger density, the larger density device may have fewer user I/O pins. The larger device requires more power and ground pins to support the additional logic within the device. Use the Quartus II Pin Planner to determine which user I/O pins are migratable between the two devices.

Table 1–4. Total Number of Non-Migratable I/O Pins for Stratix II Vertical Migration Paths

Vertical Migration Path	484-Pin FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1020-Pin FineLine BGA	1508-Pin FineLine BGA
EP2S15 to EP2S30	0 (1)	0			
EP2S15 to EP2S60	8 (1)	0			
EP2S30 to EP2S60	8 (1)	8			
EP2S60 to EP2S90				0	
EP2S60 to EP2S130				0	
EP2S60 to EP2S180				0	
EP2S90 to EP2S130			0 (1)	16	17
EP2S90 to EP2S180				16	0
EP2S130 to EP2S180				0	0

Note to Table 1–4:

- (1) Some of the DQ/DQS pins are not migratable. Refer to the Quartus II software information messages for more detailed information.



To determine if your user I/O assignments are correct, run the I/O Assignment Analysis command in the Quartus II software (Processing > Start > Start I/O Assignment Analysis).

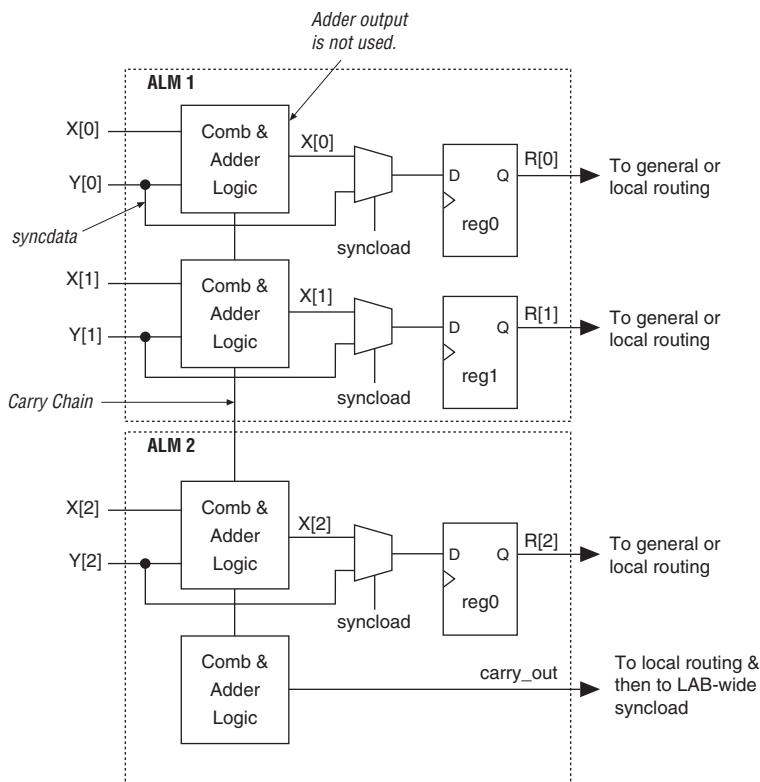


Refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook* for more information on pin migration.

Stratix II devices are available in up to three speed grades, -3, -4, and -5, with -3 being the fastest. [Table 1–5](#) shows Stratix II device speed-grade offerings.

Table 1–5. Stratix II Device Speed Grades

Device	Temperature Grade	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S30	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S60	Commercial	-3, -4, -5		-3, -4, -5		-3, -4, -5	
	Industrial	-4		-4		-4	
EP2S90	Commercial		-4, -5		-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S130	Commercial				-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S180	Commercial					-3, -4, -5	-3, -4, -5
	Industrial					-4	-4

Figure 2–12. Conditional Operation Example

The arithmetic mode also offers clock enable, counter enable, synchronous up/down control, add/subtract control, synchronous clear, synchronous load. The LAB local interconnect data inputs generate the clock enable, counter enable, synchronous up/down and add/subtract control signals. These control signals are good candidates for the inputs that are shared between the four LUTs in the ALM. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Carry Chain

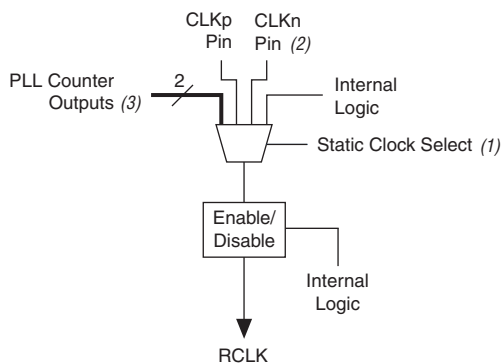
The carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. Carry chains can begin in either the first ALM or the fifth ALM in an LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

Table 2–4. M-RAM Row Interface Unit Signals

Unit Interface Block	Input Signals	Output Signals
L0	datain_a[14..0] byteena_a[1..0]	dataout_a[11..0]
L1	datain_a[29..15] byteena_a[3..2]	dataout_a[23..12]
L2	datain_a[35..30] addressa[4..0] addr_ena_a clock_a clocken_a renwe_a aclr_a	dataout_a[35..24]
L3	addressa[15..5] datain_a[41..36]	dataout_a[47..36]
L4	datain_a[56..42] byteena_a[5..4]	dataout_a[59..48]
L5	datain_a[71..57] byteena_a[7..6]	dataout_a[71..60]
R0	datain_b[14..0] byteena_b[1..0]	dataout_b[11..0]
R1	datain_b[29..15] byteena_b[3..2]	dataout_b[23..12]
R2	datain_b[35..30] addressb[4..0] addr_ena_b clock_b clocken_b renwe_b aclr_b	dataout_b[35..24]
R3	addressb[15..5] datain_b[41..36]	dataout_b[47..36]
R4	datain_b[56..42] byteena_b[5..4]	dataout_b[59..48]
R5	datain_b[71..57] byteena_b[7..6]	dataout_b[71..60]

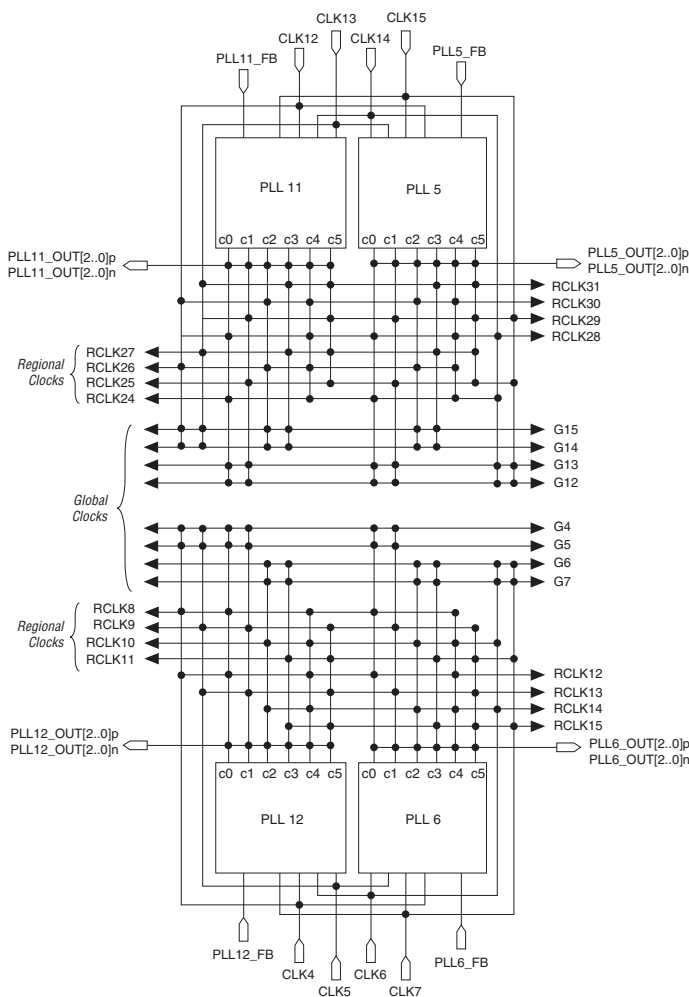


See the *TriMatrix Embedded Memory Blocks in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information on TriMatrix memory.

Figure 2–38. Regional Clock Control Blocks**Notes to Figure 2–38:**

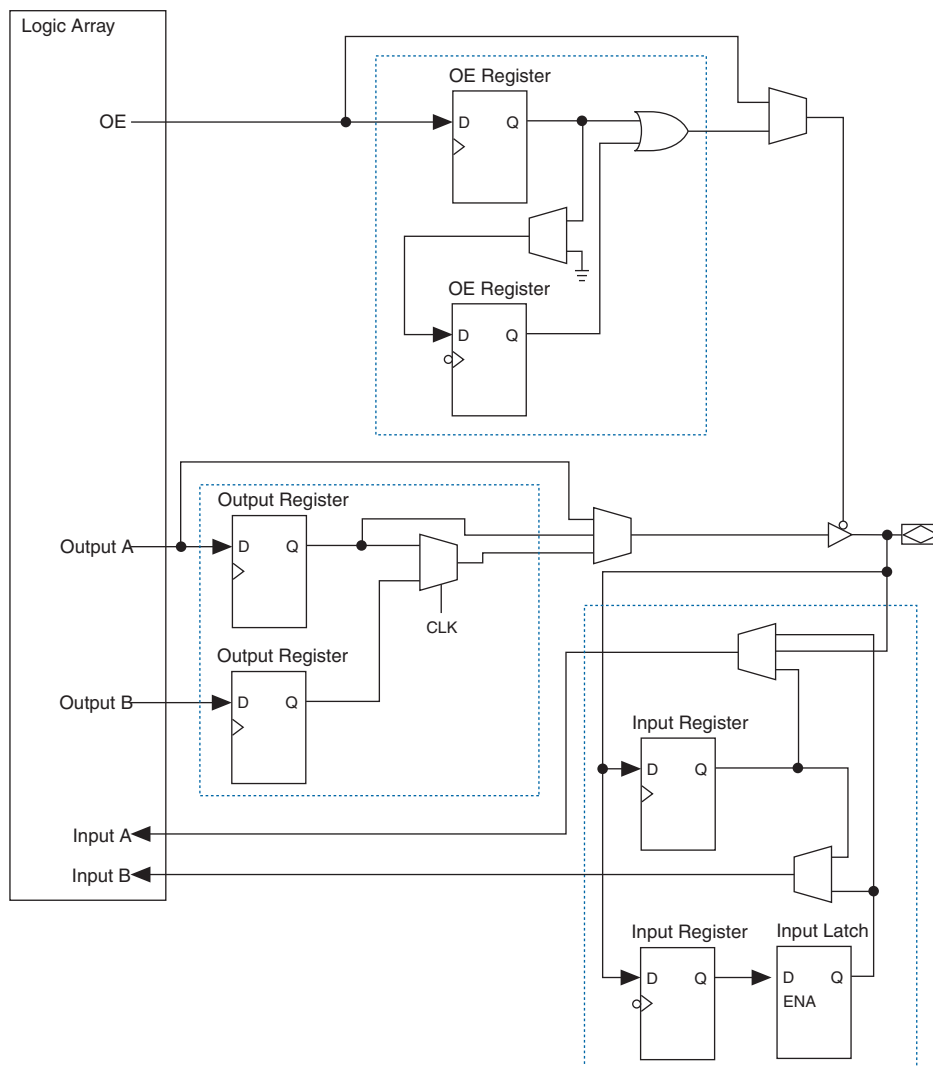
- (1) These clock select signals can only be set through a configuration file (.sof or .pof) and cannot be dynamically controlled during user mode operation.
- (2) Only the CLKn pins on the top and bottom of the device feed to regional clock select blocks. The clock outputs from corner PLLs cannot be dynamically selected through the global clock control block.
- (3) The clock outputs from corner PLLs cannot be dynamically selected through the global clock control block.

Figure 2–43. Global & Regional Clock Connections from Top & Bottom Clock Pins & Enhanced PLL Outputs
Notes (1), (2), and (3)



Notes to Figure 2–43:

- (1) EP2S15 and EP2S30 devices only have two enhanced PLLs (5 and 6), but the connectivity from these two PLLs to the global and regional clock networks remains the same as shown.
- (2) If the design uses the feedback input, you lose one (or two, if FBIN is differential) external clock output pin.
- (3) The enhanced PLLs can also be driven through the global or regional clock networks. The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

Figure 2–46. Stratix II IOE Structure

The IOEs are located in I/O blocks around the periphery of the Stratix II device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects.

Figure 2–47 shows how a row I/O block connects to the logic array.

Figure 2–48 shows how a column I/O block connects to the logic array.

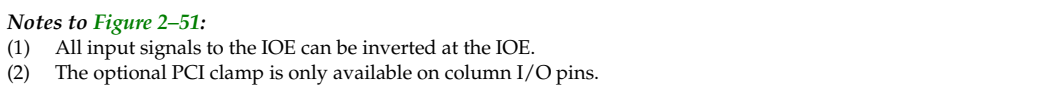
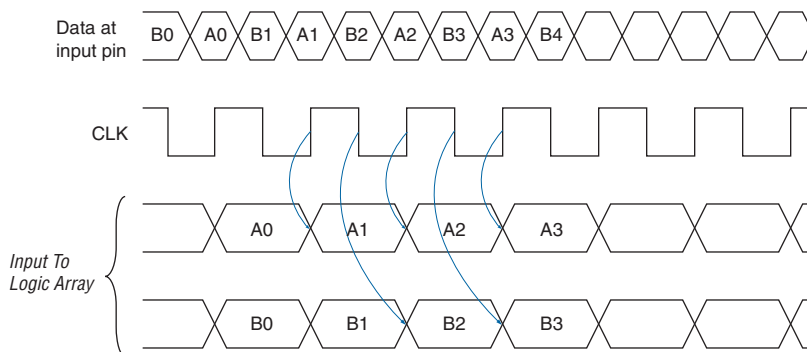
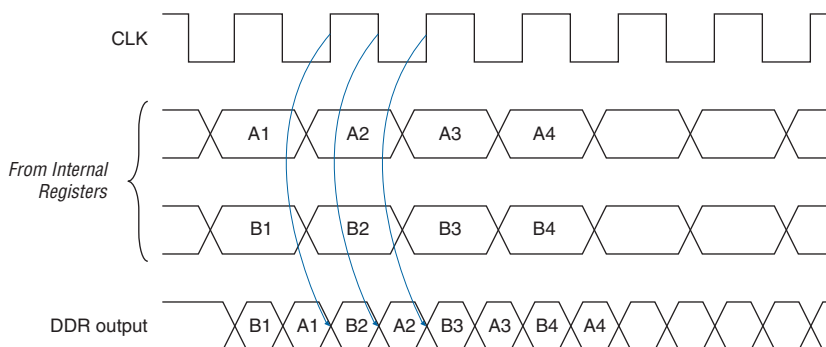


Figure 2–53. Input Timing Diagram in DDR Mode

When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from ALMs on rising clock edges. These output registers are multiplexed by the clock to drive the output pin at a $\times 2$ rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. [Figure 2–54](#) shows the IOE configured for DDR output. [Figure 2–55](#) shows the DDR output timing diagram.

Figure 2–55. Output Timing Diagram in DDR Mode

The Stratix II IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Stratix II devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces. Stratix II devices support DDR and DDR2 SDRAM, QDR II SRAM, RLDRAM II, and SDR SDRAM memory interfaces. In every Stratix II device, the I/O banks at the top (banks 3 and 4) and bottom (banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of $\times 4$, $\times 8/\times 9$, $\times 16/\times 18$, or $\times 32/\times 36$. Table 2–14 shows the number of DQ and DQS buses that are supported per device.

Table 2–14. DQS & DQ Bus Mode Support (Part 1 of 2) *Note (1)*

Device	Package	Number of $\times 4$ Groups	Number of $\times 8/\times 9$ Groups	Number of $\times 16/\times 18$ Groups	Number of $\times 32/\times 36$ Groups
EP2S15	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
EP2S30	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
EP2S60	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
	1,020-pin FineLine BGA	36	18	8	4

Table 2–17 shows the Stratix II on-chip termination support per I/O bank.

Table 2–17. On-Chip Termination Support by I/O Banks (Part 1 of 2)			
On-Chip Termination Support	I/O Standard Support	Top & Bottom Banks	Left & Right Banks
Series termination without calibration	3.3-V LVTTTL	✓	✓
	3.3-V LVCMOS	✓	✓
	2.5-V LVTTTL	✓	✓
	2.5-V LVCMOS	✓	✓
	1.8-V LVTTTL	✓	✓
	1.8-V LVCMOS	✓	✓
	1.5-V LVTTTL	✓	✓
	1.5-V LVCMOS	✓	✓
	SSTL-2 Class I and II	✓	✓
	SSTL-18 Class I	✓	✓
	SSTL-18 Class II	✓	
	1.8-V HSTL Class I	✓	✓
	1.8-V HSTL Class II	✓	
	1.5-V HSTL Class I	✓	✓
	1.2-V HSTL	✓	

Table 2–20. Supported TDO/TDI Voltage Combinations (Part 2 of 2)

Device	TDI Input Buffer Power	Stratix II TDO V_{CCIO} Voltage Level in I/O Bank 4				
		$V_{CCIO} = 3.3\text{ V}$	$V_{CCIO} = 2.5\text{ V}$	$V_{CCIO} = 1.8\text{ V}$	$V_{CCIO} = 1.5\text{ V}$	$V_{CCIO} = 1.2\text{ V}$
Non-Stratix II	VCC = 3.3 V	✓ (1)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 2.5 V	✓ (1), (4)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 1.8 V	✓ (1), (4)	✓ (2), (5)	✓	Level shifter required	Level shifter required
	VCC = 1.5 V	✓ (1), (4)	✓ (2), (5)	✓ (6)	✓	✓

Notes to Table 2–20:

- (1) The TDO output buffer meets $V_{OH}(\text{MIN}) = 2.4\text{ V}$.
- (2) The TDO output buffer meets $V_{OH}(\text{MIN}) = 2.0\text{ V}$.
- (3) An external $250\text{-}\Omega$ pull-up resistor is not required, but recommended if signal levels on the board are not optimal.
- (4) Input buffer must be 3.3-V tolerant.
- (5) Input buffer must be 2.5-V tolerant.
- (6) Input buffer must be 1.8-V tolerant.

High-Speed Differential I/O with DPA Support

Stratix II devices contain dedicated circuitry for supporting differential standards at speeds up to 1 Gbps. The LVDS and HyperTransport differential I/O standards are supported in the Stratix II device. In addition, the LVPECL I/O standard is supported on input and output clock pins on the top and bottom I/O banks.

The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- Parallel RapidIO
- HyperTransport technology

There are four dedicated high-speed PLLs in the EP2S15 to EP2S30 devices and eight dedicated high-speed PLLs in the EP2S60 to EP2S180 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Tables 2–21 through 2–26 show the number of channels that each fast PLL can clock in each of the Stratix II devices. In Tables 2–21 through 2–26 the first row for each transmitter or receiver provides the number of channels driven directly by the PLL. The second row below it shows the maximum channels a PLL can drive if cross bank channels are used from the adjacent center PLL. For example, in the 484-pin FineLine BGA EP2S15

Stratix® II devices offer hot socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a Stratix II board in a system during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot socketing feature also removes some of the difficulty when you use Stratix II devices on printed circuit boards (PCBs) that also contain a mixture of 5.0-, 3.3-, 2.5-, 1.8-, 1.5- and 1.2-V devices. With the Stratix II hot socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Stratix II hot socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter also discusses the power-on reset (POR) circuitry in Stratix II devices. The POR circuitry keeps the devices in the reset state until the V_{CC} is within operating range.

Stratix II Hot-Socketing Specifications

Stratix II devices offer hot socketing capability with all three features listed above without any external components or special design requirements. The hot socketing feature in Stratix II devices allows:

- The device can be driven before power-up without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO} , V_{CCPD} , or V_{CCINT} power supplies. External input signals to I/O pins of the device do not internally power the V_{CCIO} or V_{CCINT} power supplies of the device via internal paths within the device.

Table 5–5. LVTTTL Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{OL}	Low-level output voltage	$I_{OL} = 4 \text{ mA}$ (2)		0.45	V

Notes to Tables 5–5:

- (1) Stratix II devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.
- (2) This specification is supported across all the programmable drive strength settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–6. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} (1)	Output supply voltage		3.135	3.465	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	$V_{CCIO} = 3.0$, $I_{OH} = -0.1 \text{ mA}$ (2)	$V_{CCIO} - 0.2$		V
V_{OL}	Low-level output voltage	$V_{CCIO} = 3.0$, $I_{OL} = 0.1 \text{ mA}$ (2)		0.2	V

Notes to Table 5–6:

- (1) Stratix II devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.
- (2) This specification is supported across all the programmable drive strength available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–7. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} (1)	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.7	V
V_{OH}	High-level output voltage	$I_{OH} = -1 \text{ mA}$ (2)	2.0		V
V_{OL}	Low-level output voltage	$I_{OL} = 1 \text{ mA}$ (2)		0.4	V

Notes to Table 5–7:

- (1) Stratix II devices V_{CCIO} voltage level support of $2.5 \pm -5\%$ is narrower than defined in the Normal Range of the EIA/JEDEC standard.
- (2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–14. 3.3-V PCI Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V _{IL}	Low-level input voltage		–0.3		$0.3 \times V_{CCIO}$	V
V _{OH}	High-level output voltage	I _{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V _{OL}	Low-level output voltage	I _{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–15. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V _{CCIO}	Output supply voltage		3.0		3.6	V
V _{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V _{IL}	Low-level input voltage		–0.30		$0.35 \times V_{CCIO}$	V
V _{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
V _{OH}	High-level output voltage	I _{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V _{OL}	Low-level output voltage	I _{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–16. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V _{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V _{REF}	Reference voltage		0.855	0.900	0.945	V
V _{TT}	Termination voltage		$V_{REF} - 0.04$	V _{REF}	$V_{REF} + 0.04$	V
V _{IH} (DC)	High-level DC input voltage		$V_{REF} + 0.125$			V
V _{IL} (DC)	Low-level DC input voltage				$V_{REF} - 0.125$	V
V _{IH} (AC)	High-level AC input voltage		$V_{REF} + 0.25$			V
V _{IL} (AC)	Low-level AC input voltage				$V_{REF} - 0.25$	V
V _{OH}	High-level output voltage	I _{OH} = –6.7 mA (1)	$V_{TT} + 0.475$			V
V _{OL}	Low-level output voltage	I _{OL} = 6.7 mA (1)			$V_{TT} - 0.475$	V

Note to Table 5–16:

- (1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Power Consumption

Altera® offers two ways to calculate power for a design: the Excel-based PowerPlay Early Power Estimator power calculator and the Quartus® II PowerPlay Power Analyzer feature.

The interactive Excel-based PowerPlay Early Power Estimator is typically used prior to designing the FPGA in order to get an estimate of device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The Power Analyzer can apply a combination of user-entered, simulation-derived and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

In both cases, these calculations should only be used as an estimation of power, not as a specification.



For more information about PowerPlay tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Early Power Estimator* and *PowerPlay Power Analyzer* chapters in volume 3 of the *Quartus II Handbook*.

The PowerPlay Early Power Estimator is available on the Altera web site at www.altera.com. See [Table 5-4 on page 5-3](#) for typical I_{CC} standby specifications.

Timing Model

The DirectDrive™ technology and MultiTrack™ interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix II device densities and speed grades. This section describes and specifies the performance, internal timing, external timing, and PLL, high-speed I/O, external memory interface, and JTAG timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.



The timing numbers listed in the tables of this section are extracted from the Quartus II software version 5.0 SP1.

Preliminary & Final Timing

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. [Table 5-33](#) shows the status of the Stratix II device timing models.

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 2 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
LVCMOS	4 mA	t _{OP}	1041	1091	2036	2136	2340	2448	ps
		t _{DIP}	1061	1113	2102	2206	2416	2538	ps
	8 mA	t _{OP}	952	999	1786	1874	2053	2153	ps
		t _{DIP}	972	1021	1852	1944	2129	2243	ps
	12 mA	t _{OP}	926	971	1720	1805	1977	2075	ps
		t _{DIP}	946	993	1786	1875	2053	2165	ps
	16 mA	t _{OP}	933	978	1693	1776	1946	2043	ps
		t _{DIP}	953	1000	1759	1846	2022	2133	ps
	20 mA	t _{OP}	921	965	1677	1759	1927	2025	ps
		t _{DIP}	941	987	1743	1829	2003	2115	ps
	24 mA (1)	t _{OP}	909	954	1659	1741	1906	2003	ps
		t _{DIP}	929	976	1725	1811	1982	2093	ps
2.5 V	4 mA	t _{OP}	1004	1053	2063	2165	2371	2480	ps
		t _{DIP}	1024	1075	2129	2235	2447	2570	ps
	8 mA	t _{OP}	955	1001	1841	1932	2116	2218	ps
		t _{DIP}	975	1023	1907	2002	2192	2308	ps
	12 mA	t _{OP}	934	980	1742	1828	2002	2101	ps
		t _{DIP}	954	1002	1808	1898	2078	2191	ps
	16 mA (1)	t _{OP}	918	962	1679	1762	1929	2027	ps
		t _{DIP}	938	984	1745	1832	2005	2117	ps

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 5 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVTTTL	OCT 50 Ω	133	152	152	133	152	152	147	152	152
2.5-V LVTTTL	OCT 50 Ω	207	274	274	207	274	274	235	274	274
1.8-V LVTTTL	OCT 50 Ω	151	165	165	151	165	165	153	165	165
3.3-V LVCMOS	OCT 50 Ω	300	316	316	300	316	316	263	316	316
1.5-V LVCMOS	OCT 50 Ω	157	171	171	157	171	171	174	171	171
SSTL-2 Class I	OCT 50 Ω	121	134	134	121	134	134	77	134	134
SSTL-2 Class II	OCT 25 Ω	56	101	101	56	101	101	58	101	101
SSTL-18 Class I	OCT 50 Ω	100	123	123	100	123	123	106	123	123
SSTL-18 Class II	OCT 25 Ω	61	110	110	-	-	-	59	110	110
1.2-V HSTL (2)	OCT 50 Ω	95	-	-	-	-	-	-	-	95

Notes to Table 5–79:

- (1) For LVDS and HyperTransport technology output on row I/O pins, the toggle rate derating factors apply to loads larger than 5 pF. In the derating calculation, subtract 5 pF from the intended load value in pF for the correct result. For a load less than or equal to 5 pF, refer to Table 5–78 for output toggle rates.
- (2) 1.2-V HSTL is only supported on column I/O pins in I/O banks 4,7, and 8.
- (3) Differential HSTL and SSTL is only supported on column clock and DQS outputs.
- (4) LVPECL is only supported on column clock outputs.

Duty Cycle Distortion

Duty cycle distortion (DCD) describes how much the falling edge of a clock is off from its ideal position. The ideal position is when both the clock high time (CLKH) and the clock low time (CLKL) equal half of the clock period (T), as shown in Figure 5–7. DCD is the deviation of the non-ideal falling edge from the ideal falling edge, such as D1 for the falling edge A and D2 for the falling edge B (Figure 5–7). The maximum DCD for a clock is the larger value of D1 and D2.